High-precision Digital Temperature Sensor Optimized for Human Body Temperature Measurement

1 Features

- Optimized for human body temperature measurement
- Temperature measurement accuracy: ± 0.1°C (+30°C to +45°C)
- Power supply voltage: 1. 6V to 5.5V
- Operating temperature: −55 °C to +150 °C
- Conversion current: 40µA
- Standby current: 0.5µA
- Resolution: 16-bit (0.0078125°C)
- Communication interface: I2C, SMBus

2 Applications

- Medical thermometer
- Wearable body temperature monitoring
- High-precision temperature probe

3 Description

The GD30TS310T is a low-cost and high-precision digital temperature sensor optimized for human body temperature measurement. It can achieve 16-bit (0.0078125°C) temperature output without any external temperature sensing unit. And it has a temperature measurement error of less than ±0.1°C within the temperature range from 30°C to 45°C.

The GD30TS310T supports three packaging forms: WLCSP-4 、 MCLGA-4 and DFN6. The former is extremely small in size and is suitable for application scenarios with extremely limited space; the latter transfers heat quickly and is specially designed for human skin surface temperature measurement.

The GD30TS310T supports two-wire communication, can accommodate up to 8 slaves, being compatible with the I2C or SMBus interfaces of most MCUs and SoCs.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
GD30TS310T	WLCSP-4	0.73 mm × 0.73 mm
	MCLGA-4	3.00 mm × 3.00 mm
	DFN6	2.00 mm × 2.00 mm

1. For packaging details, see *Package Information* section.
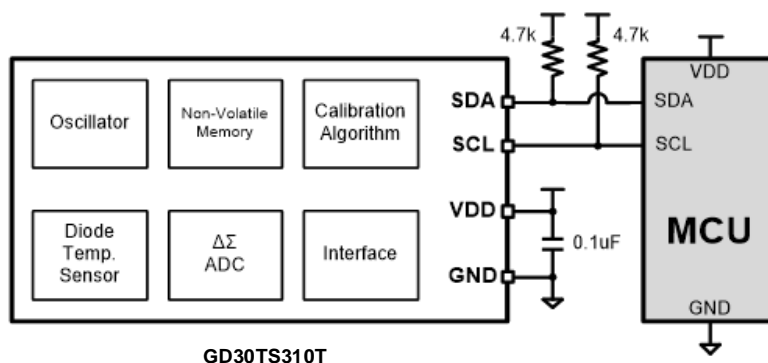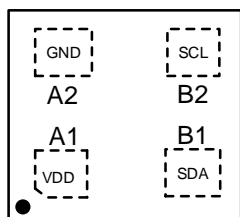
Typical Application Schematic

GD30TS310T

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4 Device Overview

4.1 Pinout and Pin Assignment

WLCSP
Top View

MCLGA
Top View
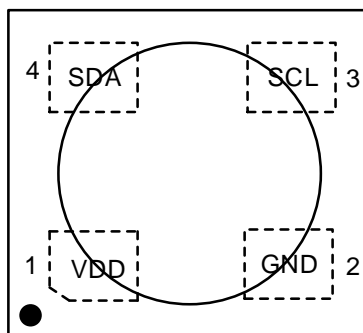
DFN
Top View
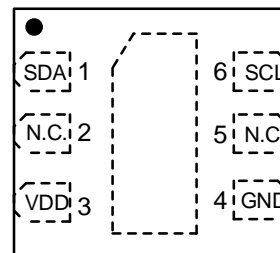
4.2 Pin Description

PINS				PIN TYPE[1]	FUNCTION
NAME	WLCSP	MCLGA	DFN		
VDD	A1	1	3	P	Power pin, it is recommended to add a 0.1uF to 10uF bypass ground capacitor.
GND	A2	2	4	G	Ground.
SCL	B2	3	6	I	Serial clock pin, requires 4.7k pull-up resistor.
SDA	B1	4	1	IO	Serial data pin, requires 4.7k pull-up resistor.
NC			2, 5		No connection.

1. P = power, G = Ground, IO=input and output.

5   Parameter Information

5.1   Absolute Maximum Ratings

Exceeding the operating temperature range (unless otherwise noted)[1]

SYMBOL	PARAMETER	MIN	MAX	UNIT
V_{IO}	Voltage at SCL, SDA	−0.5	6	V
T_J	Junction temperature		150	°C
T_A	Operating temperature	−55	150	°C
T_{stg}	Storage temperature	−60	150	°C

1. Over operating free-air temperature range (unless otherwise noted). Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device.

5.2   Recommended Operation Conditions

SYMBOL[1]	PARAMETER	MIN	TYP	MAX	UNIT
V_+	Supply voltage	1.6	3.3	5.5	V
T_A	Operating Temperature Range	−55		150	°C

1. Unless otherwise stated, over operating free-air temperature range.

5.3   Electrical Sensitivity

SYMBOL[1]	CONDITIONS	VALUE	UNIT
$V_{ESD(HBM)}$	Human Body Mode (HBM), per ANSI/ESDA/JEDEC JS-001	±4000	V
	Latch-Up, per JESD 78, Class IA	±200	mA

1. Unless otherwise stated, over operating free-air temperature range.

5.4 Electrical Characteristics

Unless otherwise specified, the following data are the characteristics of the chip at −40 °C to +125 °C and power supply voltage is in the range of 1.6 V to 5.5 V. (Typical operating conditions are + 25°C and 3.3V)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
T_A	Operating Temperature Range		−55		150	°C
T_{ERROR}	Accuracy (Temperature Error)	+30°C to +45°C, 3.3 V		±0.03125	±0.1	°C
		+10°C to + 60 °C, 3.3V		±0.1	±0.3	°C
		−40°C to +125°C, 3.3V		±0.3	±0.5	°C
	DC Power Supply Sensitivity	−40°C to +125°C			0.1	°C/V
	Resolution			0.0078125		°C
				16		bits
t_{CON}	Conversion Time			60	75	ms
t_{TIME_OUT}	Timeout Time			30		ms
f_C	Communication Frequency	Quick mode	10		400	kHz
		High-speed mode	0.01		2.5	
V_+	Power Supply Voltage		1.6	3.3	5.5	V
	Operating Current	Conversion period		40	80	μA
		Standby period		0.5	3	μA
	Pull-up Resistor		0.5	4.7	10	kΩ

6 Functional Description

6.1 Temperature Output

The 15-bit (EM=0) or 16-bit (EM=1) digital output of each temperature measurement is held in a read-only temperature register, where 1 LSB = 0.0078125°C, and negative numbers are represented in two's complement form. When EM=0, the lowest bit of the temperature register always reads 0.

To retrieve the temperature output, reading of two bytes is required. The first byte is the most significant byte (MSB), followed immediately by byte 2 which is the least significant byte (LSB). The left-aligned upper 15 bits (EM=0) or 16 bits (EM=1) are used to indicate the temperature. If a temperature resolution of less than 1°C (EM=0) or 2°C (EM=1) is not required, the user can choose not to read byte 2.

Table 1. Temperature Data Format (15bit, EM=0)

Temperature (°C)	Digital Output (Binary)				Digital Output (Hex)
+150 .0000000	0111	1111	1111	1110	7FFE
+127.9921875	0111	1111	1111	1110	7FFE
+125.0000000	0111	1101	0000	0000	7D00
+85.0000000	0101	0101	0000	0000	5500
+27.0000000	0001	1011	0000	0000	1B00
+0.0078125	0000	0000	0000	0010	000 2
+0.0000000	0000	0000	0000	0000	0000
−0.0078125	1111	1111	1111	1110	FFFE
−55.0000000	1100	1001	0000	0000	C900

Table 2. Temperature Data Format (16bit, EM= 1)

Temperature (°C)	Digital Output (Binary)				Digital Output (Hex)
+150 .0000000	0100	1011	0000	0000	4B00
+127.9 921875	0011	1111	1111	1111	3FFF
+125.0000000	0011	1110	1000	0000	3E80
+85.0000000	0010	1010	1000	0000	2A80
+27.0000000	0000	1101	1000	0000	0D80
+0.0078125	0000	0000	0000	0001	0001
+0.0000000	0000	0000	0000	0000	0000
−0.0078125	1111	1111	1111	1111	FFFF
−55.0000000	1110	0100	1000	0000	E480

1. Table 1 and Table 2 do not provide data formats for all temperatures.

6.2 Register Maps

The GD30TS310T internal register stack consists of four 16-bit registers, and the mapping relationship is shown in Table 3. The specific content of the register is shown in Table 4 to Table 9.

Table 3. Register Stack and its Pointers

Pointer	Register	Attributes	Initial Value
0x00	Temperature	R	0x0000
0x01	Configuration	R/W	0x00C0
0x02	Low threshold	R/W	0x4B00
0x03	High threshold	R/W	0x5000

1. R stands for read-only; R/W stands for read-write.

Table 4. Temperature Register (EM=0)

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Binary	T14	T13	T12	T11	T10	T9	T8	T7	T6	T5	T4	T3	T2	T1	T0	0
Temperature	sign	64	32	16	8	4	2	1	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	-
Attributes	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

1. R stands for read-only; R/W stands for read-write. Sign indicates the sign bit, 0=positive number, 1=negative number.

Table 5. Temperature Register (EM=1)

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Binary	T15	T14	T13	T12	T11	T10	T9	T8	T7	T6	T5	T4	T3	T2	T1	T0
Temperature	sign	128	64	32	16	8	4	2	1	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}
Attributes	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

1. R stands for read-only; R/W stands for read-write. Sign indicates the sign bit, 0=positive number, 1=negative number.

Table 6. Configuration Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Binary	ALT	-	-	FQ1	FQ0	-	TM	SD	EM	-	-	TO	EC	CR1	CR0	OS
Default	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0
Attributes	R	R	R	R/W	R/W	R	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W

1. R stands for read-only; R/W stands for read-write. "-" represents a reserved bit.

Table 7. Configuration Register Content Description

PARAMETER	DESCRIPTION
ALT	Over-temperature alarm flag ALT=0: The temperature output sits between the high and low thresholds ALT=1: The temperature output exceeds the high and low thresholds
FQ	Error queue depth, i.e., the number of consecutive over-temperature events required to trigger the ALT. FQ=0x0: 1 time (default) FQ=0x1: 2 times FQ=0x2: 4 times FQ=0x3: 6 times
TM	Over-temperature alarm mode TM=0: Comparison mode (default) TM=1: Interrupt mode
SD	Shutdown mode control SD=0: Continuous conversion mode (default) SD=1: Shutdown mode
EM	Extended mode EM=0: The temperature output is 15 bits EM=1: The temperature output is 16 bits (default)
TO	Timeout reset function TO=0: Turn on the timeout reset function (default) TO=1: Turn off the timeout reset function
EC	Error check function EC=0: Turn off error checking function (default) EC=1: Turn on error checking function
CR	Temperature refresh rate CR=0x0: 0.25Hz (default) CR=0x1: 1.0Hz CR=0x2: 4.0Hz CR=0x3: 8.0Hz
OS	Single conversion status bit OS=0: Single conversion completed (default) OS=1: Single conversion in progress. Writing this bit to 1 in Shutdown mode will start a temperature conversion

Table 8. Low Threshold Register

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EM=0	L14	L13	L12	L11	L10	L9	L8	L7	L6	L5	L4	L3	L2	L1	L0	0
EM=1	L15	L14	L13	L12	L11	L10	L9	L8	L7	L6	L5	L4	L3	L2	L1	L0
Default	0	1	0	0	1	0	1	1	0	0	0	0	0	0	0	0
Attributes	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

1. R stands for read-only; R/W stands for read-write. "-" represents a reserved bit.

Table 9. High Threshold Register

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EM=0	H14	H13	H12	H11	H10	H9	H8	H7	H6	H5	H4	H3	H2	H1	H0	0
EM=1	H15	H14	H13	H12	H11	H10	H9	H8	H7	H6	H5	H4	H3	H2	H1	H0
Default	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
Attribute s	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W

1. R stands for read-only; R/W stands for read-write. "-" represents a reserved bit.

The high (low) threshold register has the same data format as the temperature register. Modifying the EM bit in the configuration register will only change the way the value of the high (low) threshold register is parsed (that is, using 15-bit temperature or 16-bit temperature), and does not perform any shift operations on the high (low) threshold register itself. Therefore, when the EM bit changes, the user needs to update the high (low) threshold register in a timely manner, otherwise, it may lead to errors in the over-temperature alarm function.

6.3 Operating Mode

6.3.1 Continuous Conversion

The GD30TS310T defaults to continuous conversion mode (SD=0) when power-on. In this mode, the GD30TS310T regularly samples the surface temperature of the chip, and the conversion result is stored in the temperature register, overwriting the previous result. The temperature conversion takes approximately 60ms, with a static current of 40μA (under typical conditions); after the conversion ends, it enters a idle state, with a static current of 2μA (under typical conditions). The duration of the idle state is determined by the temperature refresh rate, which is 0.25Hz by default (CR=0x0) for GD30TS310T upon power-on, meaning the temperature is refreshed once every 4 seconds, as shown in Figure 1. Lower refresh rates can achieve lower average power consumption.
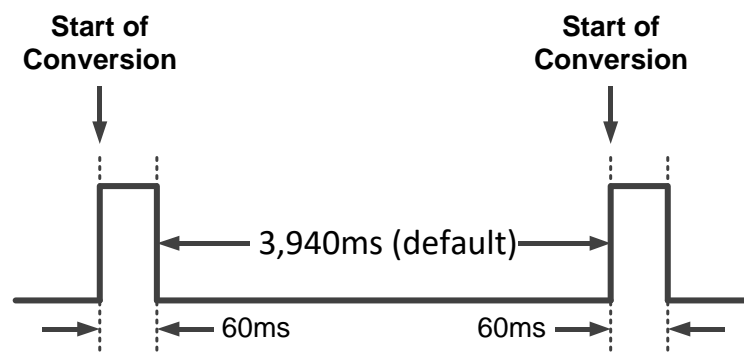
Figure 1. Temperature Refresh Rate

6.3.2 Shutdown Mode

Shutdown mode of the device allows the user to conserve power by shutting down all device circuitry except the serial interface, thereby reducing the quiescent current to less than 0.5μA (under typical conditions). Shutdown mode is initiated when writing SD=1, and the GD30TS310T will shut down after the current conversion is completed. The GD30TS310T will re-enter continuous conversion mode when writing SD=0 to exit shutdown mode.

6.3.3 Single Conversion

When GD30TS310T is in shutdown mode, writing OS=1 can trigger a temperature conversion; once the conversion is completed, the GD30TS310T will automatically turn on shutdown mode again. If continuous temperature measurement is not required, this function can significantly save chip power consumption. It should be noted that if the GD30TS310T is in continuous conversion mode, writing OS=1 will have no effect and the OS bit will always be read as 0.

6.4 Alarm Mode

6.4.1 Comparison Mode

The GD30TS310T defaults to comparison mode (TM=0) when power-on. In this mode, if the temperature measurement result is equal to or exceeds the high threshold for a number of consecutive times, reaching the value defined by the FQ bit in the configuration register, then the over-temperature alarm flag ALT bit in the configuration register will be activated. The ALT bit remains active until the temperature measurement result is equal to or lower than the low threshold for a number of consecutive times, reaching the value defined by the FQ bit in the configuration register. The difference between the high and low thresholds appears as hysteresis in the comparator output, and the error queue defined by the FQ bit can effectively avoid false alarms caused by environmental disturbances.

6.4.2 Interrupt Mode

The GD30TS310T can be configured in interrupt mode (TM=1). In this mode, if the temperature measurement result is equal to or exceeds the high threshold for a number of consecutive times, reaching the value defined by the FQ bit in the configuration register, then the over-temperature alarm flag ALT bit in the configuration register will be activated. The ALT bit remains active until the user reads any register. After the ALT bit is cleared, the ALT bit will be activated again only when the temperature measurement result is equal to or lower than the low threshold for a number of consecutive times reaching the value defined by the FQ bit in the configuration register, and will remain activated until the next user read Take the occurrence of any register action. The cycle goes back and forth.

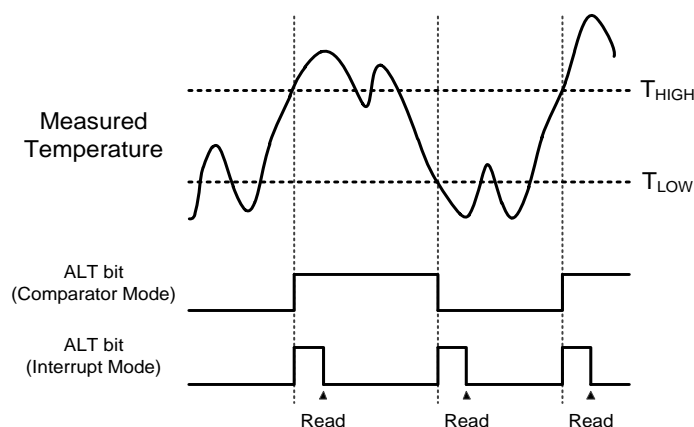The working diagram of the two alarm modes is shown in Figure 2.

Figure 2. Working Diagram of Over-temperature Alarm

6.5 Serial Interface

6.5.1 Bus Overview

I2C/SMBus is a two-wire serial communication interface that supports multiple masters and multiple slaves. Among them, the device that initiates communication is called the host, and the device controlled by the host is called the slave. The host is responsible for generating the serial clock (SCL) to control bus access and the generation of start and stop conditions (START/STOP).

Data transfer is in bytes, with 1 Ack bit appended every 8 clocks. During data transfer, SDA must remain stable while SCL is high because the falling edge of SDA during the high level of SCL is defined as the start condition (START); the rising edge of SDA is defined as the stop condition (STOP). These two represent the beginning and end of communication respectively. The standard I2C/SMBus protocol stipulates a series of timing parameters, whose definition and range are shown in Figure 3 and Table 10 respectively.

Table 10. I2C/SMBus Timing Characteristics

| SYMBOL	PARAMETER	STANDARD MODE		HIGH-SPEED		UNIT
		MIN	MAX	MIN	MAX	
f	SCL clock frequency	10	400	10	2700	kHz
$t_{SU:STA}$	Start condition: establishment time	0.6		0.26		us
$t_{HD:STA}$	Start condition: hold time	0.6		0.26		us
$t_{SU:STO}$	Stop condition: Setup time	0.6		0.26		us
t_{BUF}	Idle time between start and stop	1.3		0.5		us
$t_{SU:DAT}$	SDA data: Setup time	0.1		0.05		us
$t_{HD:DAT}$	SDA data: hold time	0		0		us
t_{HI}	SCL clock: high level time	0.6		0.26		us
t_{LOW}	SCL clock: low level time	1.3		0.5		us
t_R	SDA/SCL bus rise time		300		120	ns
t_F	SDA/SCL bus fall time		300		120	ns
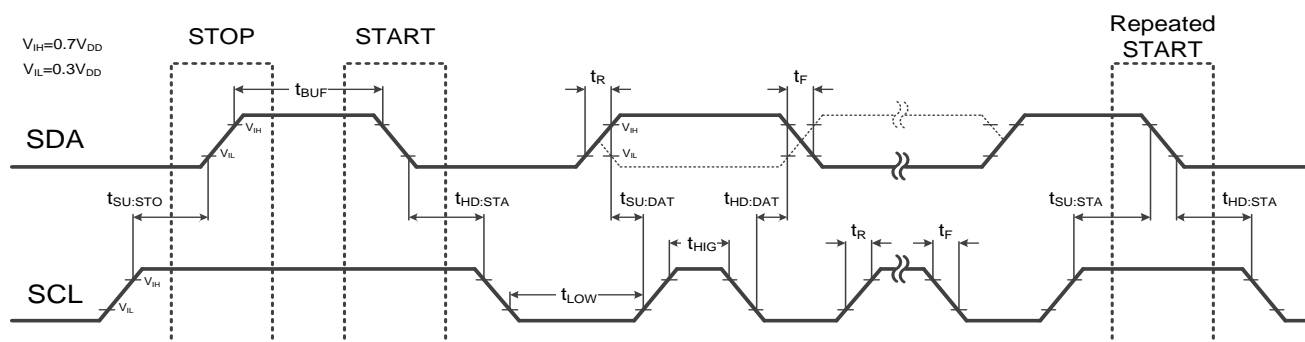
Figure 3. I²C/SMBus Timing Definition

6.5.2 Slave Address

Table 11. Mapping Relationship between Product Number and Slave Address

Product Number	Slave Address (R/W)	Product Number	Slave Address (R/W)
GD30TS310T-I	0x48	GD30TS310T-I4C	0x4C
GD30TS310T-I49	0x49	GD30TS310T-I4D	0x4D
GD30TS310T-I4A	0x4A	GD30TS310T-I4E	0x4E
GD30TS310T-I4B	0x4B	GD30TS310T-I4F	0x4F

6.5.3 Read and Write Operations

To communicate with the GD30TS310T, the master must first address slave devices through an address byte. The address byte has seven address bits and a read-write (R/W) bit. The GD30TS310T uses product numbers to distinguish address bits. The specific mapping relationship is shown in Table 11. It supports up to 8 slaves being connected at the same time. The read and write flag bits are used to indicate the data transfer direction, 0b represents host writing; 1b represents host reading. Data transfer starts with the highest bit.

The GD30TS310T uses a pointer register to indicate the name of the register operated by the current read and write process. The pointer register is the second byte of the host write operation. Each write operation to the GD30TS310T needs to be written to the pointer register, as shown in Figure 4. The two data bytes immediately following the pointer byte represent the data to be written to the specified register. The host read operation needs to modify the pointer register first, and then send (repeatedly) the start condition and the slave address byte (R/W=1) to change the data transmission direction, thereby allowing the GD30TS310T to send the target register selected by the pointer to the bus. The data is shown in Figure 5.

6.5.4 Error Check

The GD30TS310T supports communication data error check function, which is turned on or off controlled by the EC bit in the configuration register. When the function is turned on, each read and write operation will be accompanied by an additional CRC-8 check byte. The checked data includes all bytes from the start condition to the stop condition (excluding the check byte itself). The generator polynomial is: $G(x) = x8 + x2 + x1 + 1$. The specific timing sequence is shown in Figure 6 and Table 7.

(1) Take reading the initial power-on value of the low threshold register as an example:

START + 0x90 + 0x02 + Re-START + 0x91 + 0x4B+ 0x00 + ECB + STOP

ECB = CRC8 (0x90, 0x02, 0x91, 0x4B, 0x00) = 0x87

(2) Take writing the configuration register as an example:

START + 0x90 + 0x01 + 0x00 + 0x08 + ECB + STOP

ECB = CRC8 (0x90, 0x01, 0x00, 0x08) = 0x05

Note: If EC=1 when writing the configuration register, the write operation must be accompanied by the correct check byte, otherwise the write operation will be invalid.
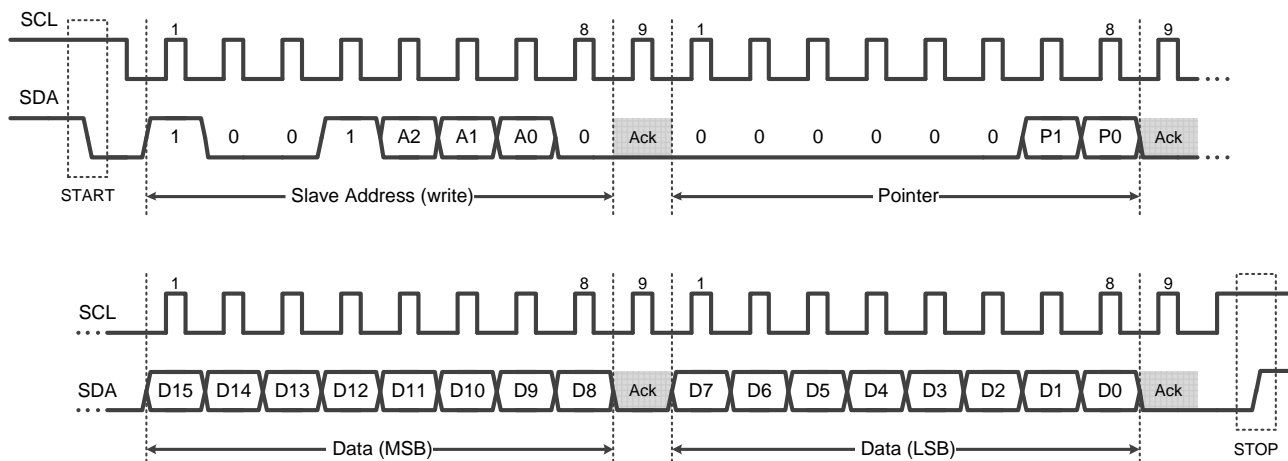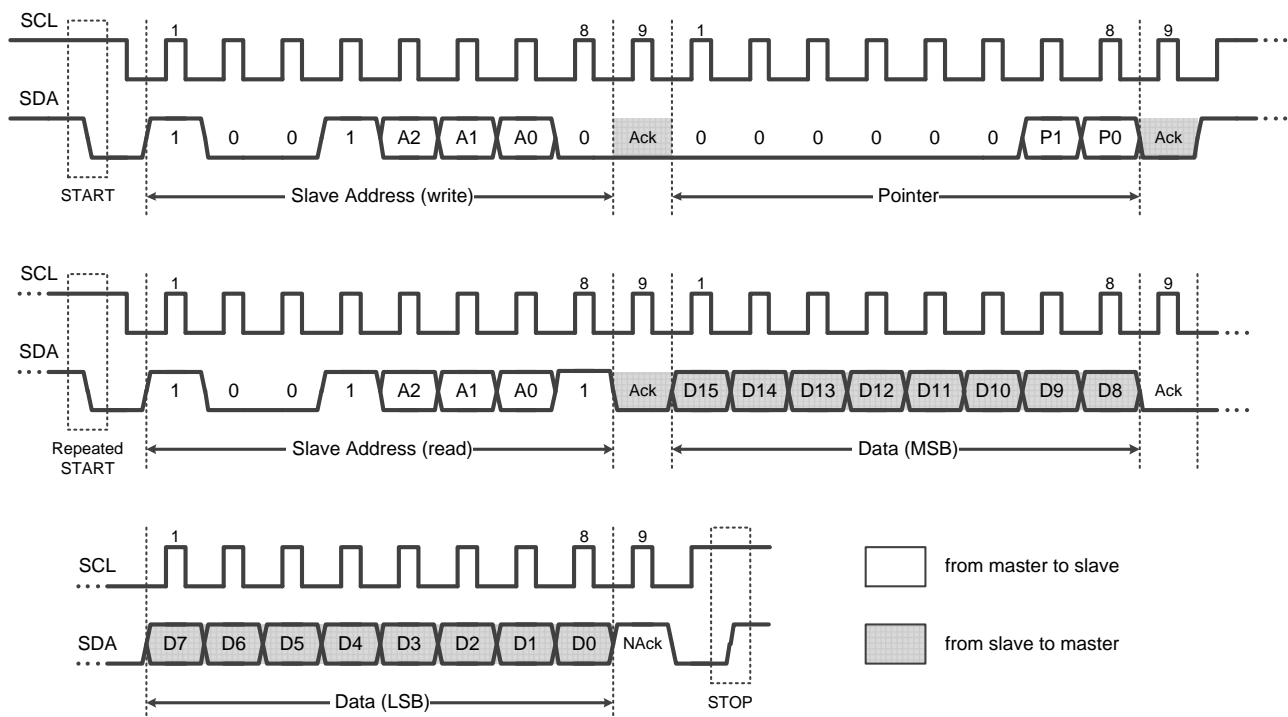
Figure 4. Write Operation Timing Diagram (EC=0)
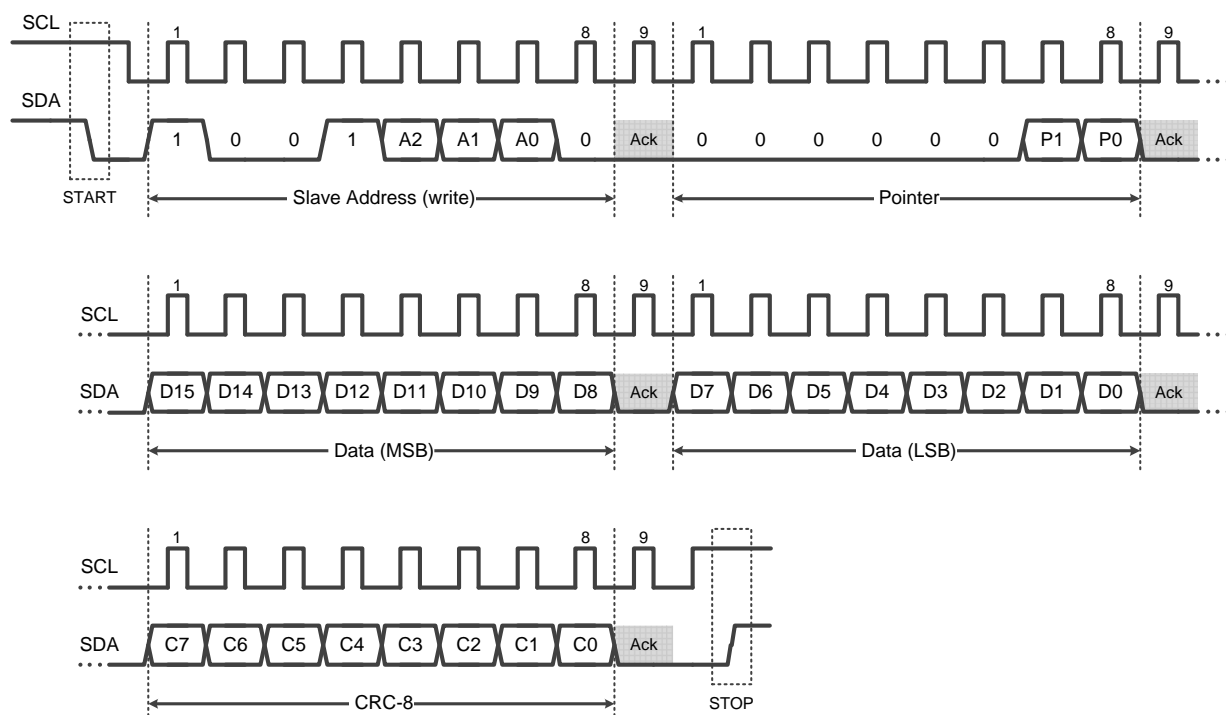

Figure 5. Read Operation Timing Diagram (EC=0)

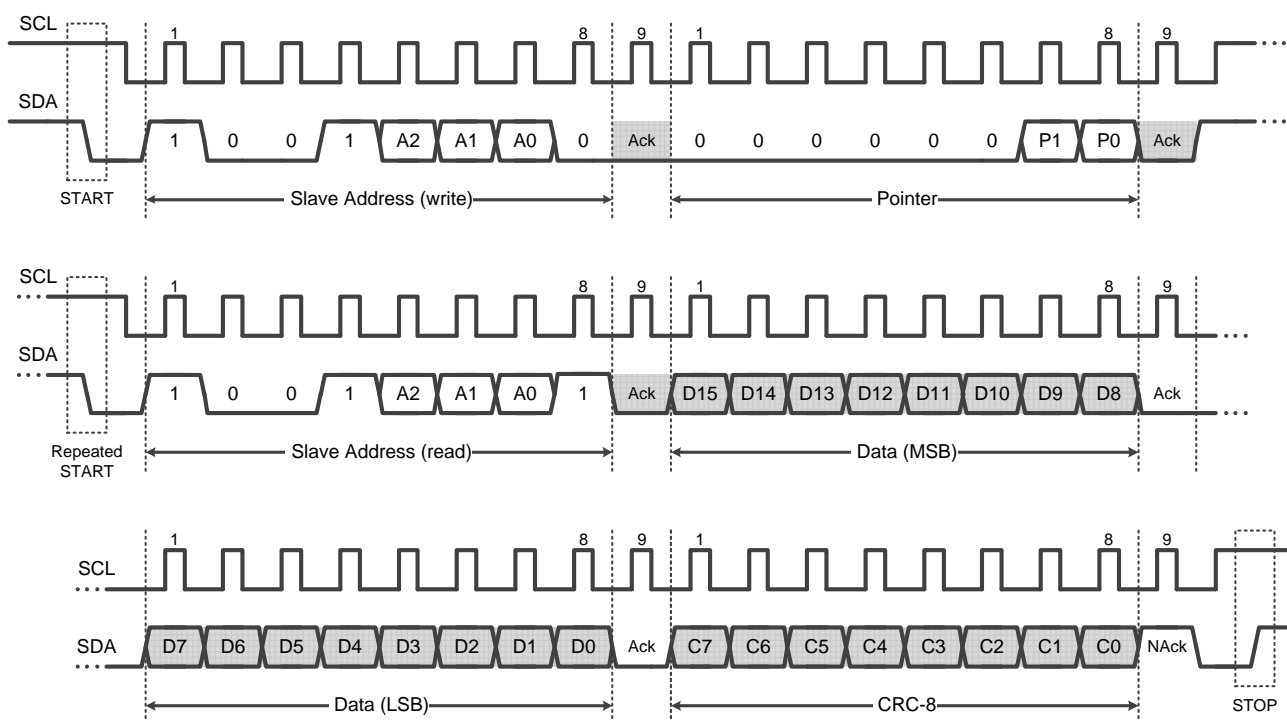**Figure 6. Write Operation Timing Diagram (EC=1)**

Figure 7. Read Operation Timing Diagram (EC=1)

6.5.5 Timeout Reset

The GD30TS310T features timeout reset function, which is turned on or off controlled by the TO bit in the configuration register. When the function is turned on, if SDA or SCL remains low for more than 30ms (typical) between the start condition and the stop condition, the GD30TS310T will automatically reset its serial interface, release the SDA bus and wait for the next communication to start. This function can effectively avoid bus deadlock and improve system stability; However, it will limit the minimum SCL clock frequency to no less than 10kHz.

6.5.6 General-call Reset

The GD30TS310T will respond to the general-call address, 0x00). If the second byte after the general-call address is a reset command (0x06), the GD30TS310T will respond to this byte and reset the internal register file to the initial power-on state. The specific timing is shown in Figure 8.
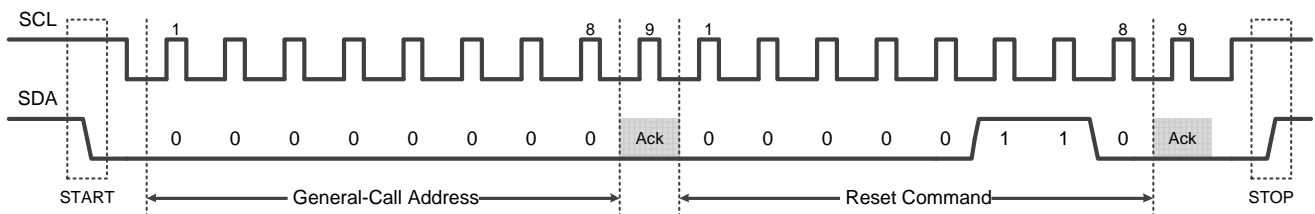

Figure 8. General-call Reset Timing Diagram

6.5.7 High-speed Mode

The GD30TS310T supports serial interface in operating at frequencies above 400kHz. The host sends a high-speed mode code (0000 1xxx) after the start condition. The GD30TS310T will not respond to this byte, but will switch the input and output filters of the SDA and SCL pins to high-speed mode, allowing the bus to transmit data at up to 2.7MHz. The GD30TS310T will continue to operate in high-speed mode until a stop condition occurs on the bus. Once a stop condition is received, the GD30TS310T switches the input and output filters back to standard mode. The specific timing is shown in Figure 9. (Take write operation as an example)
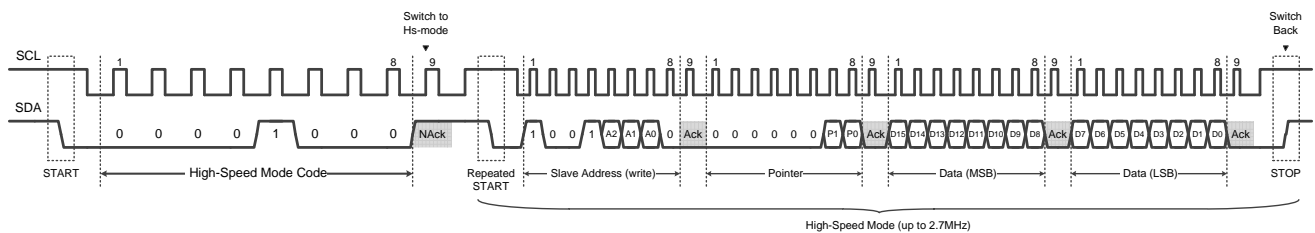

Figure 9. High-speed Mode Timing Diagram (Taking write operation as an example)

7 Application Information

The average power consumption of the GD30TS310T is extremely low (less than 3uA under default conditions), so an RC filter circuit can be added to the power pin to further reduce the impact of power supply noise. As shown in Figure 10, the resistance must be less than 1kΩ, the capacitance must be more than 0.1µF, and the power supply pin voltage cannot be less than 1.6V.
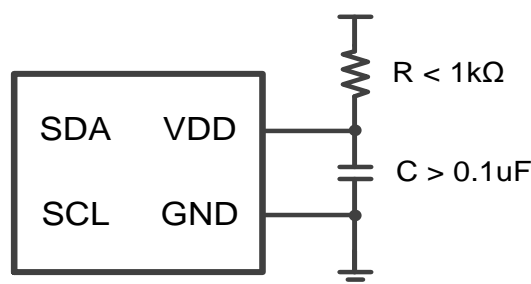

Figure 10. Power Supply Noise Suppression Technology

The GD30TS310T should be kept as far away from noise sources as high-speed digital buses, coil components, and wireless antennas. GD recommends placing a low ESR ceramic capacitor between the power pin and the ground pin to filter out power supply noise. This capacitor needs to be as close as possible to the power pin, and the recommended value is 0.1µF. Under severe noise environments, GD recommends using multiple different capacitance values in parallel, such as 1µF+0.1µF+0.01µF, etc., to filter out digital noise in multiple frequency ranges.

The GD30TS310T should be as close as possible to the heat source being monitored, and use an appropriate layout to achieve good thermal coupling to ensure that temperature changes are captured in the shortest time interval. The average power consumption of GD30TS310T is extremely low (less than 9µW under default conditions), and self-heating due to power consumption is negligible.

8 Package Information

8.1 Outline Dimensions

WLCSP-4

Top View

Pin A1 Mark

Bottom View
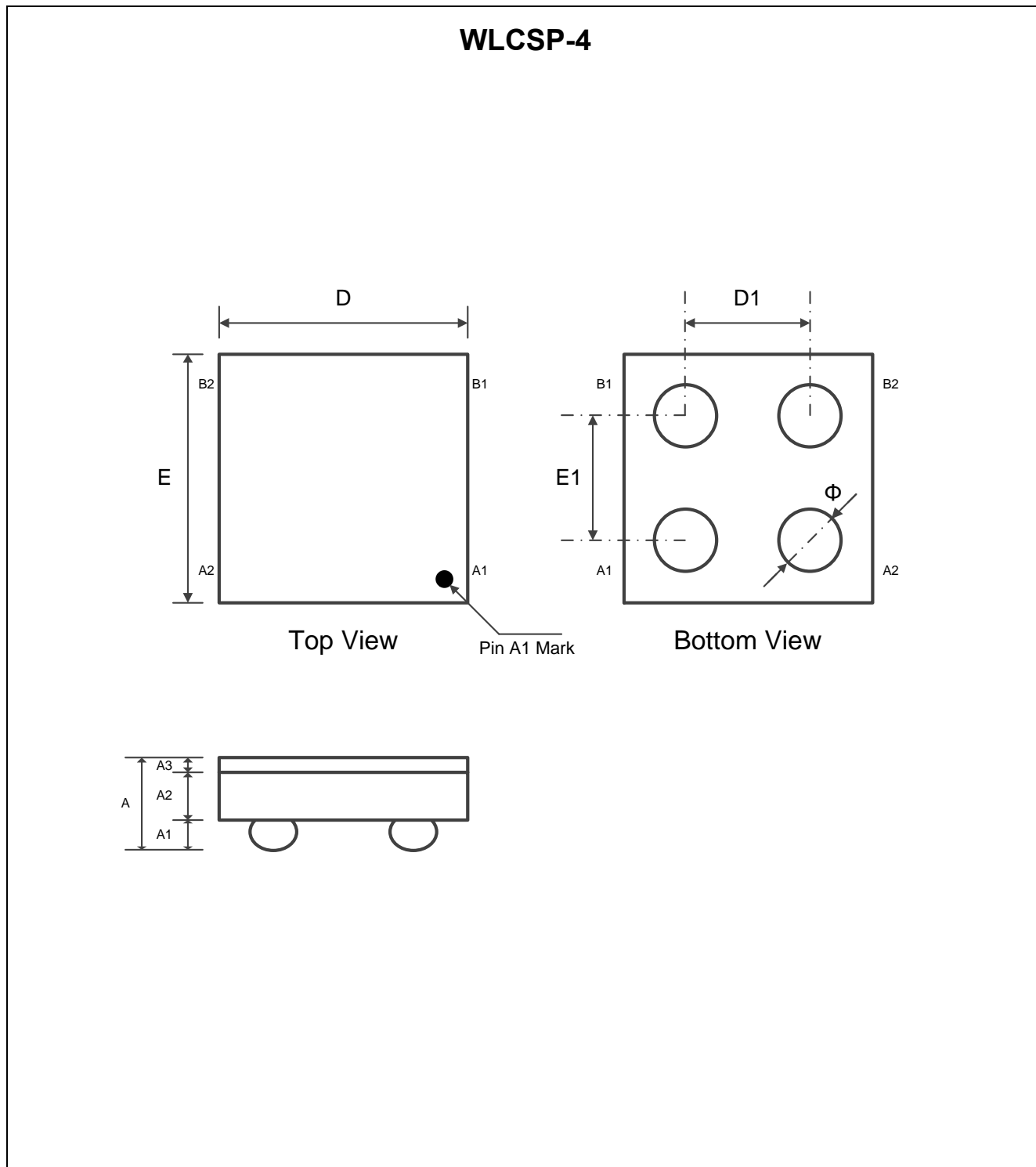
NOTES:

1. All dimensions are in millimeters.

2. Package dimensions does not include mold flash, protrusions, or gate burrs.

3. Refer to the Table 12. *WLCSP-4 dimensions(mm)*.

Table 12. WLCSP-4 dimensions(mm)

SYMBOL	MIN	NOM	MAX
A	0.5	0.54	0.58
A1	0.16	0.18	0.20
A2	0.30	0.32	0.34
A3	0.04	0.04	0.04
D	0.70	0.73	0.76
E	0.70	0.73	0.76
Φ	0.22	0.235	0.25
D1	0.4 BSC		
E1	0.4 BSC		

MCLGA-4

Top View

Bottom View

Pin 1 Mark

Pin 1

Side View
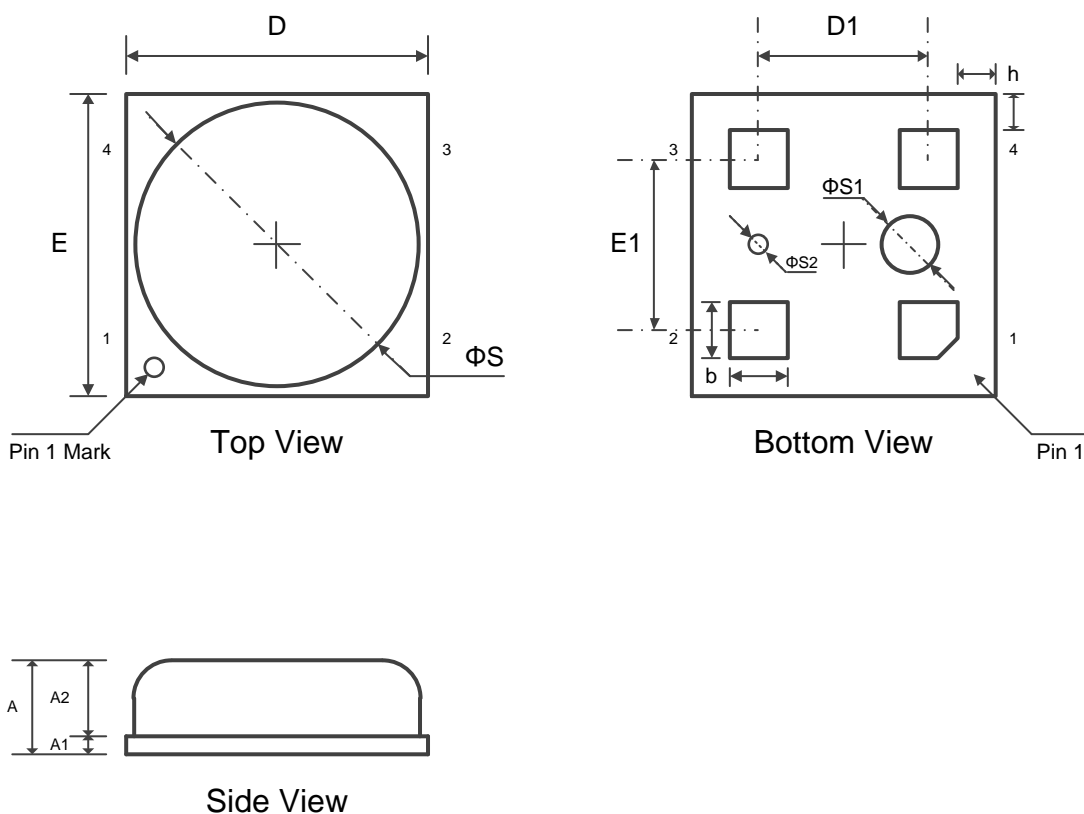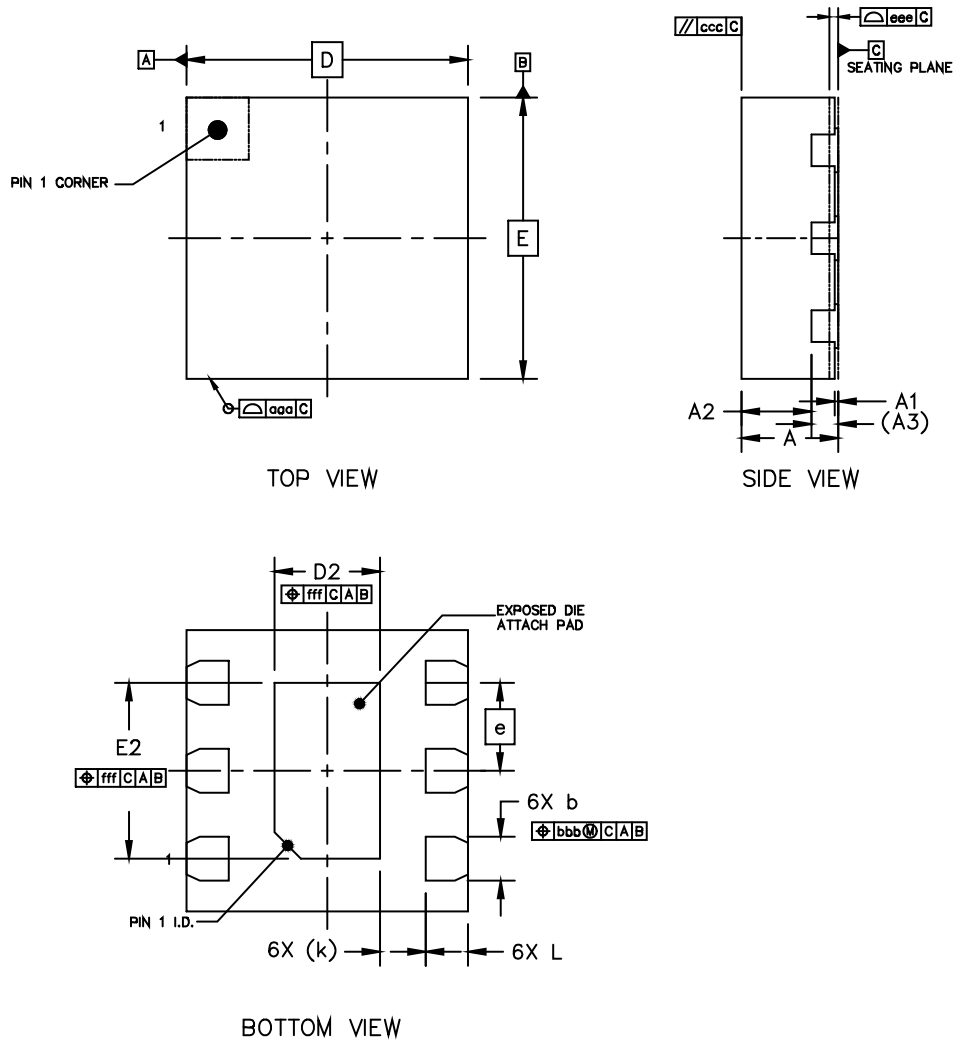
NOTES: (continued)

1. Refer to the Table 13. *WCLGA-4 dimensions(mm)*.

Table 13. WCLGA-4 dimensions(mm)

SYMBOL	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.20	0.25	0.30
A2	0.70	0.75	0.80
D	2.90	3.00	3.10
E	2.90	3.00	3.10
D1	1.80 BSC		
E1	1.80 BSC		
b	0.55	0.60	0.65
h	0.25	0.30	0.35
ΦS	2.70	2.80	2.90
ΦS1	0.55	0.60	0.65
ΦS2	0.15	0.20	0.25

DFN-6

TOP VIEW

SIDE VIEW

BOTTOM VIEW

NOTES: (continued)

1. Refer to the Table 14. *DFN-6 dimensions(mm)*.

Table 14. DFN-6 dimensions(mm)

SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.20	0.25	0.30
b1	0.18 REF		
c	0.203 REF		
D	1.90	2.00	2.10
D2	0.60	0.70	0.80
E	1.90	2.00	2.10
E2	1.50	1.60	1.70
e	0.50 BSC		
K	0.30 REF		
L	0.30	0.35	0.40
h	0.20	0.25	0.30

9 Ordering Information

Ordering Code	Package Type	ECO Plan	Packing Type	MOQ	OP Temp(°C)
GD30TS310TJVTY-I	MCLGA-4	Green	Tray	490	−55°C to +150°C
GD30TS310TJYTR-I	WLCSP-4	Green	Tape & Reel	3000	−55°C to +150°C
GD30TS310TSETR-I	DFN-6	Green	Tape & Reel	4000	−55°C to +150°C
GD30TS310TJVTY-I4x	MCLGA-4	Green	Tray	490	−55°C to +150°C
GD30TS310TJYTR-I4x	WLCSP-4	Green	Tape & Reel	3000	−55°C to +150°C
GD30TS310TSETR-I4x	DFN-6	Green	Tape & Reel	4000	−55°C to +150°C

1. The 4x in the ordering code represents the slave address, ranging from 0x49 to 0x4F(7Bit). Without "4x," it represents the slave address as 0x48(7Bit).

10 Revision History

REVISION NUMBER	DESCRIPTION	DATE
1.0	Initial release and device details	2024
1.1	Add slave address description in the *Ordering Information*.	2025
1.2	Modify slave address description in the *Ordering Information* and section 6.5.2 *Slave Address*.	2025

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