Series Low Power Digital Temperature Sensor in WLCSP Package, Compatible with SMBus and I²C Communication

1 Features

- Multiple Device Access (MDA):
  – Global read and write operations
- Temperature range: −40°C to +125°C
- Temperature accuracy:
  – ±1°C (−40°C to +125°C)
- Supply voltage range:
  – 1.4V to 2.8V
- Low quiescent current：
  – Normal operation: ≤3uA (0.25Hz)
  – Off mode: ≤1μA
- Resolution:
  – 8bits(GD30TS103N)
- Digital output：compatible with SMBus™ and I²C interface
- Package:
  – 4-Ball WLCSP(DSBGA)

2 Applications

- Phone
- Laptop
- Solid State Drive (SSDs)
- Server
- Set top box
- Low power environment
- Sensor

3 Description

The GD30TS103N series temperature sensors are all in 4-Ball wafer-level packages, of which the GD30TS103N has a resolution of 1°C.

The two-wire interface of the GD30TS103N series is compatible with SMBus and I²C communication modes, and supports multi-chip access (MDA) commands, which can realize the communication between the host and multiple chips on the bus at the same time, without sending separate read and write commands to each GD30TS103N series chip. GD30TS103N supports up to 8 different address chips to be mounted on a main line.

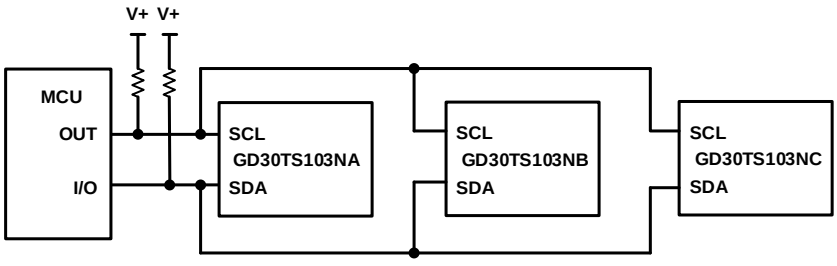
The GD30TS103N series is suitable for the system with limited temperature measurement area, temperature sensitivity, and multi-temperature area measurement and monitoring. The rated operating temperature range of the GD30TS103N series is −40°C to +125°C.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
GD30TS103N	WLCSP(4)	0.88mm × 0.88mm

1. For packaging details, see *错误!未找到引用源。* section.

GD30TS103N Application Diagram



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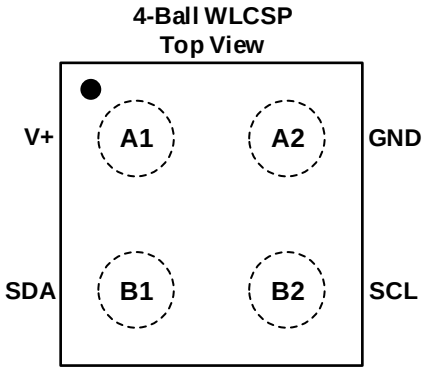
4 Device Overview

4.1 Pinout and Pin Assignment



4.2 Pin Description

PINS		PIN TYPE[1]	FUNCTION
NAME	NUM		
V+	A1	P	Supply voltage
GND	A2	G	Ground.
SDA	B1	I/O	Serial data input. Open-drain output, requires a pull-up resistor.
SCL	B2	O	Serial clock. Open-drain output, requires a pull-up resistor.

1. P = power, G = Ground, O = Output, I/O=input/output.

5 Parameter Information

5.1 Absolute Maximum Ratings

Exceeding the operating temperature range (unless otherwise noted)[1]

SYMBOL	PARAMETER	MIN	MAX	UNIT
V_+	Power supply		4	V
V_{IO}	Voltage at SCL, SDA	0.3	((V+)+0.3) and ≤ 4	V
T_J	Junction temperature		150	°C
T_A	Operating temperature	−55	160	°C
T_{stg}	Storage temperature	−60	150	°C

1. Over operating free-air temperature range (unless otherwise noted). Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device.

5.2 Recommended Operation Conditions

SYMBOL[1]	PARAMETER	MIN	TYP	MAX	UNIT
V_+	Supply voltage	1.4		2.8	V
T_A	Operating Temperature	−40		125	°C

1. Unless otherwise stated, over operating free-air temperature range.

5.3 Electrical Sensitivity

SYMBOL[1]	CONDITIONS	VALUE	UNIT
$V_{ESD(HBM)}$	Human Body Mode (HBM), per ANSI/ESDA/JEDEC JS-001	±5000	V
$V_{ESD(MM)}$	Machine Mode (MM), per JEDEC-STD Classification	300	V

1. Unless otherwise noted, the specifications in the above table apply within the atmospheric temperature range.

5.4 Electrical Characteristics

Electrical characteristics of devices at T_A = +25°C and V+ = 1.4 V to 2.8 V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
T_{RANGE}	Operating Temperature Range		−40		125	°C
T_{ERROR}	Accuracy (Temperature Error)	−10°C to 100°C，V+ = 1.8V	2	0	2	°C
		−40°C to 125°C, V+ = 1.8V	−3		3	°C
		Vs Supply	0.5	±0.2	0.5	°C/V
	Resolution			1		°C
				8		bits
	Conversion Modes	CR1 = 0, CR0 = 0		0.25		Conv/s
		CR1 = 0, CR0 = 1		1		
		CR1 = 1, CR0 = 0		4		
		CR1 = 1, CR0 = 1		8		
	Conversion Time			26	35	ms
t_{TIME_OUT}	Timeout Time			30	40	ms
f_{COMM}	Communication Frequency		0.001		2.75	MHz
V_+	Power Supply Voltage		1.4		2.8	V
I_Q	Average Conversion Current	Bus free, CR1 = 0, CR0 = 0		1.5	3	μA
		Bus actived, fSCL = 400kHz		15		
		Bus actived, fSCL = 3.4MHz		85		
I_{SD}	Shutdown Current	Bus free, V+ = 1.8V		0.5	3	μA
		Bus actived, fSCL = 400kHz		10		
		Bus actived, fSCL = 3.4MHz		80		

6 Functional Description

6.1 Device Feature Description

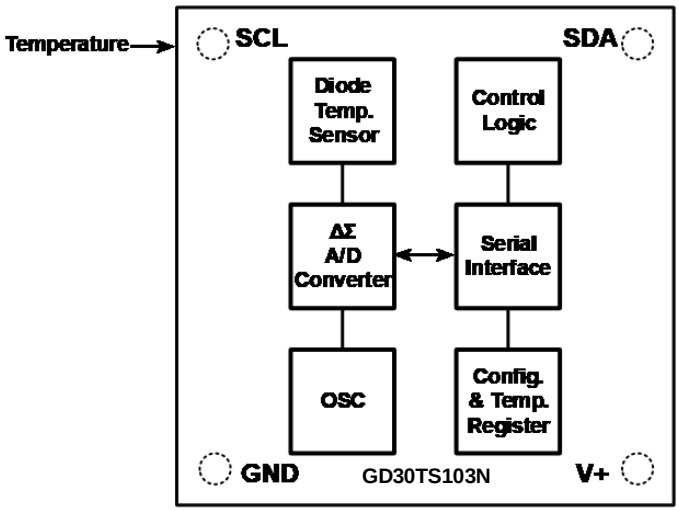


Figure 1. Block diagram of GD30TS103N series internal modules

6.1.1 Continuous Conversion Mode

Write the M1 bit in the GD30TS103N series configuration register to 1, and the chip will be in continuous conversion mode. By changing the CR1 and CR0 bits in the configuration register, the temperature measurement rate of the GD30TS103N series in this mode can be configured to 0.25Hz, 1Hz, 4Hz, or 8Hz. After each conversion, the GD30TS103N series will power down and wait for a fixed delay set by CR1 and CR0 bits before the next conversion, as shown in Figure 2. Table 1 shows the configuration of the CR1 and CR0 bits.

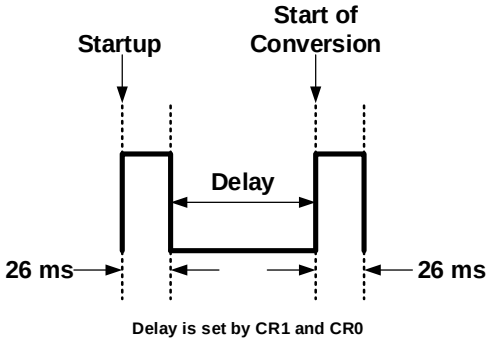


Figure 2. Schematic Diagram of Continuous Conversion

Table 1. Conversion Rate Settings

CR1	CR0	Conversion rate
0	0	0.25Hz (default)
0	1	1Hz
1	0	4Hz
1	1	8Hz

6.1.2 Shutdown Mode

Setting the M1 and M0 bits in the GD30TS103N series configuration register to 00, and the chip will enter shutdown mode after completing the conversion. In this mode, all circuits except the serial interface stop working, thus reducing the current of the GD30TS103N series to below 0.5μA (typical value).

6.1.3 Single Shot Mode (One-Shot Mode)

When the GD30TS103N series is in off mode, write the M1 and M0 bits of the configuration register to 01 to enable single shot conversion. During the conversion, the M1 and M0 bits are read as 01. After the single conversion is complete, the chip will return to the critical off state, with the M1 and M0 bits reading 00. When continuous temperature measurement is not required, this function can greatly reduce the chip power consumption.

Since the GD30TS103N series only takes 26ms (typical value) for a single temperature measurement, a higher temperature measurement rate can be achieved through this mode. By continuously configuring the GD30TS103N series in One-Shot mode, 30 or more temperature measurements per second can be achieved.

6.1.4 Temperature Monitoring Function

GD30TS103N series has temperature monitoring function. When the LC bit in the configuration register is written to 0, the chip goes into comparison mode. At this time, if the temperature measurement result is greater than or equal to the temperature threshold in the T_{HIGH} register, the high temperature marker bit FH in the configuration register will be set to 1, otherwise the bit will be set to 0; If it is less than or equal to the threshold value in the T_{LOW} register, the low temperature marker FL will be set to 1, otherwise the bit will be set to 0.

When the LC bit in the configuration register is written to 1, the chip enters interrupt mode. At this time, the FH and FL bits are set to 1 under the same conditions as in comparison mode. But after being set to 1, the FH and FL bits will remain in this state until the host sends a read command to the configuration register, and the FH and FL bits will be reset to 0.

The above process is shown in Figure 3. The default values for the above bits at power-on reset are FH=0, FL=0, LC=0.

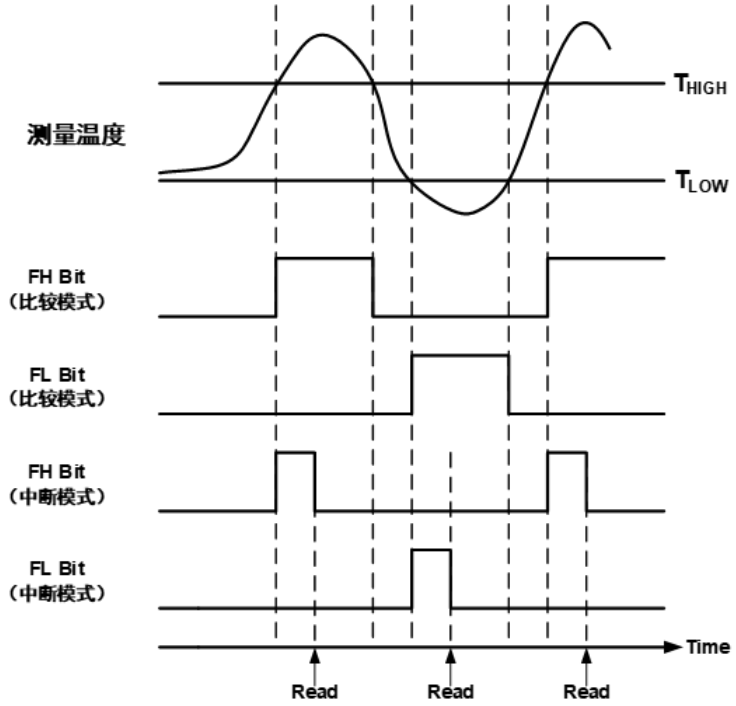


Figure 3. Schematic diagram of temperature monitoring function

6.2 Serial Interface

6.2.1 Bus Overview

The GD30TS103N series is compatible with SMBus and I²C interfaces. In the SMBus protocol, the device that initiates the transmission is called the host, and the device controlled by the host is called the slave. The bus must be controlled by the host, which produces the Serial clock Line (SCL), controls the bus access and produces the START and STOP signals. To address a specific slave, the master pulls the data line (SDA) from the high to the low level when the SCL is high to produce the START signal. All slaves on the bus receive 8bits of the slave address on the rising edge of the clock, where the last bit indicates whether to perform a read or write operation. In the ninth clock, the slave being addressed responds to the host by generating the Acknowledge bit and pulling the SDA down. Thereafter the data transmission begins and sends an Ack bit after every eight clocks. The SDA must remain stable during the data transfer period when the SCL is at high power level. Because the SCL is on high power, any change in the SDA will be treated as a START or STOP signal.

After the data transfer is complete, the master generates a STOP signal to end the communication by pulling the SDA from low to high level during high SCL.

6.2.2 Serial Bus Address

In order to communicate with the GD30TS103N series, the host must first address the specified slave through the slave address byte. The slave address byte consists of seven address bits and a flag bit that indicates the execution of a read or write operation. GD30TS103N can provide 8 different address versions, as shown in Table 2. These addresses can be used as indicators of measuring positions or temperature zones.

Table 2. Mapping between GD30TS103N slave address and chip number

PRODUCT NUMBER	TWO-WIRE ADDRESS	TEMPERATURE AREA
GD30TS103NA	1110000	Zone1
GD30TS103NB	1110001	Zone2
GD30TS103NC	1110010	Zone3
GD30TS103ND	1110011	Zone4
GD30TS103NE	1110100	Zone5
GD30TS103NF	1110101	Zone6
GD30TS103NG	1110110	Zone7
GD30TS103NH	1110111	Zone8

6.2.3 Writing and Reading Operation

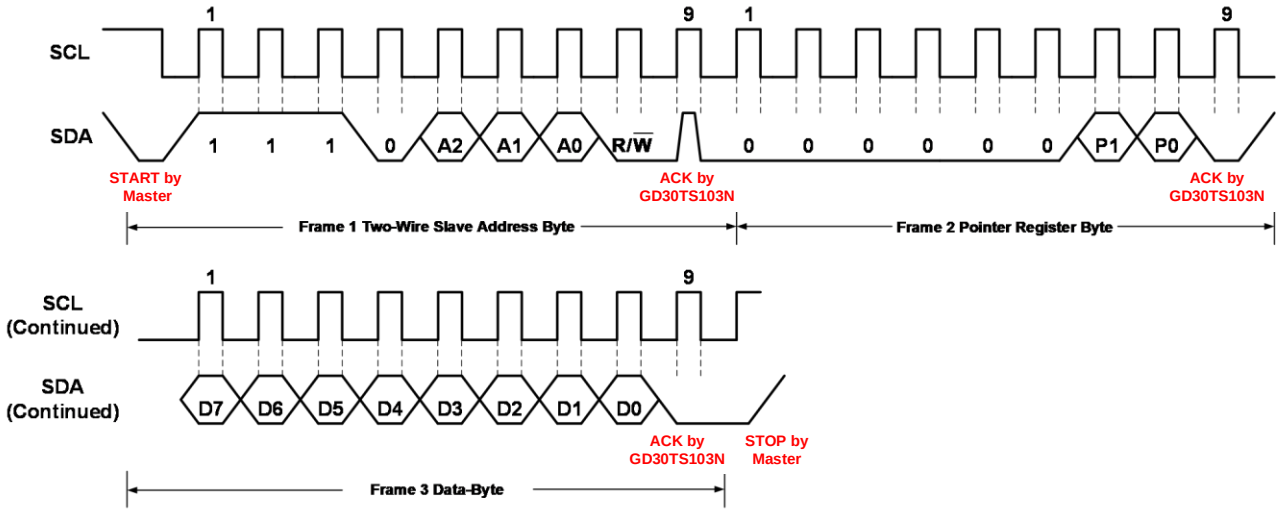


Figure 4. Two-wire Write Command Timing Diagram

NOTE: The values of A2 ~ A0 are shown in Table 2.

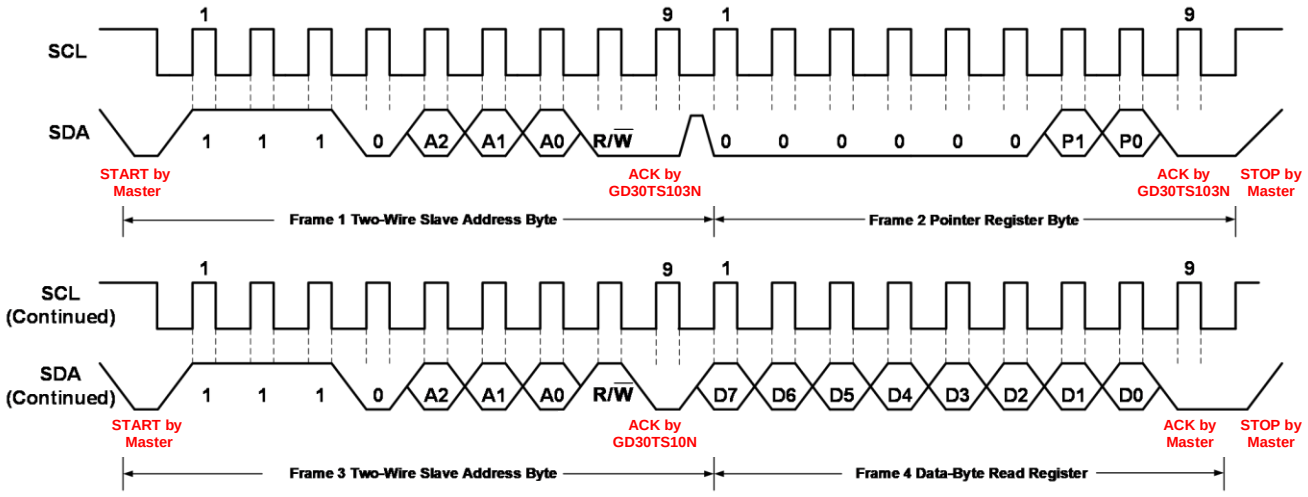


Figure 5. Two-wire Read Command Timing Diagram

NOTE: The values of A2 ~ A0 are shown in Table 2.

When writing data to the GD30TS103N series, after sending the slave address byte, the corresponding pointer register byte needs to be sent to access the specific register in the GD30TS103N series. Each write to the GD30TS103N series requires the pointer register byte to be sent.

When reading data from the GD30TS103N series, after sending the slave address byte, you also need to send the corresponding pointer register byte. Unlike the write operation, if the data needs to be read from the same register repeatedly, the pointer register byte does not need to be sent each time, the chip will automatically read the data from the previous pointer register; If the data needs to be read from a new register, it needs to rewrite and send a low slave address byte, then send a new pointer register byte, and then the host generates a START signal and sends a high slave address byte to start the read command.

It should be noted that the register byte should be sent first to MSB, then to LSB. Figure 4 and Figure 5 give a schematic of the above read and write operations, both using GD30TS103N as an example.

6.2.4 Multiple Device Access

The GD30TS103N series supports multi-chip access (MDA), allowing the host to communicate with multiple GD30TS103N series chips at different addresses on the same bus at the same time. The MDA command consists of an MDA read address (01h) and an MDA write address (00h), by which the chip acknowledges the MDA address and responds to the command. In order for the MDA command to execute properly, different numbered products from the single series of GD30TS103N must be used in the system, as shown in Table 2 and 错误!未找到引用源。. It must be noted that when MDA functions are used, they cannot be used across series, such as GD30TS103NA and GD30TS103NB cannot be mounted on the same bus at the same time.

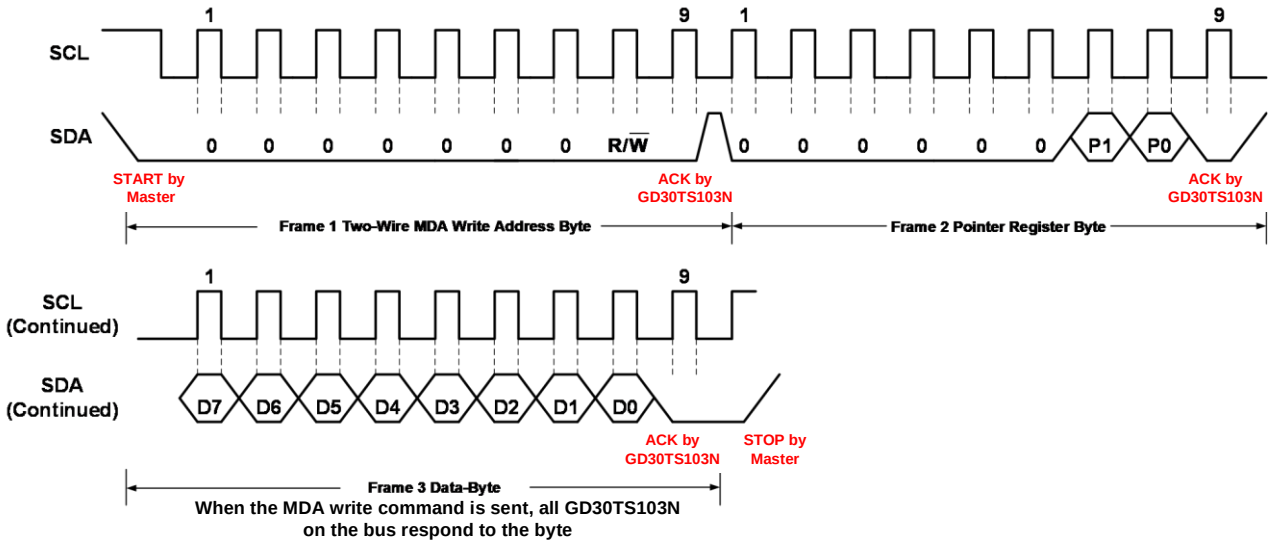
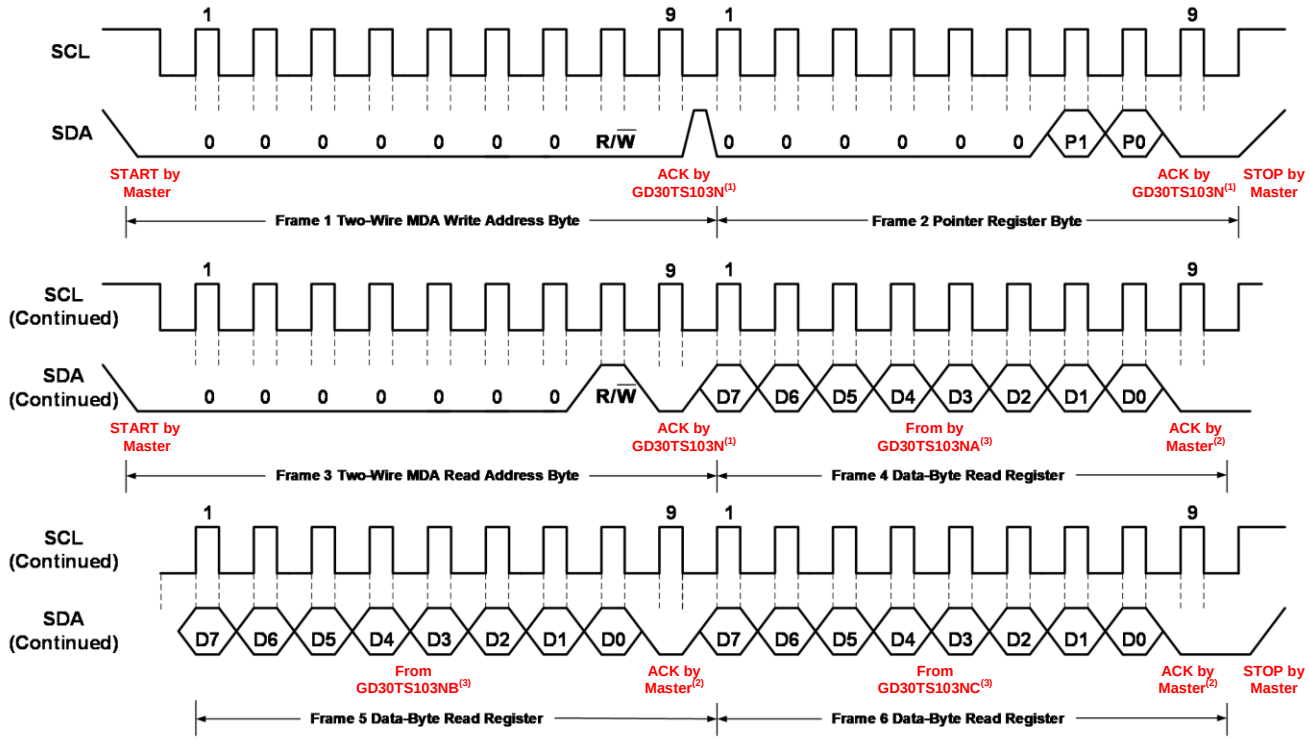


Figure 6. Timing diagram of two-wire MDA writing commands

When using the MDA write command, the host should send the MDA write address first, and then send the pointer address of the register that needs to be accessed. After sending the pointer address, all GD30TS103N series chips on the bus will answer to this. The host will continue to send the byte that needs to be written to the appropriate register, and the multiple GD30TS103N series chips on the bus will store and answer the byte. The above process is shown in Figure 6.

When the MDA read command is used, the host must first send the MDA write address and the pointer address of the register to be accessed. After that, the host continues to send the MDA read address. The GD30TS103N series chip on the bus returns the bytes to be read in turn. The host must send an ACK signal for each byte read. If the host does not respond to one of the returned bytes, all subsequent slaves will stop returning data. The above process is shown in Figure 7, with GD30TS103NA, GD30TS103NB, and GD30TS103NC mounted on the bus at the same time.



(1) All GD30TS103N on the bus respond to the byte.

(2) The host must respond after reading each byte to achieve reading of all GD30TS103N on the bus.

(3) As shown in this figure, three GD30TS103N are mounted, and up to eight can be mounted simultaneously.

Figure 7. Timing diagram of two-wire MDA command reading

If the bus contains an incomplete GD30TS103N-series address sequence, the host must send all the required bytes for the free chip address to ensure normal MDA read operations. For example, if GD30TS103NA, GD30TS103NB, and GD30TS103ND are mounted on the bus, the host must first send the MDA read address, which must be followed by four read register data bytes, each of which must be answered by the host to complete the MDA read operation. In the third byte where GD30TS103NC is originally to be read, SDA should remain 1 in that data byte since GD30TS103NC is not mounted on the main line.

6.2.5 Global Call Reset (General Call Reset)

The GD30TS103N series responds to the two-wire global response reset command 00h and executes the command in the second byte after it. If the second byte is 06h, the internal registers of the GD30TS103N series will all be reset to their power-on initial values. If the second byte is any other value, the GD30TS103N series will not respond to it.

6.2.6 High-Speed Mode

The GD30TS103N series supports bus operation at frequencies higher than 400kHz. The host issues a high speed mode command (00001xxxb) after the START signal to switch the bus to high speed mode. The GD30TS103N series does not answer the byte, but switches the input filter on its internal SDA and SCL pins and the output filter on the SDA pins to work in high speed mode, enabling the bus to transmit at a maximum frequency of 2.75MHz. When the high speed mode command is issued, the host will continue to send the slave address to initiate data transmission. The bus will continue to operate in high speed mode until a STOP signal appears on the bus. After receiving the STOP signal, the GD30TS103N series will switch to fast mode.

When using the high-speed mode for communication, it is necessary to pay attention to the size of the pull-up resistance on the SDA, SCL pins. If you need to communicate at a higher frequency, the size of the mounted pull-up resistance should be reduced accordingly. For a 5kΩ pull-up resistor, the upper limit of the communication frequency is 1.2MHz (typical value); To achieve a communication frequency of 2.75MHz, the pull-up resistor should have a resistance of less than 1.5 kΩ (typical value).

6.2.7 Time-Out Function

If the SCL remains low at 30ms (typical value) between the START and STOP signals, the GD30TS103N series will reset its serial interface. That is, if the SCL is pulled down more than 30ms, the GD30TS103N series releases the SDA and waits for the START signal. To avoid activating the timeout function, the SCL should operate at a frequency greater than 1kHz.

6.3 Register Descriptions

6.3.1 Pointer Register

Figure 8 shows the internal register structure of the GD30TS103N series. One of the 8-bit pointer registers is used to address specific data registers. The pointer register uses two LSBS to identify which data register should respond to read or write commands. Table 3 gives the pointer addresses of the available registers in the GD30TS103N series. The P1/P0 power-on reset value is 00. The GD30TS103N series is powered on by default to read the temperature register. Table 4 shows the configuration of each bit of the pointer register byte. During command writing, P2 through P7 must always be 0.

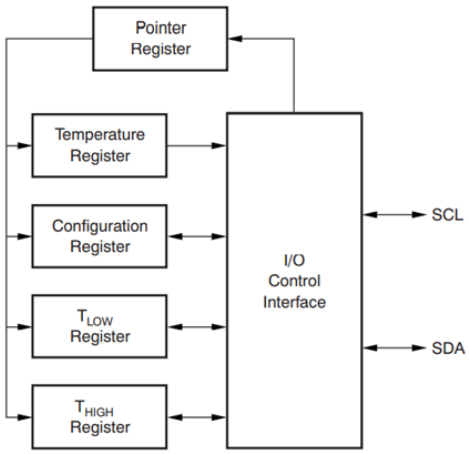


Figure 8. Internal Register Structure

Table 3. Pointer Address

P1	P0	REGISTER
0	0	Temperature Register (Read Only)
0	1	Configuration Register (Read/Write)
1	0	T_{LOW} Register (Read/Write)
1	1	T_{HIGH} Register (Read/Write)

Table 4. Pointer Register Byte

P7	P6	P5	P4	P3	P2	P1	P0
0	0	0	0	0	0	Register Bits	

6.3.2 Temperature Register

The Temperature Register of the GD30TS103N series are read-only registers, which are used to store the latest temperature measurement results, where the negative temperature is expressed in the form of binary complement. After power-on or reset, the temperature register reads 0°C by default.

The temperature register of the GD30TS103N is an 8-bit read only register, 1LSB=1°C. The specific configuration and temperature data format are shown in Table 5, Table 6, 错误!未找到引用源。.

Table 5. Format of GD30TS103N series temperature data

Temperature (°C)	GD30TS103N	
	DIGITAL OUTPUT	HEXADECIMAL
128	01111111	7F
127.875		
127	01111111	7F
100	01100100	64
80	01010000	50
75	01001011	4B
50	00110010	32
25	00011001	19
0.25		
0	00000000	00
0.25		
-1	11111111	FF
-25	11100111	E7
-55	11001001	C9

Table 6. GD30TS103N temperature register

D7	D6	D5	D4	D3	D2	D1	D0
T7	T6	T5	T4	T3	T2	T1	T0

6.3.3 Temperature Limit Register

The T_{HIGH} and T_{LOW} registers are used to store the temperature limit threshold of the GD30TS103N series temperature monitoring function. At the end of each temperature measurement, the GD30TS103N series compares the temperature measurement results to the temperature limit threshold. The temperature limit registers in the GD30TS103N series are all 8-bit read/write registers, where 1LSB=1°C, as shown in Table 7 and Table 8.

T_{HIGH} = +60°C； T_{LOW} = -10°C.

Table 7. T_{HIGH} registers in the GD30TS103N series

D7	D6	D5	D4	D3	D2	D1	D0
H7	H6	H5	H4	H3	H2	H1	H0

Table 8. T_{LOW} registers in the GD30TS103N series

D7	D6	D5	D4	D3	D2	D1	D0
L7	L6	L5	L4	L3	L2	L1	L0

6.3.4 Configuration Register

The Configuration Register of the GD30TS100 and GD30TS101 is an 8-bit read/write register used to store bits that control the operational modes of the temperature sensor. Table 9 list the format and power-up and reset values of the configuration register.

Table 9. Configuration Register High Byte

BIT	FIELD	DEFAULT	DESCRIPTION
7	ID (R)	0	**BLANK**
6	CR1 (R/W)	0	**Continuous conversion rate selection bit**
5	CR0 (R/W)	0	**Default**: **00 =** 0.25Hz, see Table 1.
4	FH (R)	0	**High temperature marker bit** **1** = Temperature measured above T **0** = Temperature measured below T
3	FL (R)	0	**Low temperature marker bit** **1** = The temperature is measured below T **0** = Temperature measured above T
2	LC (R/W)	0	**Temperature monitoring mode selection bit** **1**= Interrupt mode **0**= Compare mode
1	M1 (R/W)	1	**Chip function mode select bit** **00** = Off mode **01** = Single Switch mode **10, 11** = Continuous conversion mode
0	M0 (R/W)	0	

7 Application Information

The above contents are the precautions for the GD30TS103N recommended by GigaDevice in practical applications. Customers are responsible for determining suitability of components for their purposes based on their own usage needs and application scenarios. Customers should test and verify their design implementation to confirm system functionality and avoid losses.

As a low power chip, the GD30TS103N series can further reduce the impact of external noise by adding an RC filter to its V+ pin, as shown in Figure 9, where R_F must$_F$ be less than 5kΩ and C_F must$_F$ be greater than 10nF.

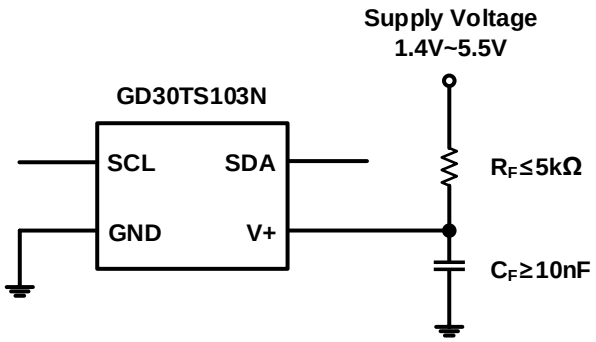


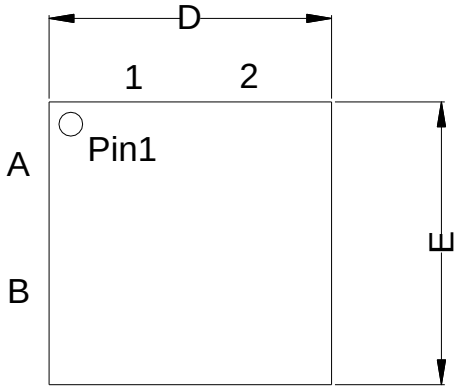
Figure 9. Noise Reduction Techniques

Place the device in close proximity to the heat source that must be monitored, with a proper layout for good thermal coupling. This placement ensures that temperature changes are captured within the shortest possible time interval. To maintain accuracy in applications that require air or surface temperature measurement, take care to isolate the package and leads from ambient air temperature. A thermally-conductive adhesive is helpful in achieving accurate surface temperature measurement.

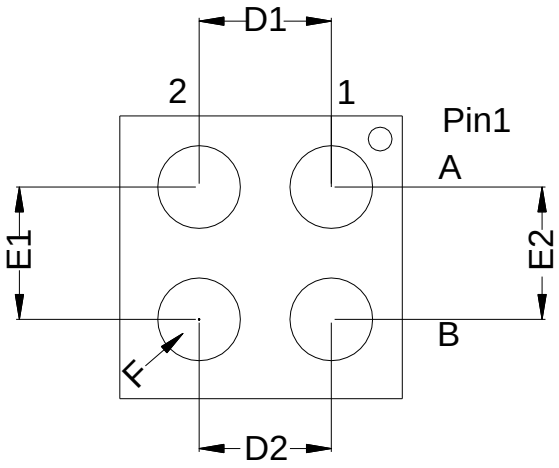
8 Package Information

8.1 Outline Dimensions

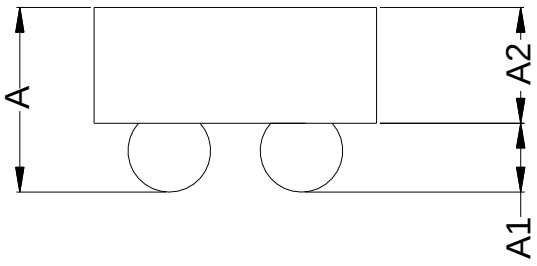
WLCSP-4 Package Outline



Top View



Bottom View



Side View

NOTES:

1. All dimensions are in millimeters.
2. Package dimensions does not include mold flash, protrusions, or gate burrs.
3. Refer to the *Table 10. WLCSP(4) dimensions*(mm).

Table 10. WLCSP(4) dimensions(mm)

SYMBOL	MIN	NOM	MAX
A	0.5235	0.556	0.5885
A1	0.186	0.206	0.226
A2	0.3375	0.350	0.3625
D	0.830	0.855	0.880
E	0.830	0.855	0.880
F	0.240	0.260	0.280
D1		0.400	
D2		0.400	
E1		0.400	
E2		0.400	

9 Ordering Information

Ordering Code	Package Type	ECO Plan	Packing Type	MOQ	OP Temp(°C)
GD30TS103NJYTR-I	WLCSP-4	Green	Tape & Reel	4000	−40°C to +125°C

10 Revision History

REVISION NUMBER	DESCRIPTION	DATE
1.0	Initial release and device details	2024
1.1	Delete GD30TS103SJYTR-I	2024

Important Notice

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