H-Bridge Motor Driver with nFAULT Function

1 Features

- Wide 4.5V to 40V Supply Voltage
- Output Current Capability: 6A Peak and 4A Continuous
- FAULT Status Indication Function
- Low $R_{DS(ON)}$ Integrated MOSFET:
  - RDS(on) (HS+LS): 200mΩ
- Separate Logic and Motor Power Supply Pins
- Standard PWM Interface (IN1/IN2)
- Low Power Sleep Mode, Maximum Sleep Current 1μA
- Small Package and Footprint
  - 8 pin SOP (With Thermal Pad)
- Protection Features
  - Over Current Protection (OCP)
  - Thermal Shutdown (TSD)
  - Under Voltage Lock-Out (UVLO)
  - MOSFET Shoot-Through Prevention

2 Applications

- Home Appliances
- DC Brush Motors
- Printers
- Industrial Automation
- Sweeping Robot

3 Description

The GD30DR3002 is an H-bridge driver, and is designed to drive one DC brush motor or other inductive loads. The H-bridge is composed of four high voltage N-Channel MOSFETs that can control motors bidirectionally with up to 6A peak current. Two logic inputs are provided to control the H-bridge driver, and therefore control the speed and direction of the DC motor with externally applied PWM control signals. Setting both inputs low enters a low power sleep mode. At the same time, the device also has a fault status indication function.

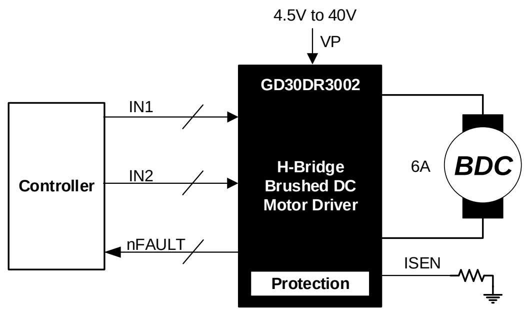
The GD30DR3002 device features integrated current regulation, based on the internal reference voltage and the voltage on the ISEN pin, which is proportional to motor current through an external sense resistor. The ability to limit current to a known level can significantly reduce the system power requirements and bulk capacitance needed to maintain stable voltage, especially for motor startup and stall conditions.

The device internal protection includes undervoltage (UVLO), overcurrent(OCP), and overtemperature(TSD). When the fault condition is removed, the device automatically resumes normal operation.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
GD30DR3002	EP-SOP (8)	4.90 mm × 3.90 mm

1. For packaging details, see *Package Information* section.



Simplified Application Schematic

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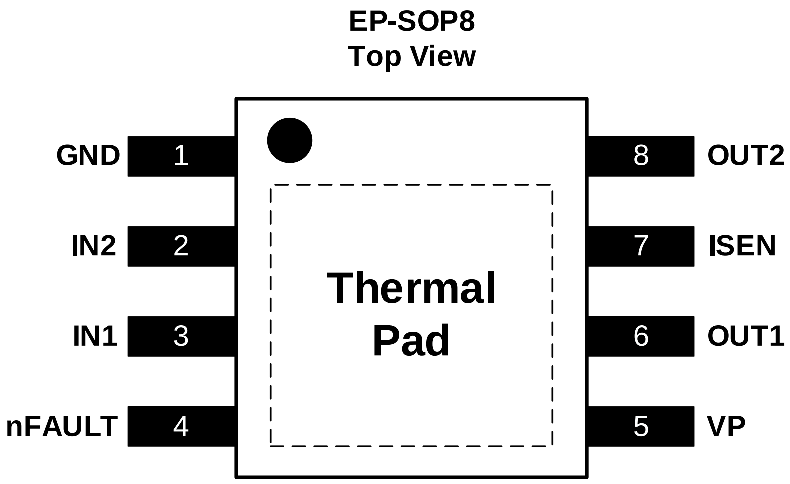
4 Device Overview

4.1 Pinout and Pin Assignment



4.2 Pin Description

PIN		PIN TYPE1	FUNCTION
NAME	NUM		
GND	1	P	Device logic ground, connect to board ground.
IN2	2	I	Logic input, control signal of H-bridge, internal pulldown. See Table 1.
IN1	3	I	Logic input, control signal of H-bridge, internal pulldown. See Table 1.
nFAULT	4	O	Open Drain output, connect by a pull up resistor, it will be pull down when UVLO, TSD, or OCP fault.
VP	5	P	Power supply, connect a 0.1μF bypass capacitor to ground, as well as sufficient bulk capacitance, rated for the VP voltage.
OUT1	6	O	H-bridge output, connect to the DC motor or other inductive load.
ISEN	7	P	Current path to ground, connect a sense resistor to ground to set the current regulation or directly to ground when not using regulation.
OUT2	8	O	H-bridge output, connect to the DC motor or other inductive load.
Thermal pad	Thermal pad	P	Power ground, connect to board ground, use large ground plane for good thermal dissipation, and multiple nearby vias connecting those planes, see *Layout Guidelines and Example*.

1. I = input, O = output, P = power, G = ground.

5 Parameter Information

5.1 Absolute Maximum Ratings

Exceeding the operating temperature range (unless otherwise noted)[1,2]

SYMBOL	PARAMETER	MIN	MAX	UNIT
VP	Motor power supply voltage	−0.3	45	V
nFAULT	FAULT output	−0.3	6	V
V_{INx}	Control input pin voltage	−0.3	6	V
V_{OUTx}	H-bridge output drive	−1.0	VP + 0.7	V
V_{ISEN}	Current path to ground[3]	−0.7	1.0	V
I_{LIM}	Internal current limit	0	6	A
T_J	Operating junction temperature	−40	150	°C
T_{stg}	Storage temperature	−65	150	°C

1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. All voltage values are with respect to network ground terminal.
3. Transients of ±1V for less than 25ns are acceptable.

5.2 Recommended Operation Conditions

SYMBOL[1,2]	PARAMETER	MIN	TYP	MAX	UNIT
VP	Motor power supply voltage	4.5		40	V
nFAULT	FAULT output	0.3		5.5	V
V_{INx}	Control input pin voltage	0		5.5	V
I_{OUTx}	Continuous motor drive output current	0		4	A
I_{PEAK}	Peak output current	0		6	A
f_{pwm}	Externally applied PWM frequency[2]	0		200	kHz
V_{ISEN}	Current path to ground	−0.7		1.0	V
T_A	Operating ambient temperature	−40		125	°C

1. The device is not guaranteed to function outside of its operating conditions.
2. At an input frequency of 100KHz/200KHz, the maximum supported duty cycle is 95%/92%.
3.

5. Application Information section for further information.

5.3 Electrical Sensitivity

SYMBOL	CONDITIONS	VALUE	UNIT
$V_{ESD(HBM)}$	Human-body model (HBM), ANSI/ESDA/JEDEC JS-001-2017[1]	±4000	V
$V_{ESD(CDM)}$	Charge-device model (CDM), ANSI/ESDA/JEDEC JS-002-2022[2]	±1000	V

1. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
2. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.4 Electrical Characteristics

T_A = 25°C (unless otherwise noted).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY(VP)						
VP	VP operating voltage		4.5		40	V
I_{VP}	VP operating supply current	VP = 24 V		2	4	mA
I_{VPQ}	VP standby mode current	VP = 24 V			1	μA
t_{WAKE}	Turn-on time	VP > V_{UVLO}, IN1 or IN2 high		40	50	μs
t_{SLEEP}	Turn-off delay time	IN1=IN2=0		1		ms
LOGIC-LEVEL INPUTS(IN1, IN2)						
V_{IL}	Input low voltage				0.5	V
V_{IH}	Input high voltage		1.5			V
V_{HYS}	Input logic hysteresis			500		mV
I_{IL}	Input low current	V_{INx} = 0	−1		1	μA
I_{IH}	Input high current	V_{INx} = 3.3V		30	50	μA
R_{PD}	Pulldown resistance			100		kΩ
t_{PD}	Propagation delay	IN1/IN2 transition to OUT1/OUT2 transition		300		ns
MOTOR DRIVER OUTPUTS(OUT1, OUT2)						
$R_{DS(ON)\_HS}$	High side MOSFET R_{DSON}	VP = 24V, I = 1A, T_A = 25°C		100		mΩ
$R_{DS(ON)\_LS}$	Low side MOSFET R_{DSON}	VP = 24V, I = 1A, T_A = 25°C		100		mΩ
V_D	Body diode forward voltage	I_{OUT} = 1A, T_A = 25°C		0.8	1	V
t_{DT}	Output drive dead time			200		ns
t_{RISE}	Output rise time	OUTx rising from 10% to 90%		170		ns
t_{FALL}	Output fall time	OUTx falling from 10% to 90%		170		ns
CURRENT REGULATION						
V_{TRIP}	ISEN voltage for current chopping		0.32	0.35	0.38	V
t_{OFF}	Fixed PWM off-time			25		μs
t_{BLANK}	PWM blanking time			2		μs
PROTECTION CIRCUITS						
V_{UVLO}	VP undervoltage lockout	VP falling	4.0	4.2	4.3	V
V_{UVLO_HYS}	VP undervoltage hysteresis	Rising to falling threshold		150		mV
t_{UVLO_DEG}	VP undervoltage deglitch time	VP falling		10		μs
I_{OCP}	Over current protection		6.0	7.0		A
t_{OCP_DEG}	Over current deglitch time			1.5		μs
t_{RETRY}	OCP retry time			3		ms

Electrical Characteristics(continued)

T_A = 25°C (unless otherwise noted).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
T_{TSD}	Thermal shutdown temperature			155		°C
T_{HYS}	Thermal shutdown hysteresis			35		°C
nFAULT OPEN DRAIN OUTPUT(nFAULT)						
V_{OL}	Output Low Voltage	I_O = 5mA			0.5	V
I_{OH}	Output high leakage current	V_O=3.3V			1	µA

5.5 Timing Requirements

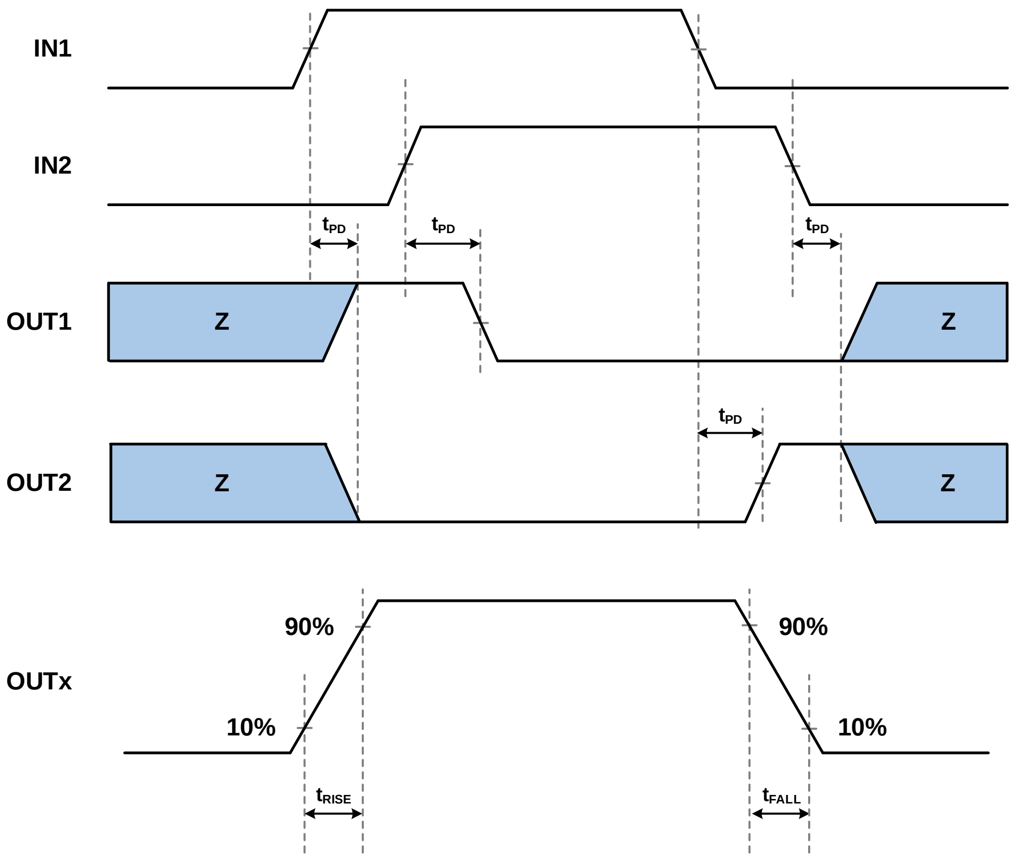


Figure 1. Input and Output Timing for GD30DR3002

5.6 Typical Characteristics

T_A = 25°C, unless otherwise noted.

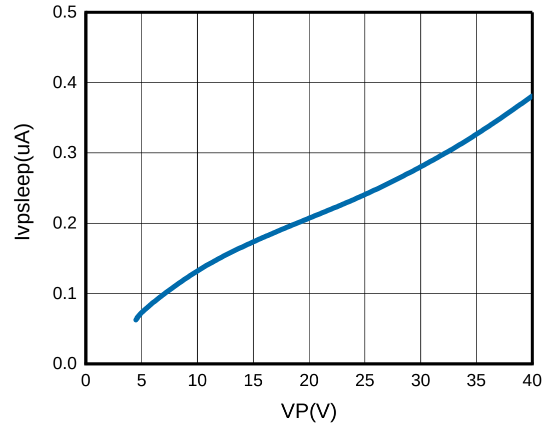


Figure 2. Sleep Current vs. Input Voltage

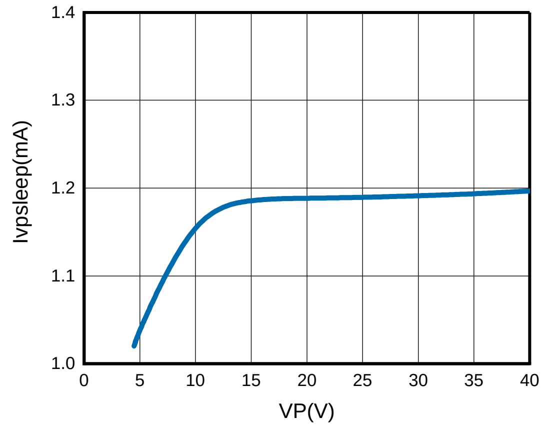


Figure 3. Active Current vs. Input Voltage

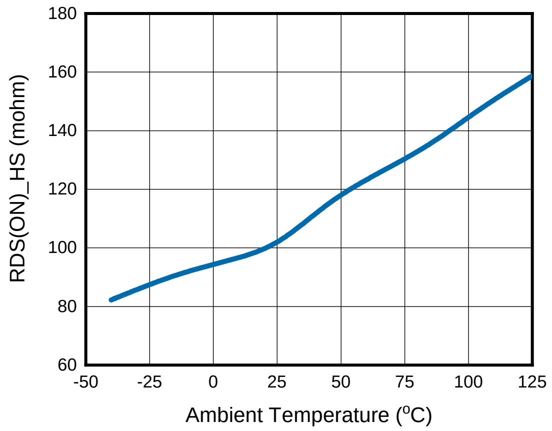


Figure 4. High-Side RDS(ON) vs. Temperature

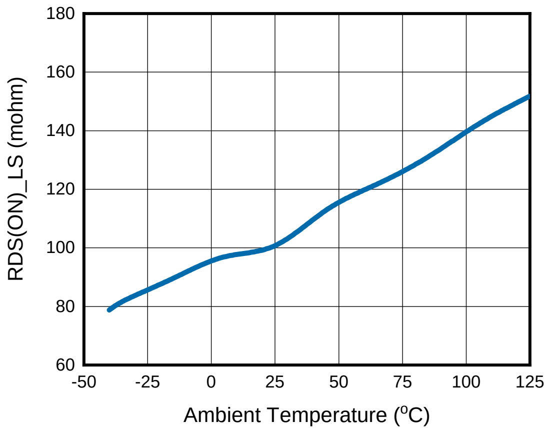


Figure 5. Low-Side RDS(ON) vs. Temperature

6 Functional Description

6.1 Block Diagram

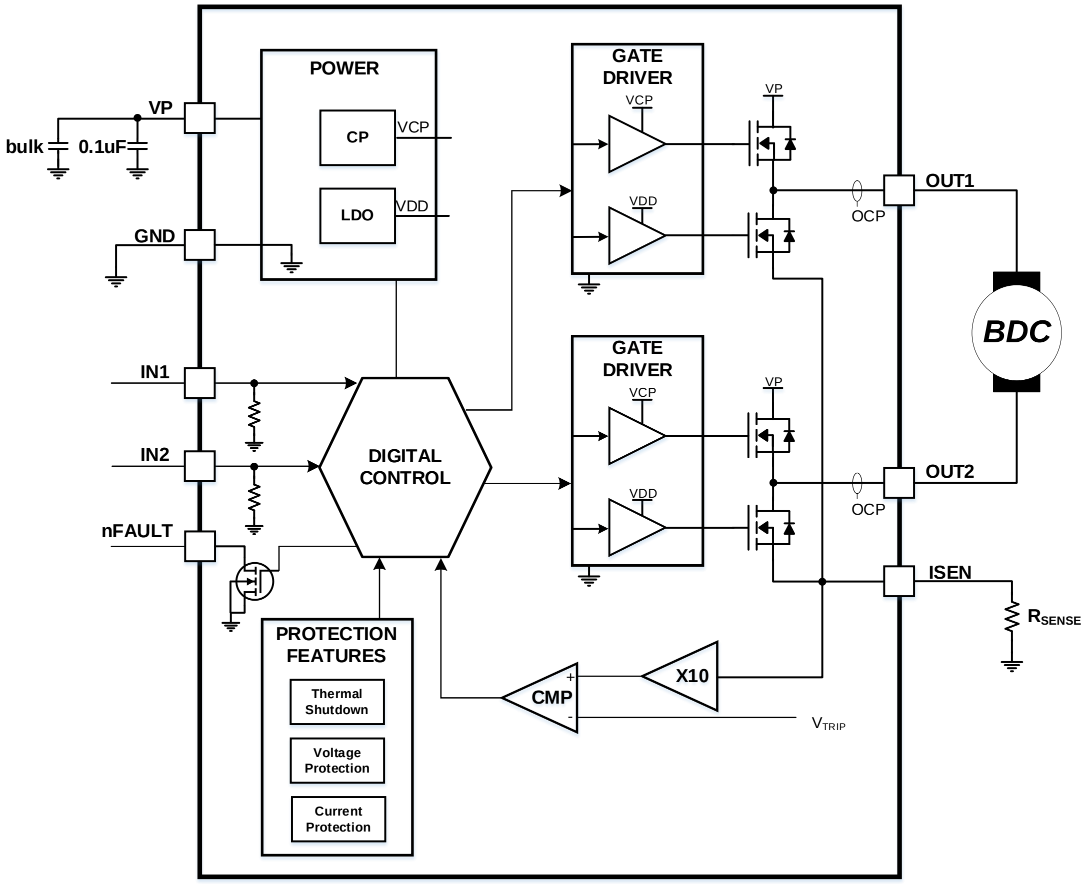


Figure 6. GD30DR3002 Functional Block Diagram

6.2 Operation

The GD30DR3002 serves as an H-bridge driver capable of powering a single DC motor or other devices, such as solenoids. It regulates its outputs through a PWM interface (IN1/IN2) up to 200kHz. When both logic inputs are low for a 1ms period, the device will be set into standby mode and consume less power. Protection features such as OCP, OTSD and UVLO are implemented to prevent the device and system from fault and damage. At the same time, the device also has a fault status indication function.

6.2.1 PWM Mode

In GD30DR3002, the device operates in PWM mode. H-bridge in PWM mode supports four output states: coast (Hi-Z), forward, reverse and brake. They are controlled by IN1/IN2 according to Table 1. The inputs can be set to static voltage for 100% duty cycle drive, or PWM for variable motor speed. When using PWM, it typically works best to switch between driving and braking.

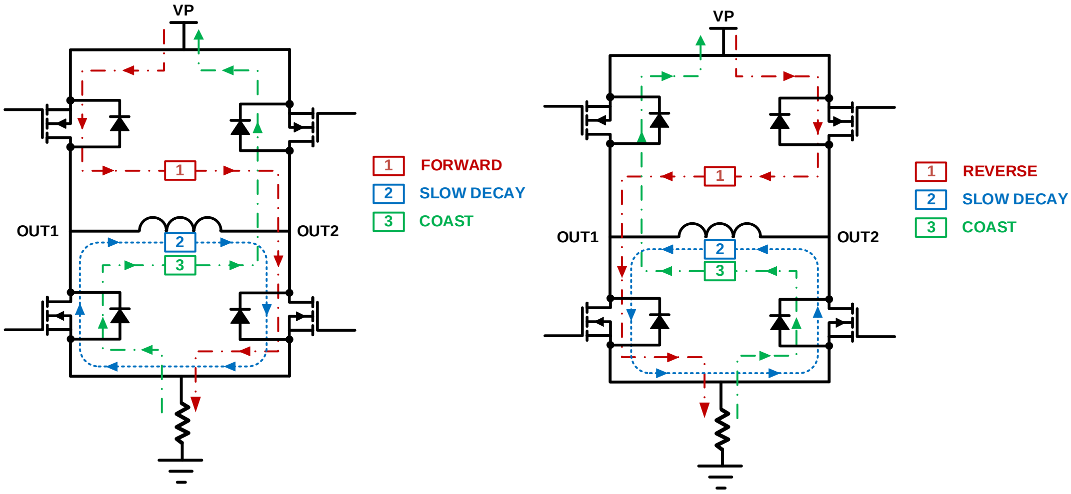


Figure 7. The Driver Outputs and Current Path

Table 1 shows the logic for the GD30DR3002 device.

Table 1. H-Bridge Control

IN1	IN2	OUT1	OUT2	FUNCTION (DC MOTOR)
0	0	Z	Z	Coast
0	1	L	H	Reverse
1	0	H	L	Forward
1	1	L	L	Brake

6.2.2 Dead Time

An internal handshaking scheme is used to prevent shoot-through between the high side and low side MOSFETs. A typical dead time of 200ns is inserted when transitioning between MOSFETs in each half-bridge.

6.2.3 Current Regulation

The output current is regulated at a limit set by an internal reference voltage V_{TRIP} and the resistor R_{ISEN} connected from ISEN to ground, according to the Equation(1):

$$I_{TRIP} = \frac{V_{TRIP}(V)}{R_{REF}(\Omega)} = \frac{0.35(V)}{R_{SEN}(\Omega)}(A) \quad (1)$$

For example, if R_{ISEN}=0.2Ω, the GD30DR3002 will limit motor current limit to 1.75A no matter how much load torque is applied.

Usually I_{TRIP} is set above the normal motor operating current, and high enough to achieve adequate spin-up time, and low enough to constrain current to a desired level.

If ISEN is connected to ground directly, the current regulation function is disabled. VREF should still be applied to a value which could provide high noise margin. The output current could go up to 6A for a few hundred milli-second. Over current protection and over temperature protection may be triggered to protect the IC and system.

6.2.4 Mixed current decay

When current regulation is triggered, IC will enter a fixed time PWM off cycle to re-circulate the current. By default, the device enforces slow current decay by enabling both low-side MOSFETs for the fixed off time (t_{OFF}, 25μs typical).

A mixed current decay mode is implemented as an option only in GD30DR3002. In this mode, when current regulation is triggered, the driver outputs are switched to opposite polarity (High to Low, or Low to High) for the first half t_{OFF}. In the latter half of t_{OFF}, the driver is switched back to slow-decay mode. Mixed current decay are explained in Figure 8.

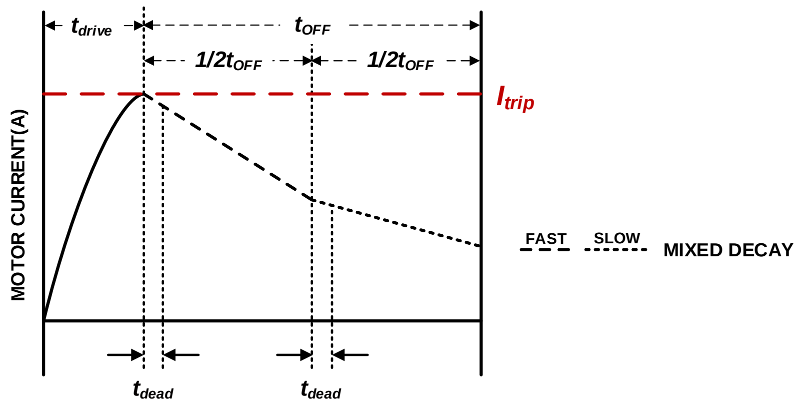


Figure 8. Mixed Current Decay

6.2.5 Protection Circuits

The GD30DR3002 device is fully protected against VP undervoltage, overcurrent, and overtemperature events. When the device is in a protected state, nFAULT is driven low. When the fault condition is removed, nFAULT becomes a high-impedance state.

6.2.5.1 Power Supply undervoltage lockout(UVLO)

At any time if the voltage on the power supply VP falls below the UVLO threshold, all the internal MOSFETs in the H-bridge will be disabled. Normal operation will resume when VP rises above UVLO threshold.

6.2.5.2 Overcurrent protection (OCP)

The individual currents go through the MOSFETs (high-side and low-side) are monitored cycle by cycle. In case any current is over the over-current limit, all the MOSFETs are disabled and the internal power supply will be shutdown. The recycle of the PWM control will be retried after a delay time of 3ms and normal operation will be resumed if the OCP events are cleared

6.2.5.3 Thermal shutdown (TSD)

If the die temperature exceeds the trip point of the thermal shutdown limit (T_{OTSD}, typical 150°C), all the MOSFETs are disabled, the internal power supplies are shut down. Normal operation starts again when the temperature falls below the hysteresis and the over temperature condition clears.

6.2.5.4 Fault Conditions Summary

Table 2. Fault Conditions Summary

FAULT	CONDITION	H-BRIDGE	INTERNAL CIRCUIT	RECOVERY
VP undervoltage(UVLO)	VP < 4.2V	Disabled	Disabled	VP > 4.2V
Overcurrent(OCP)	I_{OUT} > 6A (MIN)	Disabled	Operating	t_{OCP_RST}
Thermal Shutdown(TSD)	T_J > 150°C (MIN)	Disabled	Operating	$T_J < T_{OTSD} - T_{HYS}$

7 Application Information

The GD30DR3002 is typically used to drive one brushed DC motor or other devices like solenoids.

7.1 Typical Application Circuit

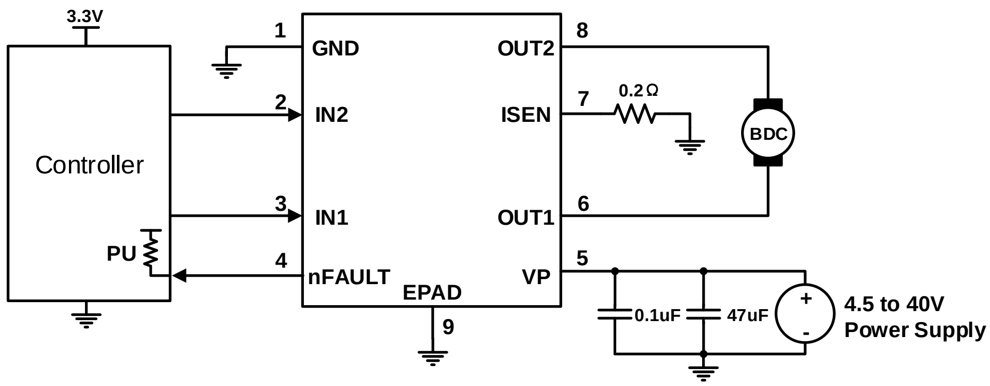


Figure 9. Schematic of GD30DR3002 Application

7.2 Design Example

For this design example, use the parameters in Table 3.

Table 3. Design Parameters

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Motor voltage	VP	24 V
Motor RMS current	I_{RMS}	0.8 A
Motor startup current	I_{START}	2 A
Motor current trip point	I_{TRIP}	1.75 A
Sense resistance	R_{SEN}	0.2 Ω
PWM frequency	f_{PWM}	2 KHz

7.3 Detailed Design Description

7.3.1 Motor Voltage

The motor voltage to use will depend on the ratings of the motor selected and the desired RPM. A higher voltage spins a brushed DC motor faster with the same PWM duty cycle applied to the power FETs. A higher voltage also increases the rate of current change through the inductive motor windings.

7.3.2 Low Power Mode

When entering sleep mode, GD recommends keeping all input pins low level to minimize system power consumption.

7.3.3 Sense Resistor

To ensure optimal performance, it is important for the sense resistor to be:

- Surface-mount
- Rated power meets the requirements
- Low Inductance
- Placed as close as to the motor driver pin

The power dissipated by the sense resistor can be calculated using $(I_{RMS})^2 \times R$. For example, if peak motor current is 2A, RMS motor current is 1A, and a 0.2Ω sense resistor is used, the resistor dissipates $1A^2 \times 0.2\Omega = 0.2W$. The power rapidly increases with higher current levels.

Resistors generally have a rated power within a specific range of ambient temperature and a reduced power curve at high ambient temperatures. When the PCB is shared with other components generating heat, the system designer should increase the margin. It is always best to measure the actual sense resistor temperature in a final system.

Power resistors are larger and more expensive than standard resistors, and it is common to use multiple standard resistors in parallel between the sense node and ground to distributes the current and heat dissipation.

7.4 Power Dissipation

Power dissipation in the GD30DR3002 is dominated by the power dissipated in the output FET resistance, or $R_{DS(on)}$. There is additional power due to PWM switching losses, which are dependent on PWM frequency, rise and fall time, and VP supply voltages. These switching losses are typically on the order of 10% to 30% of DC power dissipation.

The power dissipation of the GD30DR3002 device is on function of RMS motor current and FET ON-resistance of each output.

$$P_D \approx I_{RMS}^{\ 2} \times \left(R_{HS\_DS(ON)} + R_{LS\_DS(ON)}\right) \tag{2}$$

where

- PD is the device power dissipation
- RHS_DS(ON) is the resistance of the high-side FET
- RLS_DS(ON) is the resistance of the low-side FET
- IRMS is the RMS or DC output current being supplied to the load

$R_{DS(ON)}$ increases with temperature, so as the device heats, the power dissipation increases. This must be taken into consideration when sizing the heatsink.

7.5 Typical Application Curves

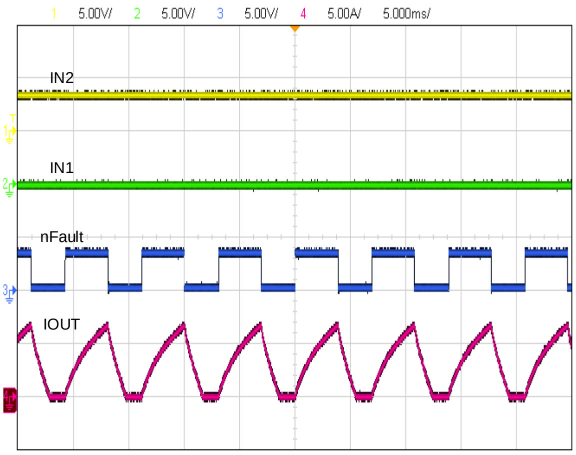


Figure 10. OCP nFault Report

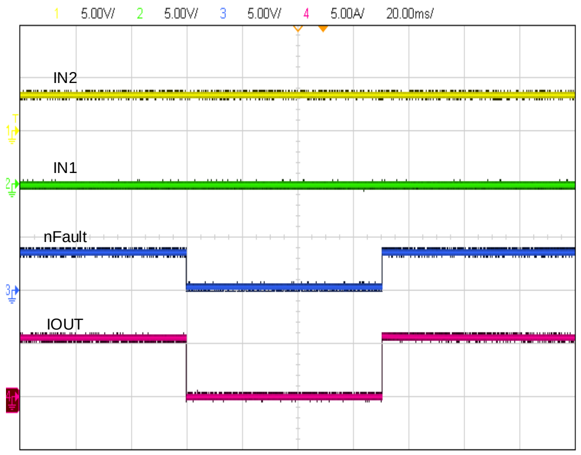


Figure 11. OTP nFault Report

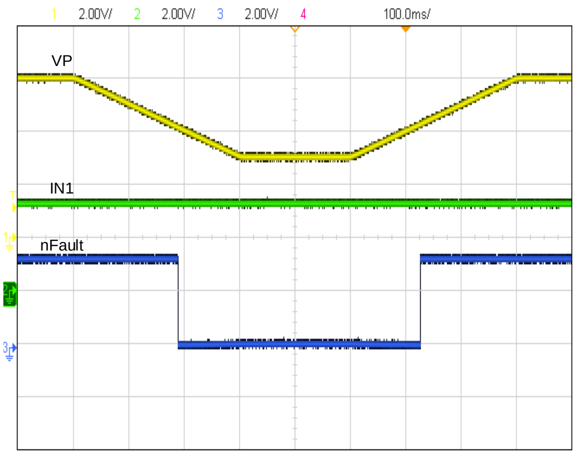


Figure 12. VP UVLO nFault Report

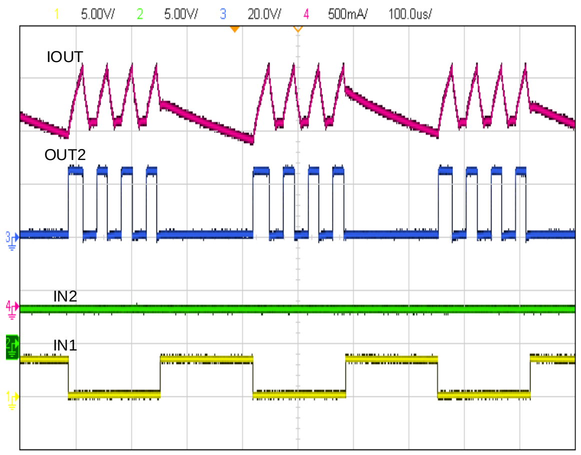


Figure 13. Current Regulation

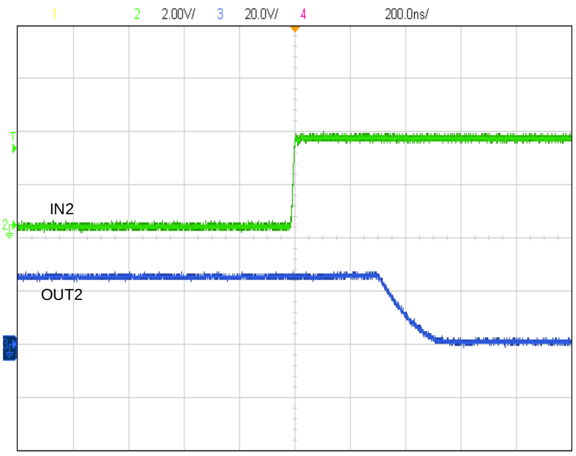


Figure 14. tpd

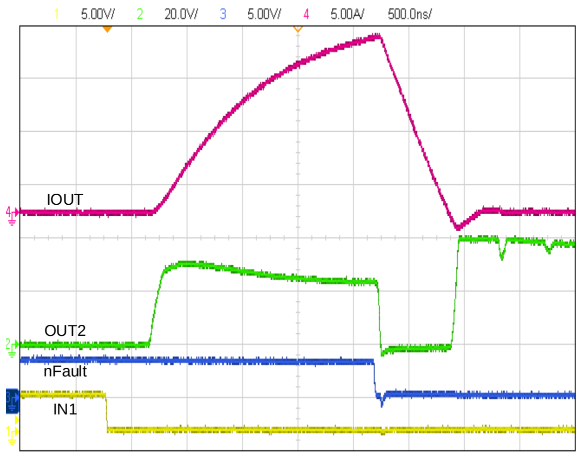


Figure 15. SCP

8 Layout Guidelines and Example

8.1 Layout Guidelines

Low ESR ceramic capacitors should be utilized for the VP to GND bypass capacitors. 0.1μF X5R or X7R types are recommended. These capacitors should be placed as close to the VP pin as possible with a thick trace or ground plane connection to the device GND pin.

In addition, bulk capacitor is required on the VP pin. This bulk capacitor can be ceramic or electrolytic type, but should also be placed as close as possible to the VP pin to minimize the loop inductance.

The high-current device outputs should use wide metal trace, and numerous vias should be used when connecting PCB layers.

8.2 Layout Example

Recommended layout and placement is shown in the following diagram.

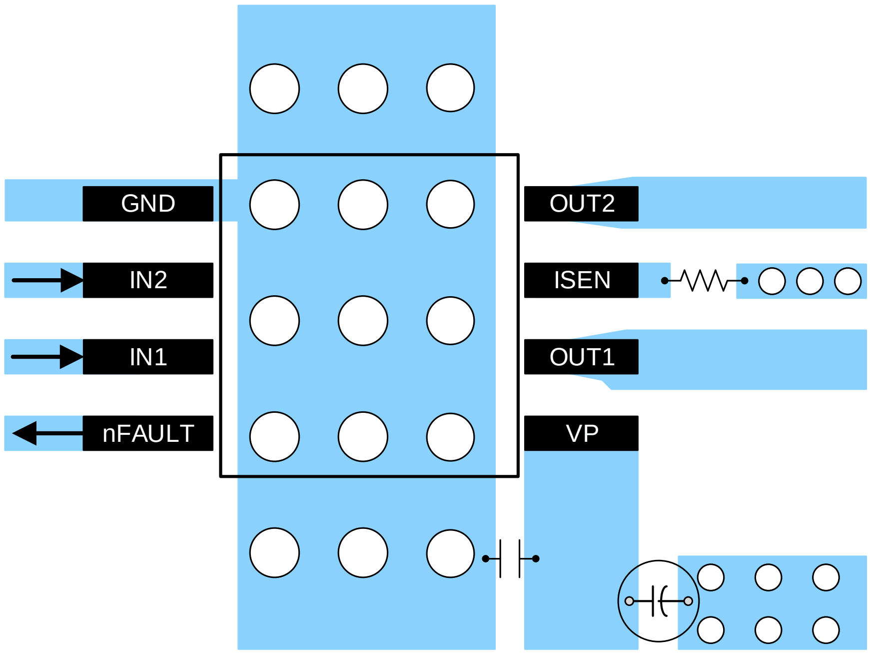
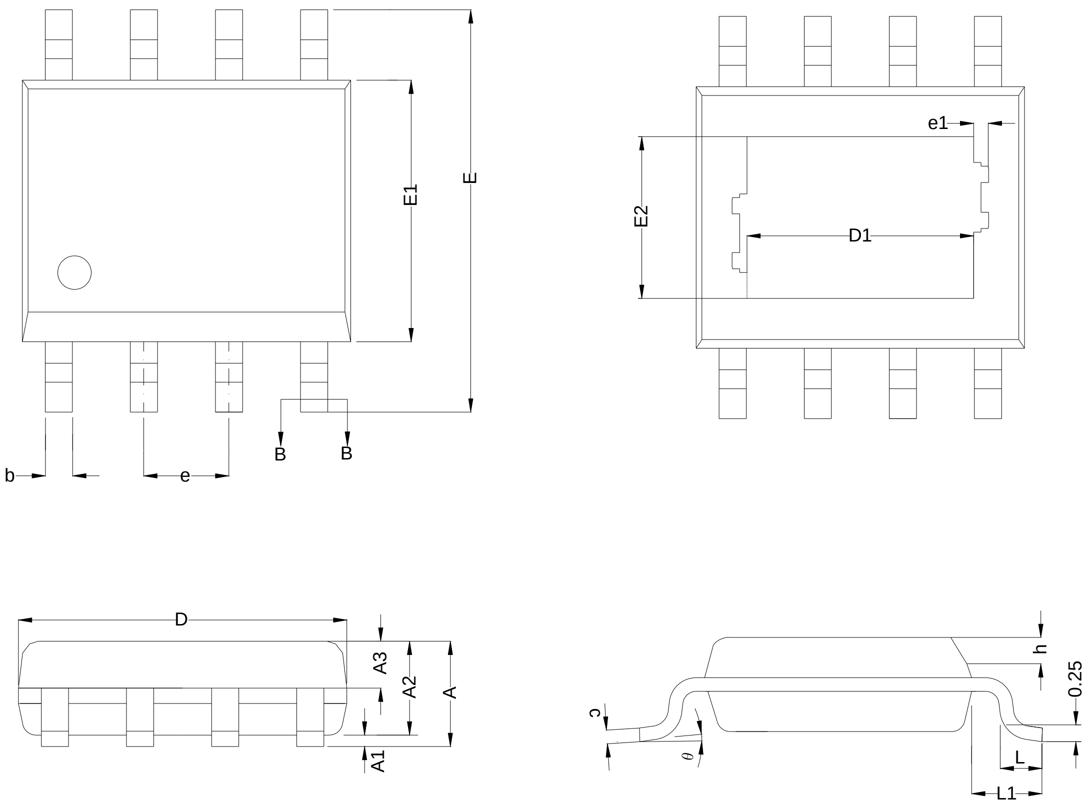


Figure 16. Simplified Layout Example

9 Package Information

9.1 Outline Dimensions

EP-SOP8 Package Outline



NOTES:

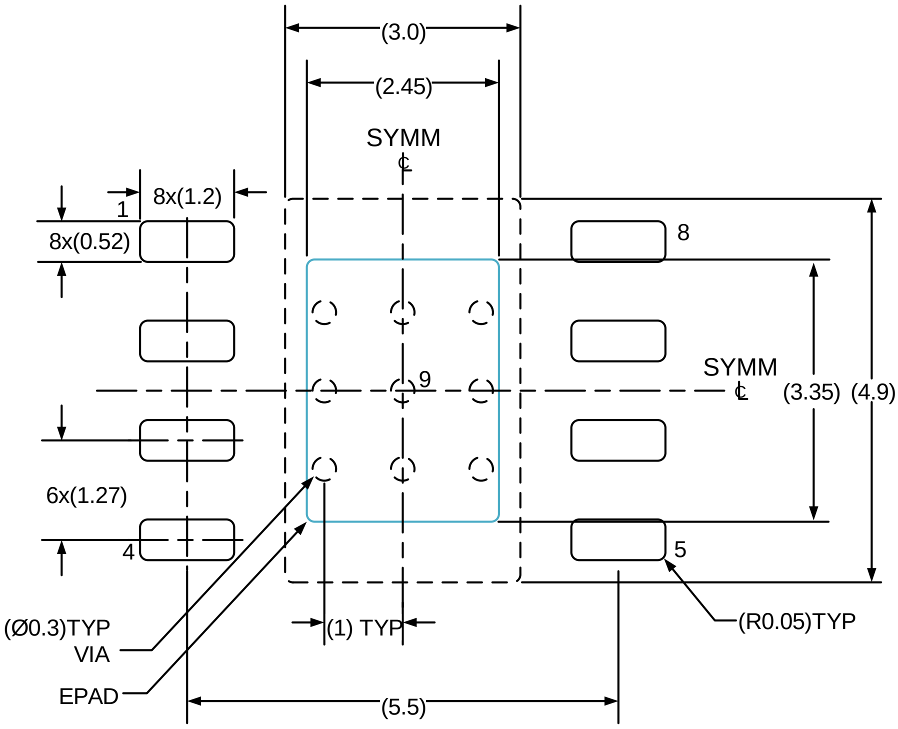
1. All dimensions are in millimeters.
2. Package dimensions does not include mold flash, protrusions, or gate burrs.
3. Refer to the Table 4 *EP-SOP8 dimensions(mm)*.

Table 4. EP-SOP8 dimensions(mm)

SYMBOL	MIN	NOM	MAX
A			1.65
A1	0.05		0.15
A2		1.30	
A3	0.60	0.65	0.70
b	0.39		0.47
c	0.20		0.24
D	4.80	4.90	5.00
D1		3.10	
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
E2		2.21	
e		1.27	
e1		0.10	
L	0.50	0.60	0.80
L1		1.05	
h	0.25		0.50
θ	0°		8°

9.2 Recommended Land Pattern

EP-SOP8 Land Pattern Example



NOTES: (continued)

1. Refer to the IPC-7351 can also help you complete the designs.
2. Exposed metal shown.
3. Drawing is 10X scale.

10 Ordering Information

Ordering Code	Package Type	ECO Plan	Packing Type	MOQ	OP Temp(°C)
GD30DR3002WGTR-K	EP-SOP8	Green	Tape & Reel	4000	−40°C to +125°C

11 Revision History

REVISION NUMBER	DESCRIPTION	DATE
1.0	Initial release and device details	2023
1.1	Modify Input low voltage V_{IL} value	2023

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