Mico-Power 22µA, 66ns, 1.7V, RRI, CMOS Input Comparators

1 Features

- Micro-power Operating Current (22µA) Preserves Battery Power
- Fast 66 ns Propagation Delay (100mV Overdrive)
- Single 1.7V to 5.5V Supply Voltage Range – Can be Powered from the Same 1.8V/2.5V/3.3V/5V System Rails
- Rail-to-Rail Input
- Push-Pull Output Current Drive: 30mA Typically at 5V Supply
- Internal Hysteresis for Clean Switching
- Internal RF/EMI Filter
- Operating Temperature Range: −40°C to +125°C

2 Applications

- Consumer Accessories
- Handsets, Tablets and Notebooks
- Portable and Battery-Powered Devices
- Threshold Detectors and Discriminators
- Alarms and Monitoring Circuits
- Zero-Crossing Detectors
- Window Comparators
- Level Translators
- Line Receivers
- IR Receivers

3 Description

The GD30CP872x are tiny, single-channel and dual-channel comparators with push-pull output that offer the ultimate combination of high speed (66ns propagation delay) and very low power consumption (22µA), available in extremely small packages with features such as rail-to-rail inputs, low offset voltage (0.8mV), large output drive current, and a wide range of supply voltages from 1.7V to 5.5V. The devices are very easy to implement in a wide variety of applications where require critical response time, power-sensitive, low-voltage, and/or tight board space.

The output of the GD30CP872x pulls to within 0.1V of either supply rail without external pull-up circuitry, making these devices ideal for interface with both CMOS and TTL logics. All input and output pins can tolerate a continuous short-circuit fault condition to either rail. Internal hysteresis ensures clean output switching, even with slow-moving input signals.

The GD30CP8721/GD30CP8723 (single) is available in both SOT23-5L and SC70-5L packages. The GD30CP8722 (dual) is offered in DFN-8L, SOIC-8L and MSOP-8L packages. All devices are rated over −40°C to +125°C industrial temperature range.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
GD30CP8721	SOT23-5L	2.92mm x 1.63mm
	SC70-5L	2.10mm x 1.25mm
GD30CP8722	DFN2x2-8L	2.00mm x 2.00mm
	SOIC-8L	4.90mm x 3.92mm
	MSOP-8L	3.00mm x 3.00mm
GD30CP8723	SOT23-5L	2.92mm x 1.63mm

1. For all available packages, see *Package Information* and *Ordering Information* at the end of datasheet.

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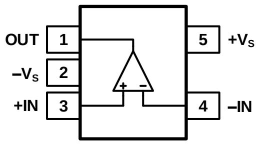
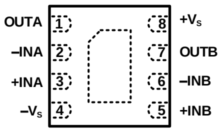
4 Device Overview

4.1 Pinout and Pin Assignment

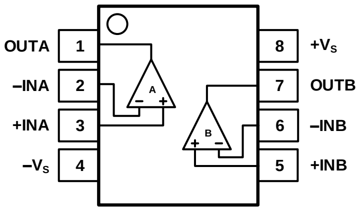
GD30CP8721-I
SOT23-5L / SC70-5L
Top View



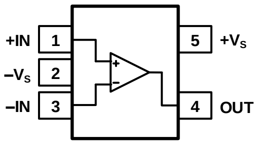
GD30CP8722-I
DFN2x2-8L
Top View



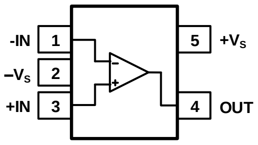
GD30CP8722-I
SOIC-8 / MSOP-8
Top View



GD30CP8723-I
SOT23-5L
Top View



GD30CP8723-S
SOT23-5L
Top View



4.2 Pin Description

NAME	PIN TYPE[1]	FUNCTION
-IN	I	Negative input. The voltage range is from(V_{S-}– 0.1V) to (V_{S+} + 0.1V).
+IN	I	Positive input. This pin has the same voltage range as –IN.
+V_S	P	Positive power supply. The voltage is from 1.7V to 5.5V. Split supplies are possible as long as the voltage between V_{S+} and V_{S-} is from 1.7V to 5.5V.
-V_S	P	Negative power supply. It is normally tied to ground. It can also be tied to a voltage other than ground as long as the voltage between V_{S+} and V_{S-} is from 1.7V to 5.5V.
OUT	O	Comparator output.

1. I = Input, O = Output, P = Power.

5 Parameter Information

5.1 Absolute Maximum Ratings

Exceeding the operating temperature range (unless otherwise noted)[1]

SYMBOL	PARAMETER	MIN	MAX	UNIT
V_{S+} to V_{S-}	Supply voltage		10	V
V_I	Signal Input Voltage	$V_{S-} - 0.5$	$V_{S+} + 0.5$	V
I_I	Signal Input Current	−10	10	mA
	Output Short-Circuit		Continuous	s
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature Range	−65	+150	°C
	Lead Temperature Range (Soldering 10 sec)		260	°C

1. The maximum ratings are the limits to which the device can be subjected without permanently damaging the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

5.2 Recommended Operation Conditions

SYMBOL[1,2]	PARAMETER	MIN	TYP	MAX	UNIT
V_S	Input supply voltage range	1.7		5.5	V
V_{CM}	Common-mode voltage range	$V_{S-} - 0.1$		$V_{S+} + 0.1$	V
T_A	Operating temperature range	−40		125	°C

1. The device is not guaranteed to function outside of its operating conditions.

5.3 ESD Rating

PARAMETER	ITEM	VALUE	UNIT
Electrostatic Discharge Voltage	Human body model (HBM), per MIL-STD-883J / Method 3015.9[1]	±3000	V
	Charged device model (CDM), per ESDA/JEDEC JS-002-2014[2]	±2000	

1. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
2. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.4 Thermal Resistance

SYMBOL[1]	CONDITIONS	PACKAGE	VALUE	UNIT
Θ_{JA}	Package Thermal Resistance	SC70-5L	333	°C/W
		SOT23-5L	190	
		DFN2x2-8L	80	
		MSOP-8L	216	
		SOIC-8L	125	

1. Thermal characteristics are based on simulation, and meet JEDEC document JESD51-7.

5.5 Electrical Characteristics

V_S = 5V, T_A = 25°C, unless otherwise noted.

Boldface limits apply over the specified temperature range, T_A = −40 to +125 °C.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	V_{CM} = V_S / 2		±0.8	±3.5	mV
		T_A = −40 to +125°C			±4	
dV_{OS}/d_T	Offset voltage drift[1]	T_A = −40 to +125°C		±1		μV/°C
PSRR	Power supply rejection ratio	V_S = 1.7 to 5.5 V, V_{CM} < V_{S+} − 1V	65	80		dB
		T_A = −40 to +125°C	60			
Hyst	Input hysteresis	V_{CM} = V_S / 2		3		mV
INPUT BIAS CURRENT						
I_B	Input bias current	V_{CM} = V_{S+} / 2		5		pA
		T_A = +85°C		200		
		T_A = +125°C		750		
I_{OS}	Input offset current	V_{CM} = V_{S+} / 2		10		pA
		T_A = +125°C		900		uA
INPUT VOLTAGE						
V_{CM}	Common-mode voltage range	T_A = −40 to +85 °C	V_{S-} – 0.1		V_{S-} + 0.1	V
		T_A = −40 to +125 °C	V_{S-} + 0.1		V_{S-} – 0.1	
CMRR	Common-mode rejection ratio	V_{CM} = −0.1 to 5.0 V	60	82		dB
		V_{CM} = 0.1 to 4.8 V, T_A = −40 to +125 °C	55			
		V_S = 2.0 V, V_{CM} = −0.1 to 2.0 V	56	78		
		V_{CM} = 0 to 1.8 V, T_A = −40 to +125 °C	52			
INPUT IMPEDANCE						
R_{IN}	Input resistance		100			GΩ
C_{IN}	Input capacitance	Differential		2.0		pF
		Common mode		3.5		
OUTPUT						
A_{VOL}	High output voltage swing	I_{SOURCE} = 1mA		63	80	mV
		T_A = −40 to +125 °C			120	
V_{OL}	Low output voltage swing	I_{SINK} = 1mA		44	58	mV
		T_A = −40 to +125 °C			90	
I_{SC}	Output short-circuit current			±30		mA
POWER SUPPLY						
V_S	Operating supply voltage	T_A = −40 to +125 °C	1.7		5.5	V

Electrical Characteristics(continued)

V_S = 5V, T_A = 25°C, unless otherwise noted.

Boldface limits apply over the specified temperature range, T_A = −40 to +85 °C.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
I_Q	Quiescent current (per comparator)	V_S = 1.8 V, V_{CM}= 0.5 V, I_O= 0		19	26	uA
		T_A = −40 to +85 °C			37	
		V_S = 5.0 V, V_{CM}= 0.5 V, I_O= 0		22	32	
		T_A = −40 to +85 °C			46	
		V_S = 1.8 V, V_{CM}= 0.5 V, I_O= 0, T_A = +125 °C			50	
		V_S = 5.0 V, V_{CM}= 0.5 V, I_O= 0, T_A = +125 °C			60	
SWITCHING CHARACTERISTICS						
t_{PD+}	Propagation delay time, Low to high	Input overdrive = 20 mV, C_L= 15 pF		138		ns
		Input overdrive = 100 mV, C_L= 15 pF		78		
t_{PD-}	Propagation delay time, High to low	Input overdrive = 20 mV, C_L= 15 pF		155		ns
		Input overdrive = 100 mV, C_L= 15 pF		66		
t_R	Rise time	Input overdrive = 20 mV, C_L= 15 pF		10		ns
		Input overdrive = 100 mV, C_L= 15 pF		8		
t_F	Fall time	Input overdrive = 20 mV, C_L= 15 pF		8		ns
		Input overdrive = 100 mV, C_L= 15 pF		6		

1. Guaranteed by design and engineering sample characterization.

5.6 Typical Characteristics

V_S = ±2.5V, V_{CM} = $V_S/2$, R_L = 10kΩ connected to $V_S/2$, and C_L = 15pF, at T_A = +25°C, unless otherwise noted.

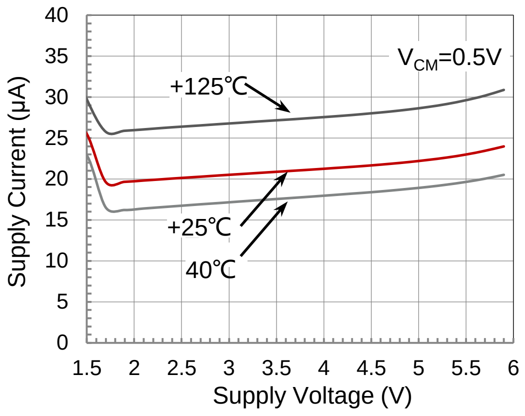


Figure 1. Supply Current vs. Supply Voltage

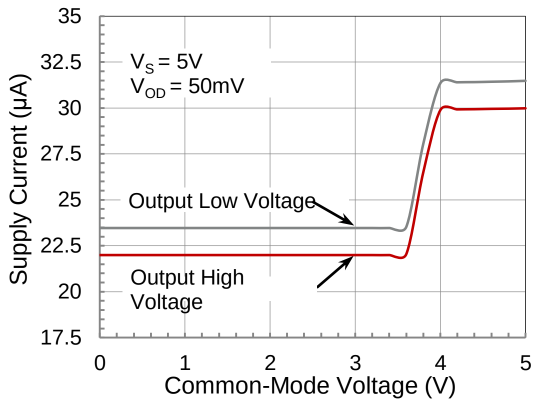


Figure 2. Supply Current vs. Common-Mode Input

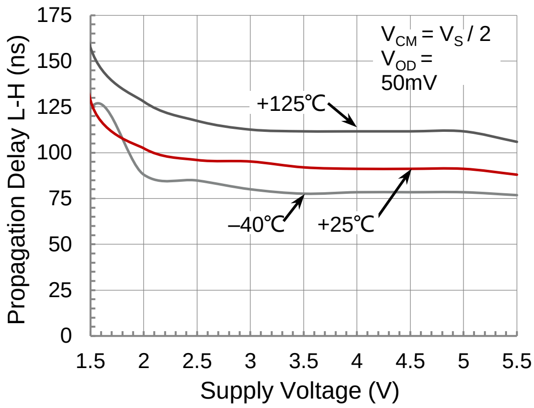


Figure 3. Propagation Delay L-H (t_{PD+})vs. Supply Voltage

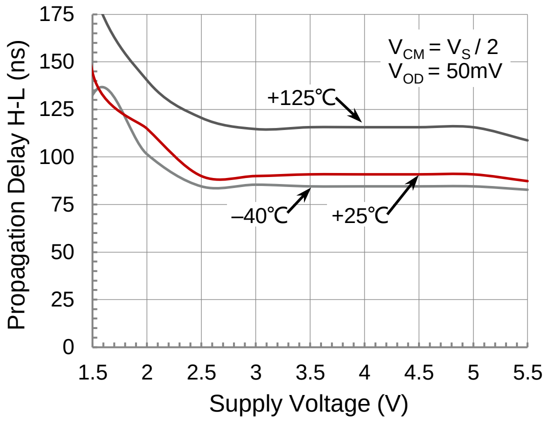


Figure 4. Propagation Delay H-L (t_{PD-})vs. Supply Voltage

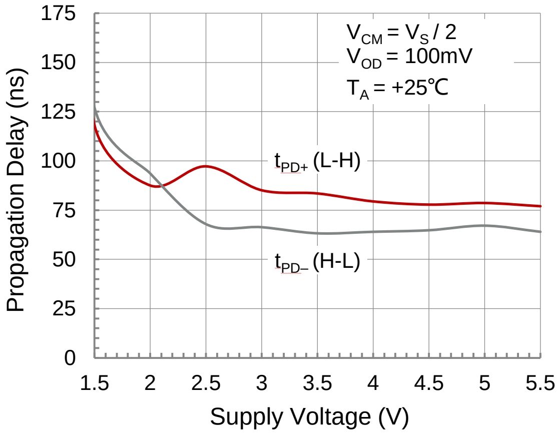


Figure 5. Propagation Delay vs. Supply Voltage

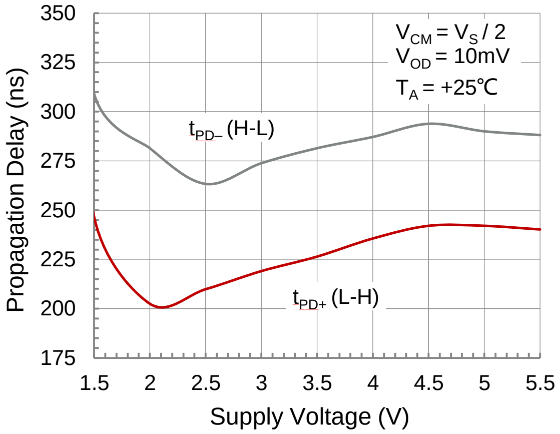


Figure 6. Propagation Delay vs. Supply Voltage

Typical Characteristics (continued)

V_S = ±2.5V, V_{CM} = V_S/2, R_L = 10kΩ connected to V_S/2, and C_L = 15pF, at T_A = +25°C, unless otherwise noted.

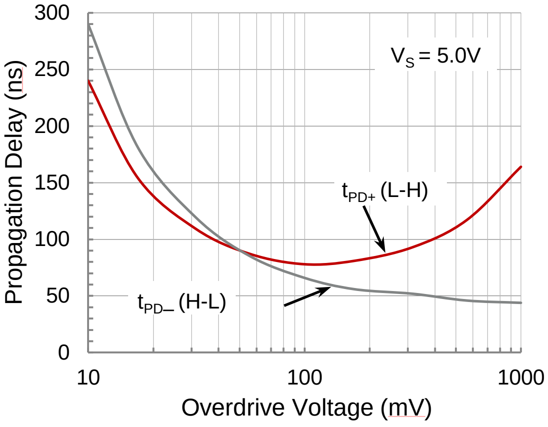


Figure 7. Propagation Delay vs. Input Overdrive

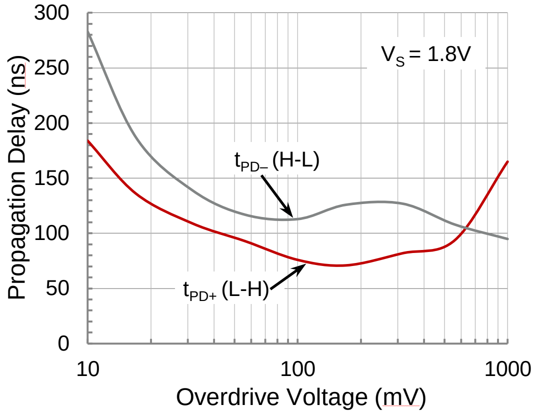


Figure 8. Propagation delay vs. Input Overdrive

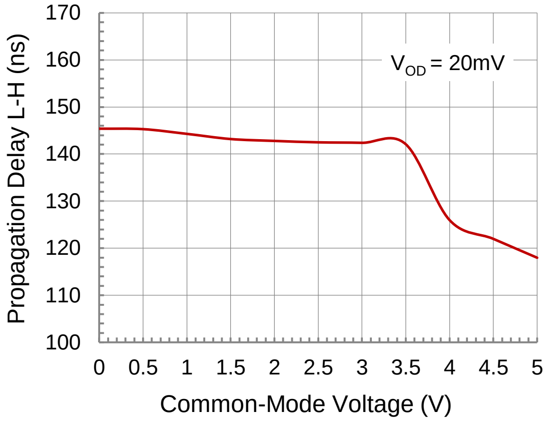


Figure 9. Propagation Delay L-H vs. Input Common-Mode

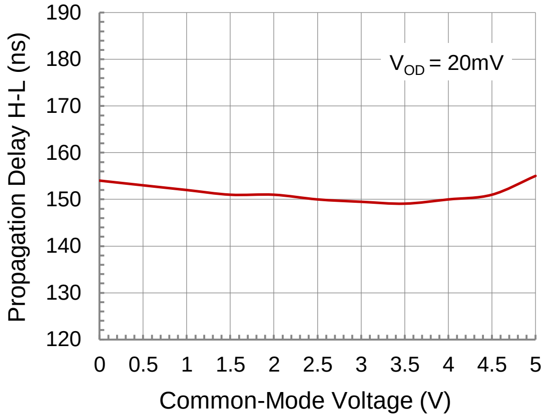


Figure 10. Propagation Delay H-L vs. Input Common-Mode

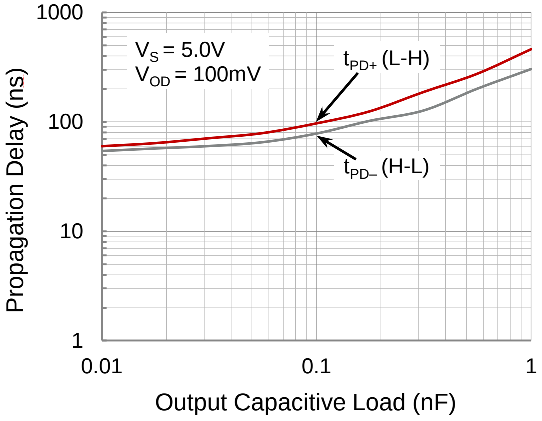


Figure 11. Propagation Delay vs. Capacitive Load

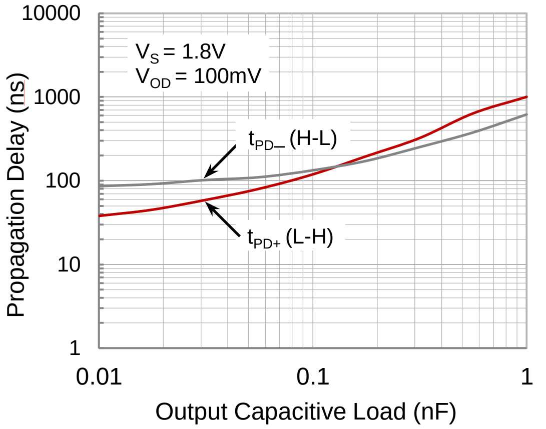


Figure 12. Propagation Delay vs. Capacitive Load

Typical Characteristics (continued)

V_S = ±2.5V, V_{CM} = $V_S/2$, R_L = 10kΩ connected to $V_S/2$, and C_L = 15pF, at T_A = +25°C, unless otherwise noted.

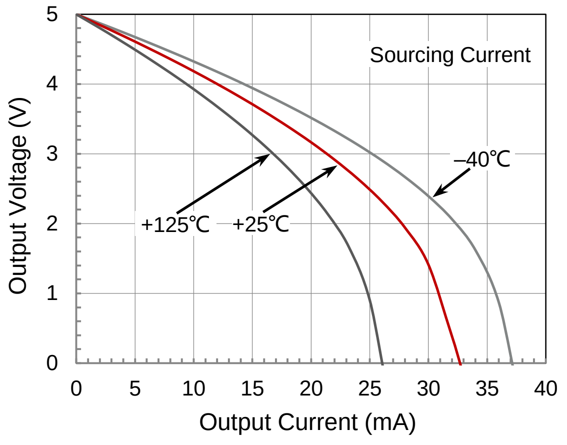


Figure 13. Output Voltage vs. Output Sourcing Current

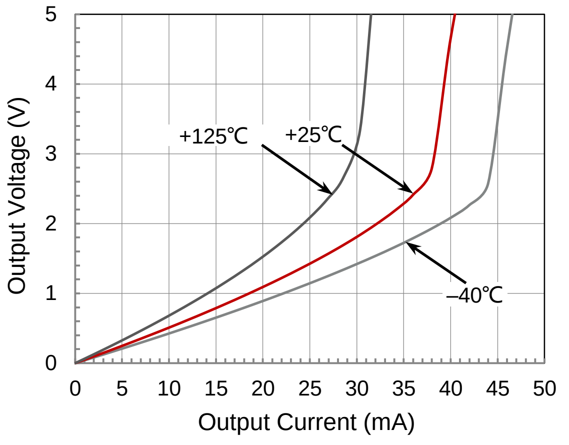


Figure 14. Output Voltage vs. Output Sinking Current

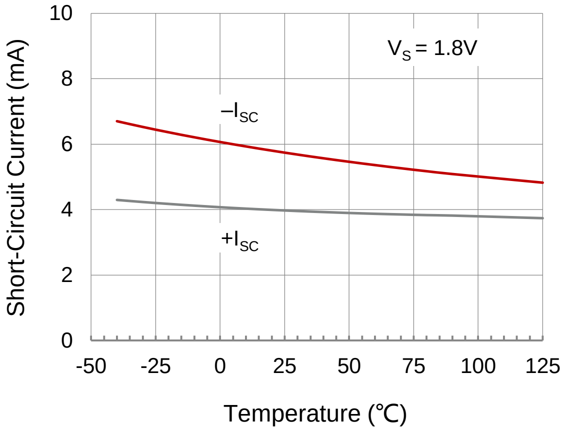


Figure 15. Short Circuit Current vs. Temperature

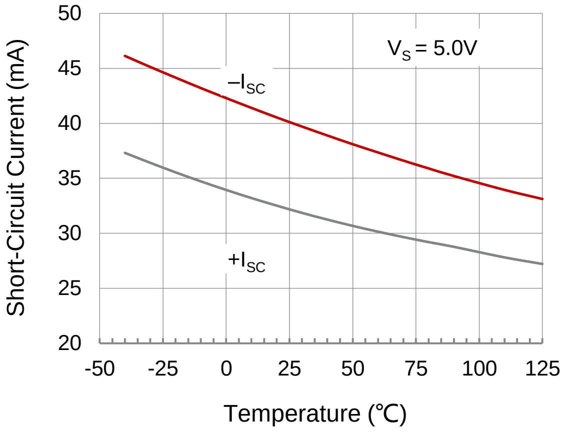


Figure 16. Short Circuit Current vs. Temperature

6 Detailed Design Description

6.1 Operating Voltage

The GD30CP872x of micro-power push-pull output comparators is fully specified and ensured for operation from 1.7V to 5.5V and offers an excellent speed-to-power combination with a propagation delay of 70ns and a quiescent supply current of 22µA. This combination of fast response time at micro- power enables power conscious systems to monitor and respond quickly to fault conditions.

In addition, and many specifications apply over the industrial temperature range of −40°C to +125°C. Parameters that vary significantly with operating voltages or temperature are illustrated in the *Typical Characteristics* graphs.

6.2 Input Voltage

The input common-mode voltage range of the GD30CP872x comparators extends 100mV beyond the supply rails. This performance is achieved with a complementary input stage: an N-channel input differential pair in parallel with a P-channel differential pair. The N-channel pair is active for input voltages close to the positive rail, typically V_{S+}−1.4V to the positive supply, whereas the P-channel pair is active for inputs from 100mV below the negative supply to approximately V_{S+}−1.4V. There is a small transition region, typically V_{S+}−1.2V to V_{S+}−1V, in which both pairs are on. This 200mV transition region can vary up to 200mV with process variation. Thus, the transition region (both stages on) can range from V_{S+}−1.4V to V_{S+}−1.2V on the low end, up to V_{S+}−1V to V_{S+}−0.8V on the high end. Within this transition region, PSRR, CMRR, offset voltage, offset drift, and THD can be degraded compared to device operation outside this region.

6.3 Input EMI Filter and Clamp Circuit

The GD30CP872x comparator family uses CMOS transistors at the inputs which prevent phase inversion when the input pins exceed the supply voltages.

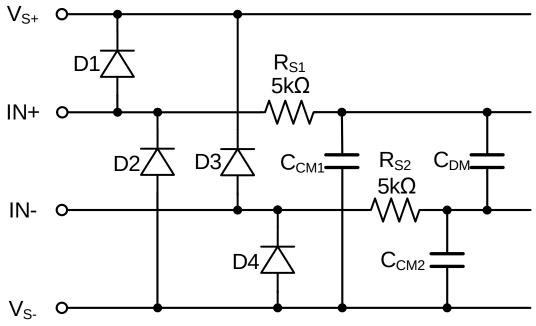


Figure 17. Input EMI Filter and Clamp Circuit

Figure 17 shows the input EMI filter and clamp circuit. The GD30CP872x comparators have internal ESD protection diodes (D1, D2, D3, and D4) that are connected between the inputs and each supply rail. These diodes protect the input transistors in the event of electrostatic discharge and are reverse biased during normal operation. This protection scheme allows voltages as high as approximately 500mV beyond the rails to be applied at the input of either terminal without causing permanent damage. See the table of *Absolute Maximum Ratings* for more information.

6.4 EMI Rejection Ratio

Circuit performance is often adversely affected by high frequency EMI. When the signal strength is low and transmission lines are long, an amplifier must accurately amplify the input signals. However, all comparator pins — the non-inverting input, inverting input, positive supply, negative supply, and output pins — are susceptible to EMI signals. These high frequency signals are coupled into an comparator by various means, such as conduction, near field radiation, or far field radiation. For example, wires and printed circuit board (PCB) traces can act as antennas and pick up high frequency EMI signals.

Amplifiers do not amplify EMI or RF signals due to their relatively low bandwidth. However, due to the nonlinearities of the input devices, comparators can rectify these out of band signals. When these high frequency signals are rectified, they appear as a dc offset at the output.

The GD30CP872x comparators have integrated EMI filters at their input stage. A mathematical method of measuring EMIRR is defined as follows:

$$EMIRR = 20\log\left(\frac{V_{IN\_PEAK}}{\Delta V_{OS}}\right) \tag{1}$$

6.5 Internal Hysteresis

Most high-speed comparators oscillate in the linear region because of noise or undesired parasitic feedback. This tends to occur when the voltage on one input is at or equal to the voltage on the other input. To counter the parasitic effects and noise, the devices have an internal hysteresis of 5mV.

The hysteresis in a comparator creates two trip points: one for the rising input voltage and one for the falling input voltage. The difference between the trip points is the hysteresis. The average of the trip points is the offset voltage. When the comparator's input voltages are equal, the hysteresis effectively causes one comparator input voltage to move quickly past the other, thus taking the input out of the region where oscillation occurs. Standard comparators require hysteresis to be added with external resistors. To increase hysteresis and noise margin even more, add positive feedback with two resistors as a voltage divider from the output to the non- inverting input. Figure 18 illustrates the case where IN– is fixed and IN+ is varied. If the inputs were reversed, the figure would look the same, except the output would be inverted.

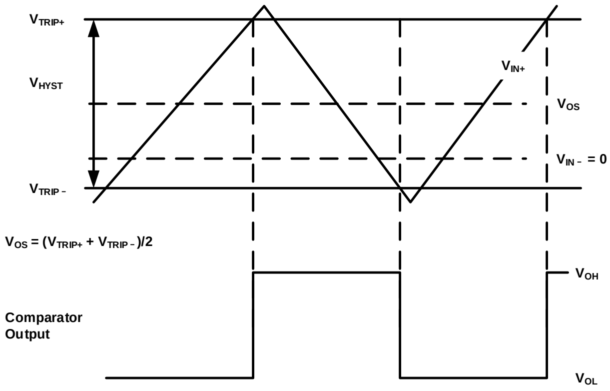


Figure 18. Input and Output Waveform, Non-inverting Input Varied

6.6 Input-to-Output Coupling

To minimize capacitive coupling, the input and output signal traces should not be parallel. This helps reduce unwanted positive feedback.

6.7 Maximizing Performance Through Proper Layout

To achieve the maximum performance of the extremely high input impedance and low offset voltage of the GD30CP872x devices, care is needed in laying out the circuit board. The PCB surface must remain clean and free of moisture to avoid leakage currents between adjacent traces. Surface coating of the circuit board reduces surface moisture and provides a humidity barrier, reducing parasitic resistance on the board. The use of guard rings around the comparator inputs further reduces leakage currents. Figure 3 shows proper guard ring configuration and the top view of a surface-mount layout. The guard ring does not need to be a specific width, but it should form a continuous loop around both inputs. By setting the guard ring voltage equal to the voltage at the non-inverting input, parasitic capacitance is minimized as well. For further reduction of leakage currents, components can be mounted to the PCB using Teflon standoff insulators.

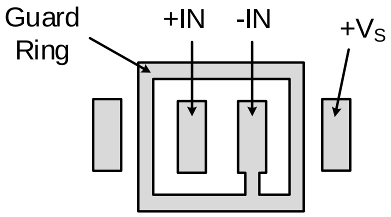


Figure 19. Use a Guard Ring Around Sensitive Pins

Other potential sources of offset error are thermo-electric voltages on the circuit board. This voltage, also called Seebeck voltage, occurs at the junction of two dissimilar metals and is proportional to the temperature of the junction. The most common metallic junctions on a circuit board are solder-to- board trace and solder-to-component lead. If the temperature of the PCB at one end of the component is different from the temperature at the other end, the resulting Seebeck voltages are not equal, resulting in a thermal voltage error.

This thermocouple error can be reduced by using dummy components to match the thermoelectric error source. Placing the dummy component as close as possible to its partner ensures both Seebeck voltages are equal, thus canceling the thermocouple error. Maintaining a constant ambient temperature on the circuit board further reduces this error. The use of a ground plane helps distribute heat throughout the board and reduces EMI noise pickup.

7 Application Information

7.1 Typical Application Circuit

7.1.1 IR Receiver AFE and Wake- Up Circuit

Infrared (IR) communication is inherently immune to RF interference as long as there is a line-of-sight path between the transmitter and the receiver. It is also one of the lowest cost communication schemes. This makes it a good choice for implementing wireless communications in applications such as utility metering. A common system topology to extend battery life is to use a power efficient IR receiver analog front end (AFE) that is always on and wakes up the host only when there is a valid IR signal detected as shown in Figure 20.

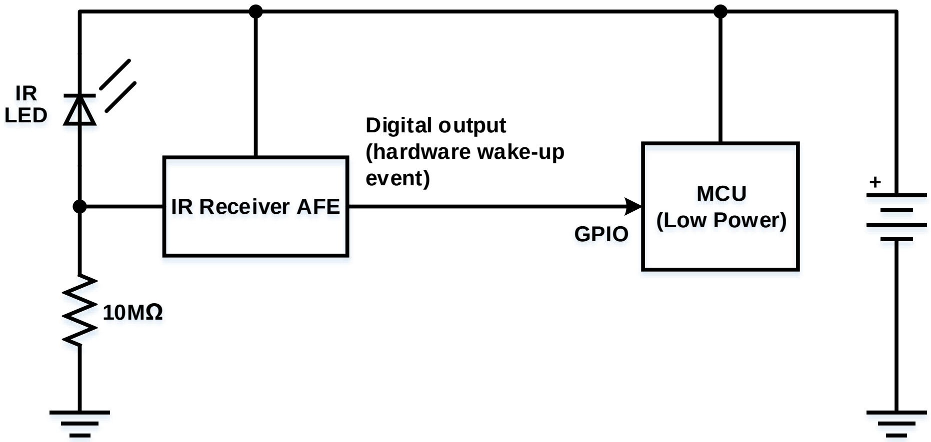


Figure 20. Coin Cell Battery Powered IR Receiver

Power efficient comparators such as the GD30CP872x can be used in the IR receiver AFE to increase battery life. The GD30CP872x device is responsible for two major tasks:

1. IR signal conditioning.
2. Host system wake-up.

The GD30CP872x device is constantly powered to always be ready to receive IR signals and wake up the host microcontroller (MCU) when data is received. The short working distance (approx 5 cm) is suitable for a virtual-contact operation where the IR transmitter and receiver are closely placed with an optional mechanical alignment guide.

Figure 20 shows the IR receiver system block diagram. The host MCU is normally in the shutdown mode (during which the quiescent current is less than 1μA) except when data is being transferred.

Figure 21 shows the detailed circuit design. The circuit establishes a threshold through R2 and C1 which automatically adapts to the ambient light level. To further reduce BOM cost, this example uses an IR LED as the IR receiver. The IR LED is reverse-biased to function as a photodiode (but at a reduced sensitivity).

The low input bias current allows a greater load resistor value (R_1) without sacrificing linearity, which in turn helps reduce the always-on supply current.

The load resistor R_1 converts the IR light induced current into a voltage fed into the inverting input of the comparator. R_2 and C_1 establish a reference voltage V_{REF} which tracks the mean amplitude of the IR signal. The non-inverting input is connected to V_{REF} through R_3. And finally R_3 and R_4 are used to introduce additional hysteresis to keep the output free of spurious toggles.

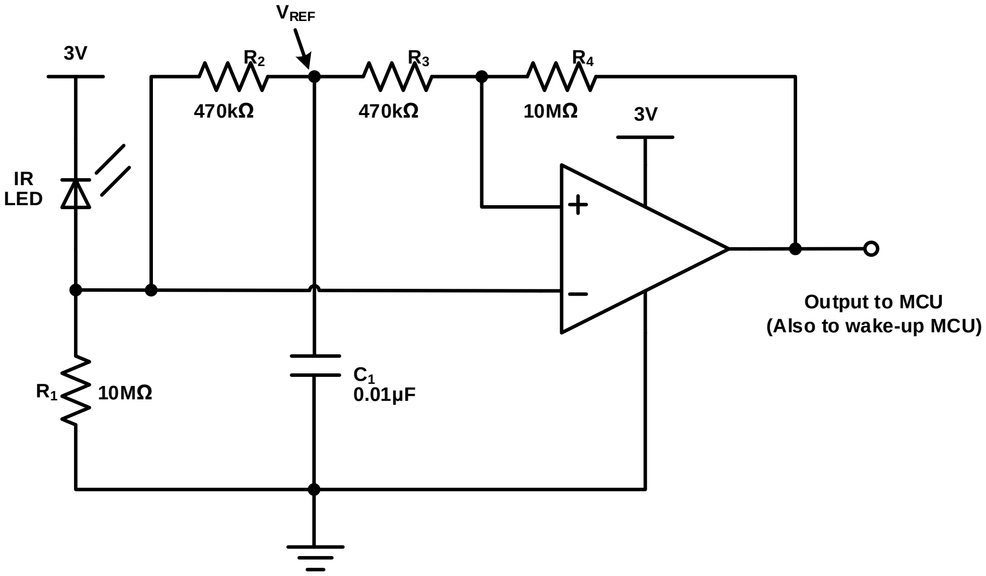


Figure 21. IR Receiver AFE Using Comprator

7.1.2 Use Window Comparator to Detect Under-Voltage and Over-Voltage

Window comparators are commonly used to detect undervoltage (UV) and overvoltage (OV) conditions. Figure 22 shows a simple window comparator circuit.

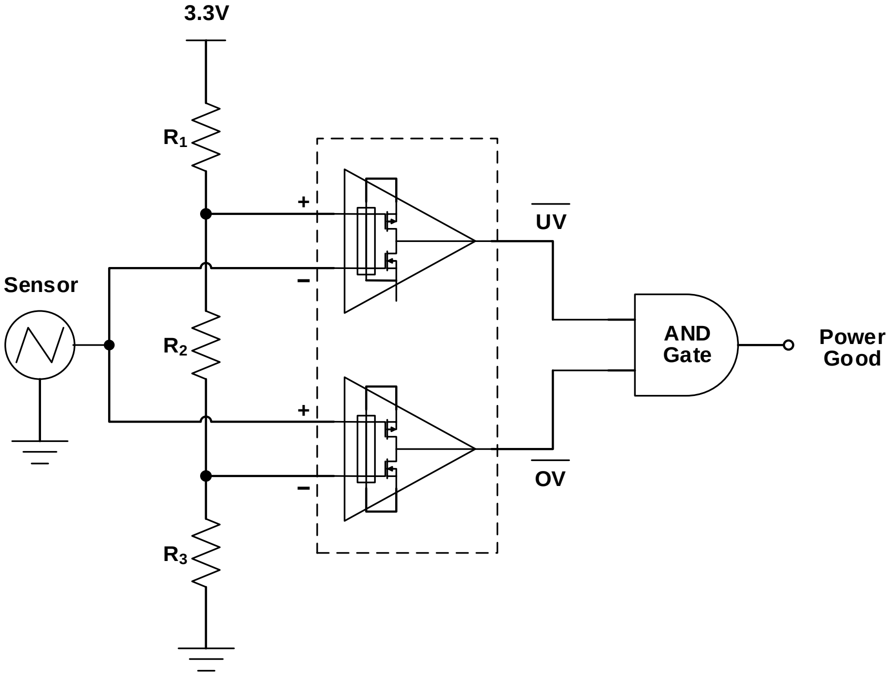


Figure 22. Window Comparator

For this design, follow these design requirements:

- Alert (logic low output) when an input signal is less than 1.1V
- Alert (logic low output) when an input signal is greater than 2.2V
- Alert signal is active low
- Operate from a 3.3V power supply

Configure the circuit as shown in Figure 22. Connect V_{S+} to a 3.3V power supply and V_{S-} to ground. Make R_1, R_2 and R_3 each 10MΩ resistors. These three resistors are used to create the positive and negative thresholds for the window comparator (V_{TH+} and V_{TH-}). With each resistor being equal, V_{TH+} is 2.2V and V_{TH-} is 1.1V. Large resistor values such as 10MΩ are used to minimize power consumption. The sensor output voltage is applied to the inverting and non-inverting inputs of the 2-channel GD30CP5020's. The respective comparator outputs will be low when the sensor is less than 1.1V or greater than 2.2V. V_{OUT} will be high when the sensor is in the range of 1.1V to 2.2V. See the application curve in Figure 23.

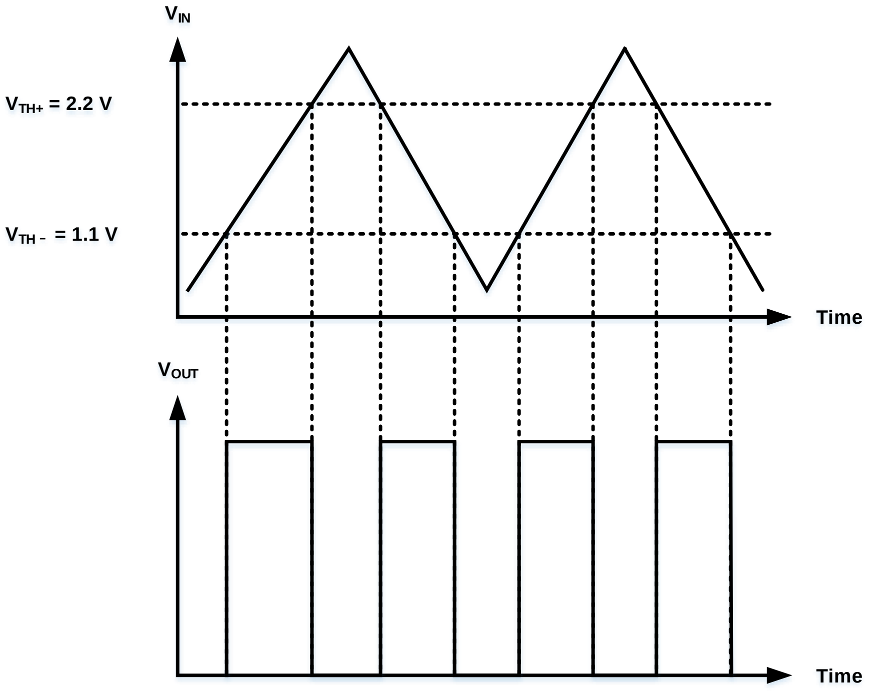
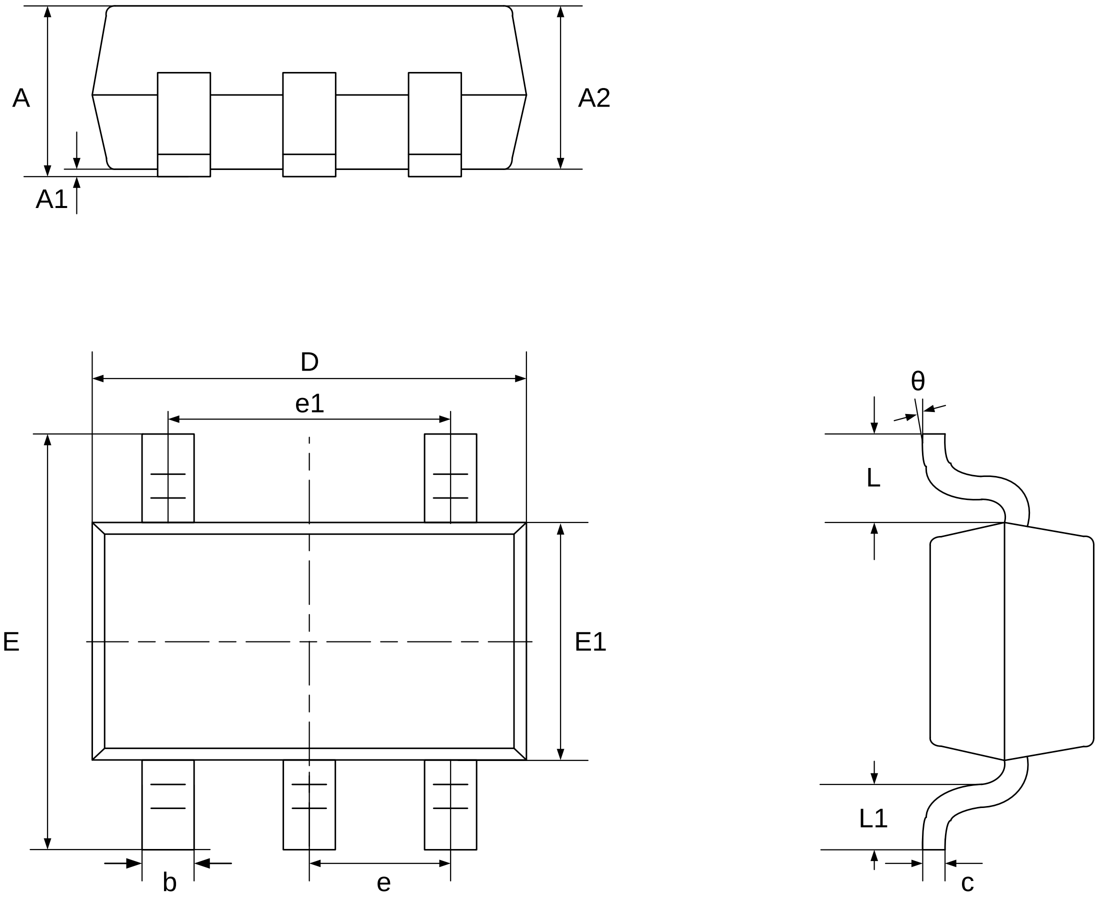


Figure 23. Window Comparator Results

8 Package Information

8.1 Outline Dimensions

SOT23-5L Package Outline



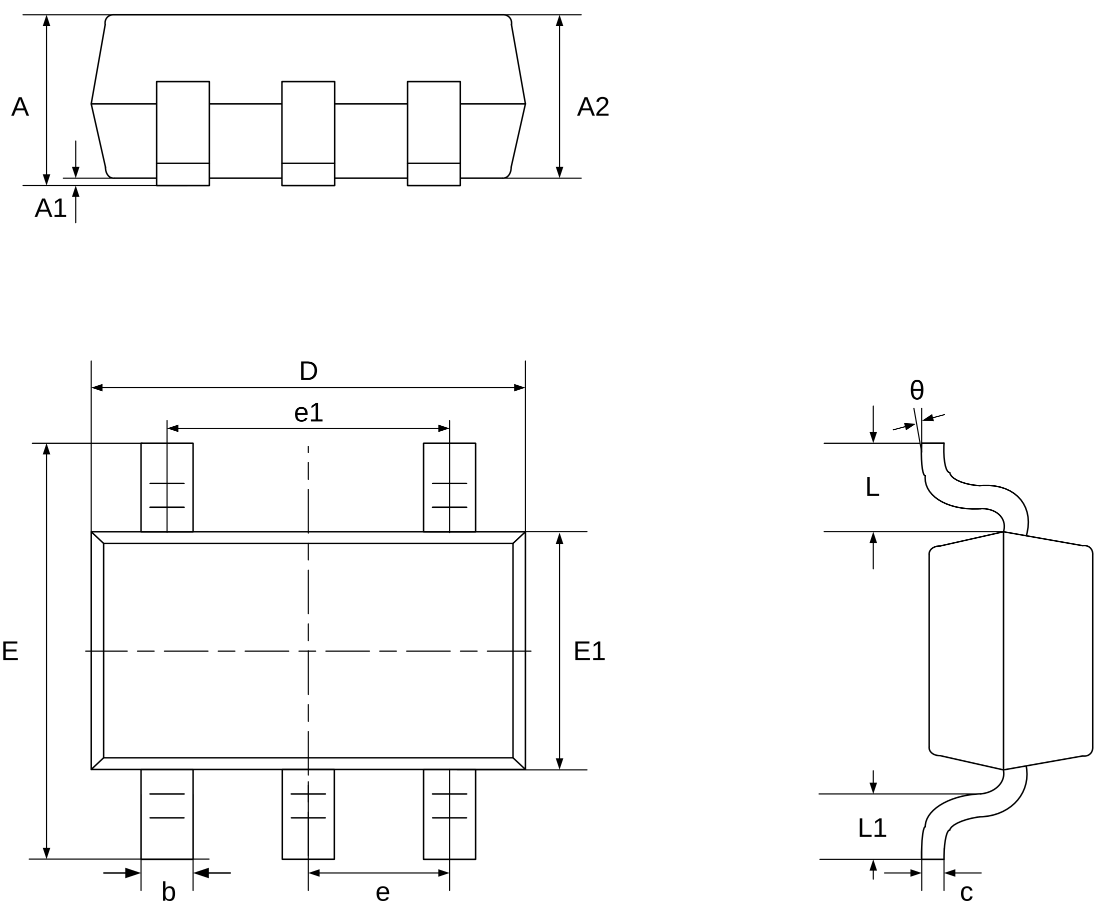
NOTES:

1. All dimensions are in millimeters.
2. Package dimensions does not include mold flash, protrusions, or gate burrs.
3. Refer to the Table 1 *SOT23-5L dimensions(mm).*

Table 1. SOT23-5L dimensions(mm)

SYMBOL	MIN	NOM	MAX
A			1.35
A1	0.00		0.15
A2	1.00		1.20
b	0.35		0.45
c	0.14		0.20
D	2.82		3.02
E	2.60		3.00
E1	1.526		1.726
e	0.95 BSC		
e1	1.90 BSC		
L	0.60 REF		
L1	0.30		0.60
θ	0°		8°

SC70-5L Package Outline



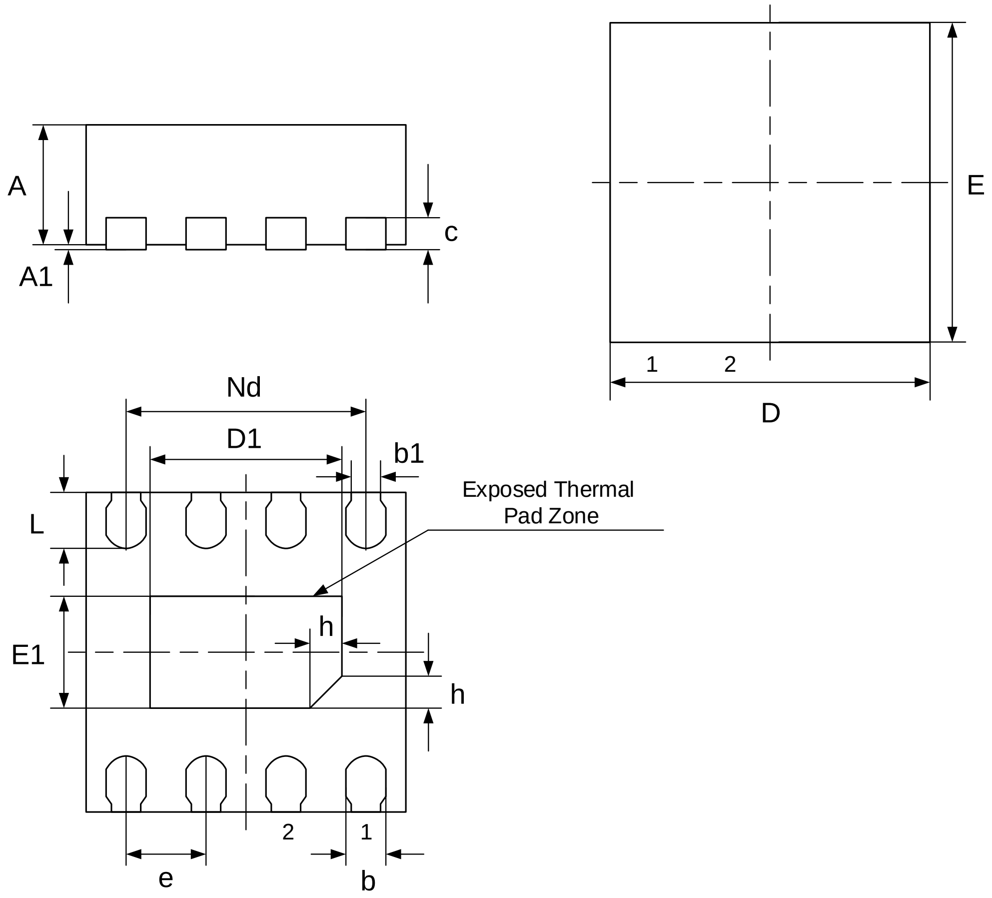
NOTES: (continued)

1. Refer to the Table 2 *SC70-5L dimensions(mm)*.

Table 2. SC70-5L dimensions(mm)

SYMBOL	MIN	NOM	MAX
A	0.90		1.10
A1	0.00		0.10
A2	0.90		1.00
b	0.15		0.35
c	0.08		0.15
D	2.00		2.20
E	2.15		2.45
E1	1.15		1.35
e	0.65 BSC		
e1	1.30 BSC		
L	0.525 REF		
L1	0.26		0.46
θ	0°		8°

DFN2x2-8L Package Outline



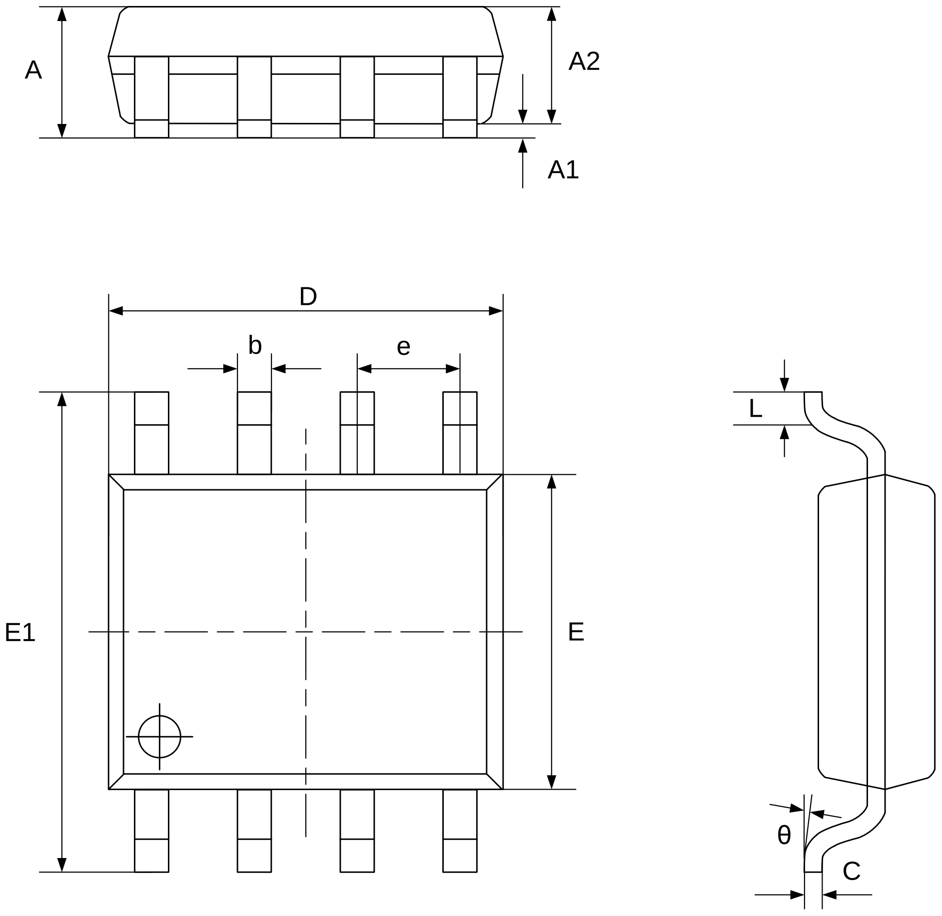
NOTES: (continued)

1. Refer to the Table 3 *DFN2x2-8L dimensions(mm)*.

Table 3. DFN2x2-8L dimensions(mm)

SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1		0.02	0.05
b	0.20	0.25	0.30
b1	0.18 REF		
c	0.18	0.20	0.25
D	1.90	2.00	1.30
D1	1.10	1.20	1.30
Nd	1.50 BSC		
E	1.90	2.00	2.10
E1	0.60	0.70	0.80
e	0.50 BSC		
L	0.30	0.35	0.40
h	0.15	0.20	0.25

SOIC-8L Package Outline



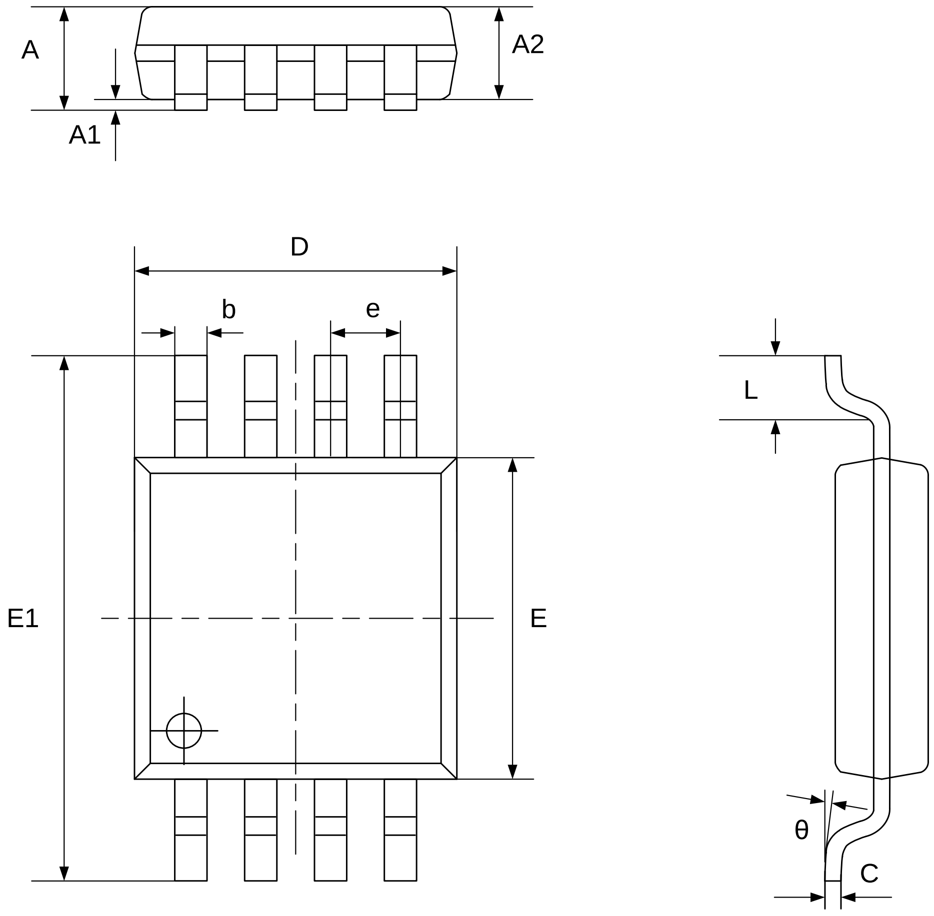
NOTES: (continued)

1. Refer to the Table 4 *SOIC-8L dimensions(mm)*.

Table 4. SOIC-8L dimensions(mm)

SYMBOL	MIN	NOM	MAX
A	1.370		1.670
A1	0.070		0.170
A2	1.300		1.500
b	0.306		0.506
C		0.203	
D	4.700		5.100
E	3.820		4.020
E1	5.800		6.200
e		1.270	
L	0.450		0.750
θ	0°		8°

MSOP-8L Package Outline



NOTES: (continued)

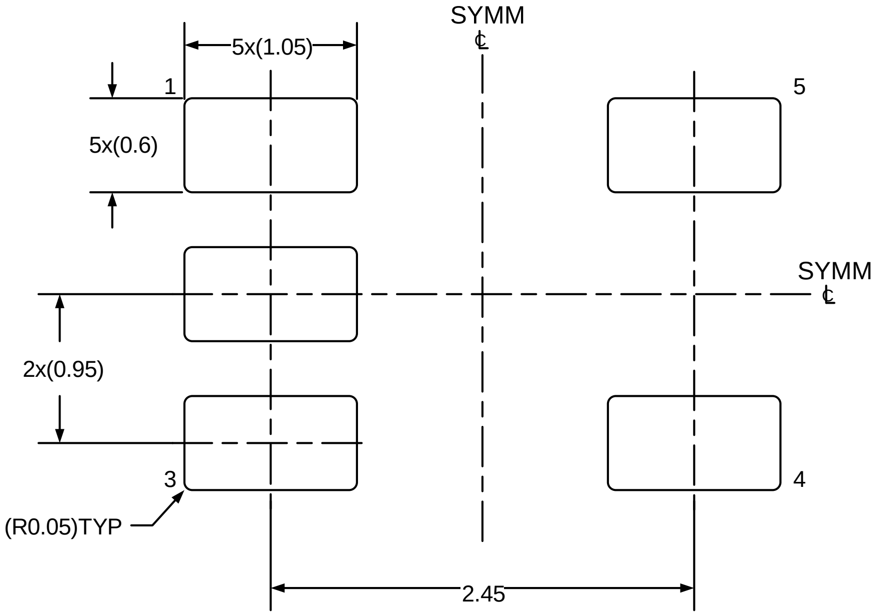
1. Refer to the Table 5 *MSOP-8L dimensions(mm)*.

Table 5. MSOP-8L dimensions(mm)

SYMBOL	MIN	NOM	MAX
A	0.800		1.100
A1	0.050		0.150
A2	0.750		0.950
b	0.290		0.380
C	0.150		0.200
D	2.900		3.100
E	2.900		3.100
E1	4.700		5.100
e		0.650	
L	0.400		0.700
θ	0°		8°

8.2 Recommended Land Pattern

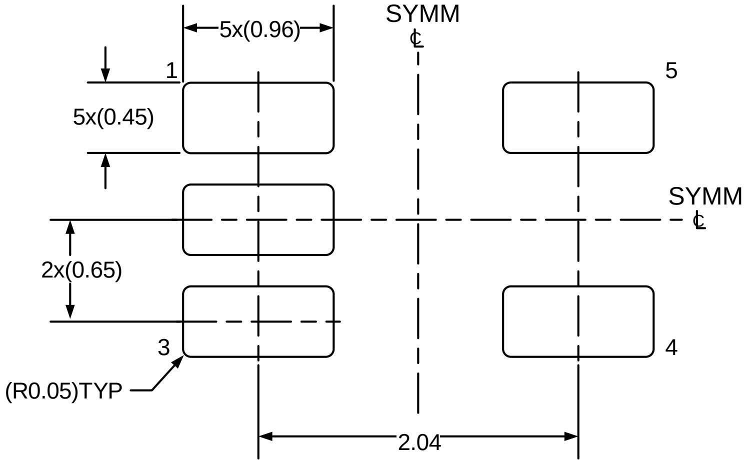
SOT23-5L Land Pattern Example



NOTES: (continued)

1. Refer to the IPC-7351 can also help you complete the designs.
2. Exposed metal shown.
3. Drawing is 20X scale.

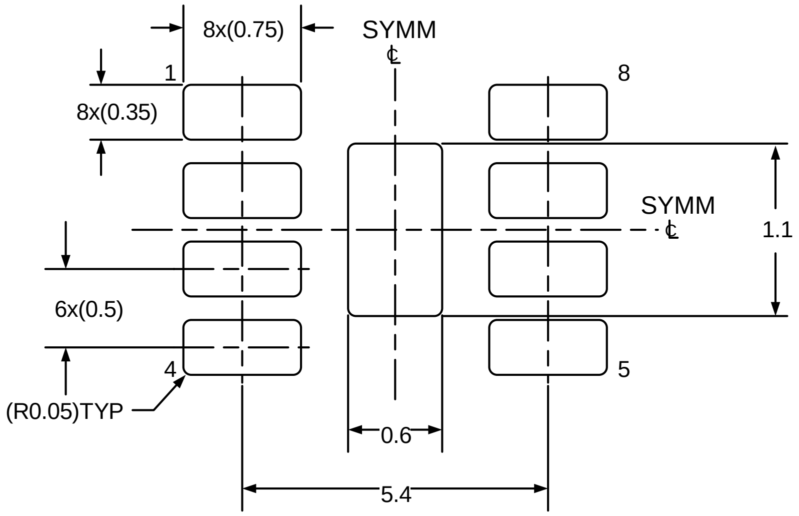
SC70-5L Land Pattern Example



NOTES: (continued)

1. Refer to the IPC-7351 can also help you complete the designs.
2. Exposed metal shown.
3. Drawing is 20X scale.

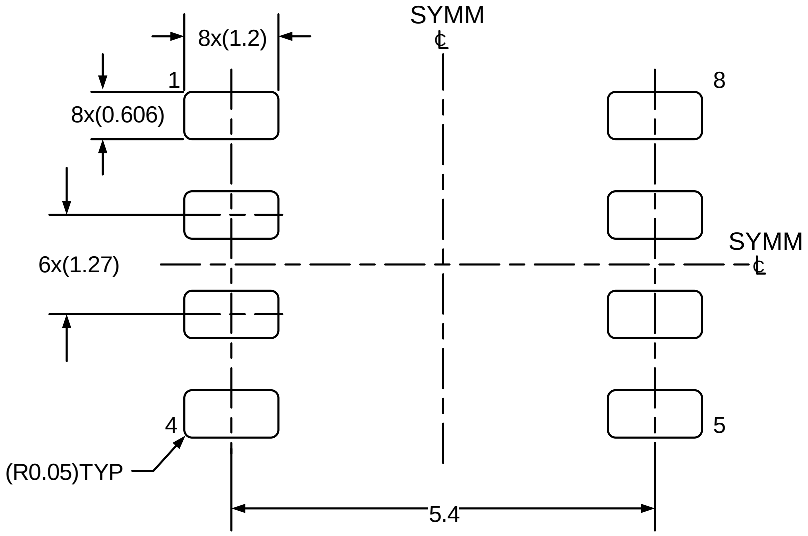
DFN2x2-8L Land Pattern Example



NOTES: (continued)

1. Refer to the IPC-7351 can also help you complete the designs.
2. Exposed metal shown.
3. Drawing is 20X scale.

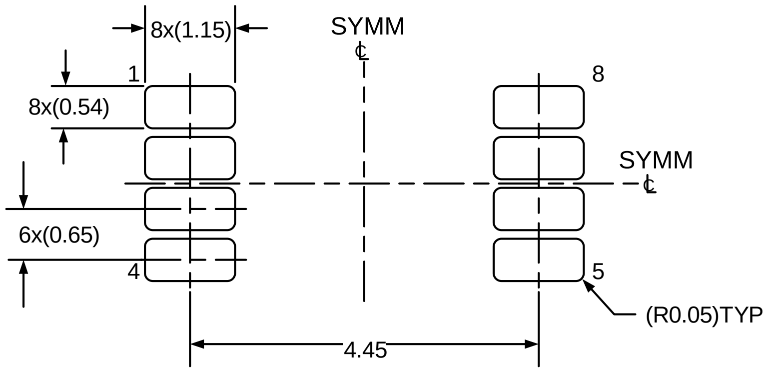
SOIC-8L Land Pattern Example



NOTES: (continued)

1. Refer to the IPC-7351 can also help you complete the designs.
2. Exposed metal shown.
3. Drawing is 10X scale.

MSOP-8L Land Pattern Example



NOTES: (continued)

1. Refer to the IPC-7351 can also help you complete the designs.
2. Exposed metal shown.
3. Drawing is 10X scale.

9 Ordering Information

Ordering Code	Package Type	ECO Plan	Packing Type	MOQ	OP Temp(°C)
GD30CP8721NSTR-K	SOT23-5L	Green	Tape & Reel	3000	−40°C to +125°C
GD30CP8721NDTR-K	SC70-5L	Green	Tape & Reel	3000	−40°C to +125°C
GD30CP8722WETR-K	DFN2x2-8L	Green	Tape & Reel	3000	−40°C to +125°C
GD30CP8722WLTR-K	SOIC-8L	Green	Tape & Reel	4000	−40°C to +125°C
GD30CP8722WMTR-K	MSOP-8L	Green	Tape & Reel	3000	−40°C to +125°C
GD30CP8723NSTR-K	SOT23-5L	Green	Tape & Reel	3000	−40°C to +125°C
GD30CP8723NSTR-R	SOT23-5L	Green	Tape & Reel	3000	−40°C to +125°C

10 Revision History

REVISION NUMBER	DESCRIPTION	DATE
1.0	Initial release and device details	2023
1.1	Modify ambient operating temperature +85°C to +125°C	2024

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