Ultra-Small, Low-Power 1KSPS, 24-bit ADC

1 Features

- Wide supply voltage: 2.7 V to 5.5 V
- Low power consumption: 150 μA (continuous conversion mode)
- Programmable data rate: 6.25SPS to 1KSPS
- Single cycle stable
- Internal low drift voltage reference
- Internal Oscillator
- SPI interface
- Four single-ended inputs or two differential inputs
- Programmable comparator
- Operating temperature range: −40 °C to +125°C

2 Application

- Portable Instruments
- Battery voltage and current monitoring
- Temperature measurement system
- Consumer Electronics
- Factory Automation and Process Control

3 Description

GD30AD3641 device is an SPI-compatible 24-bit high-precision, low-power analog-to-digital converter (ADC) in a small MSOP-10 package.

The GD30AD3641 device integrates a low-drift voltage reference and oscillator. The GD30AD3641 also includes a programmable gain amplifier (PGA) and a digital comparator. These features, combined with a wide operating supply voltage range, make the GD30AD3641 ideal for power -constrained and space-constrained sensor measurement applications.

The GD30AD3641 can perform conversions at data rates up to 1000 samples per second (SPS). The PGA provides an input range from ±64mV to ±6.144V, enabling precise measurement of large and small signals. The GD30AD3641 has an input multiplexer (MUX) that enables two pairs of differential input measurements or four single-ended input measurements. Digital comparators can be used in the GD30AD3641 for undervoltage and overvoltage detection.

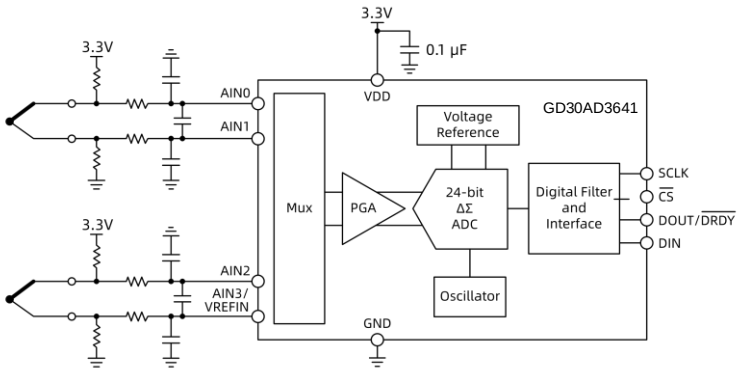
The GD30AD3641 can operate in either continuous conversion mode or single-shot mode. In single-shot mode, these devices automatically power down after one conversion; thus significantly reducing power consumption during idle periods.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
GD30AD3641	MSOP-10	3.00mm x 3.00mm

1. For packaging details, see *Packaging Information* section .

Simplified Application Schematic for K- type Thermocouple Measurement



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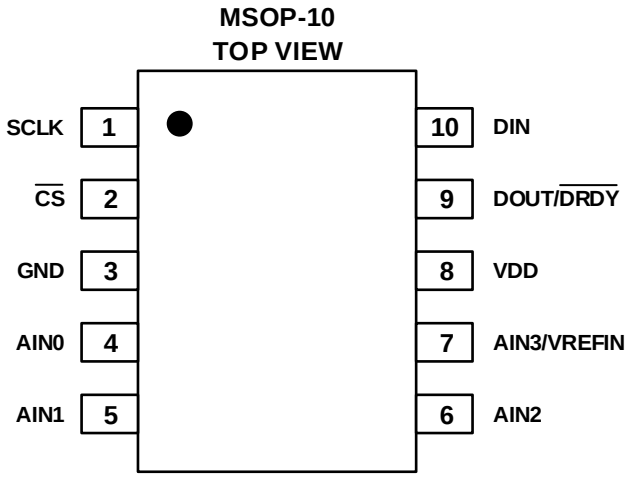
4 Device Overview

4.1 Pinout and Pin Assignment



4.2 Pin Description

PINS		PIN TYPE[1]	FUNCTION
NAME	NUM		
SCLK	1	DI	Serial clock input.
$\overline{CS}$	2	DI	Chip Select, active low, if not used, connect to GND.
GND	3	GND	Ground pin.
AIN0	4	AI	Analog Input 0. Leave it unconnected or connect to VDD if not used.
AIN1	5	AI	Analog Input 1. Leave it unconnected or connect to VDD if not used.
AIN2	6	AI	Analog Input 2. Leave it unconnected or connect to VDD if not used.
AIN3	7	AI	Analog Input 3 or Reference Input. Leave it unconnected or connect to VDD if not used.
VDD	8	P	Power supply. Connect a 100nF power supply decoupling capacitor to GND .
DOUT / $\overline{DRDY}$	9	DO	Serial data output or data ready, low level is valid.
DIN	10	DI	Serial clock input.

1. P = Power, I /O = Input/Output, DI = Digital input, DO = Digital output, AI = Analog input, GND = Ground.

5 Parameter Information

5.1 Absolute Maximum Ratings

T_A = 25° C, unless otherwise noted[1].

SYMBOL	PARAMETER	MIN	MAX	UNIT
Supply voltage	VDD to GND	− 0.3	7	V
Analog input voltage	AIN0, AIN1, AIN2, AIN3	GND − 0.3	VDD + 0.3	V
Digital input voltage	DIN, DOUT / $\overline{DRDY}$, SCLK, $\overline{CS}$	GND − 0.3	VDD + 0.3	V
Continuous input current	Any pin except the power pins	−10	1 0	mA
T_A	Operating temperature	−40	125	°C
T_J	Operating junction temperature	−40	150	°C
T_{stg}	Storage temperature	−60	150	°C

1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to maximum rated voltage conditions for extended periods may affect device reliability.

5.2 Recommended Operating Conditions

T_A = 25°C unless otherwise noted.

SYMBOL	PARAMETER	MIN	MAX	UNIT
VDD	VDD to GND	2.7	5.5	V
$V_{(AINP)} – V_{(AINN)}$ [1]	Full-scale input voltage range[2]	±0.064	±6.144	V
$V_{(AINx)}$ [1]	Analog input voltage	GND	VDD	V
V_{DIG}	Digital input voltage	GND	VDD	V
T_A	Operating temperature	−40	125	°C

1. AINP and AINN indicate the selected positive and negative inputs. AINx indicates one of the four available analog inputs.
2. This parameter represents the full-scale input voltage range of the ADC scaling. The analog inputs of the device cannot exceed VDD + 0.3V.

5.3 ESD Performance

SYMBOL	CONDITIONS	VALUE	UNIT
$V_{ESD(HBM)}$	Human-body model (HBM), ANSI/ESDA/JEDEC JS-001-2017[1]	±2000	V
$V_{ESD(CDM)}$	Charge-device model (CDM), ANSI/ESDA/JEDEC JS-002-2022[2]	±500	V

1. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing using standard ESD control processes.
2. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing using standard ESD control processes.

5.4 Thermal Resistance

SYMBOL[1]	PARAMETER	MSOP-10	UNIT
Θ_{JA}	Junction to ambient thermal resistance	182.7	°C/W
$\Theta_{JC(TOP)}$	Junction to case (top) thermal resistance	67.2	°C/W
Θ_{JB}	Junction to board thermal resistance	103.8	°C/W
Ψ_{JB}	Junction-to-Board Parameters	102.1	°C/W
Ψ_{JT}	Junction to Top Parameters	10.2	°C/W

1. Thermal resistance characteristic parameter data is based on thermal simulation results and complies with JEDEC document JESD51-7.

5.5 Technical Specifications

VDD = 3.3 V, data rate = 6.25 SPS, full-scale input voltage range (FSR) = ±2.048 V (unless otherwise noted). Maximum and minimum specifications apply from T_A = − 40 °C to +125 °C. Typical specifications are at T_A = 25 °C.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
Analog input impedance			1		GΩ
System Performance					
Resolution (no missing code)		24			Bits
Data rate (DR)		6.25, 12.5, 25, 50, 100, 250, 500, 1000			SPS
Data rate changes	All data rates	− 5		5	%
Output Noise		See the *Noise Performance* section			
Integral Nonlinearity (INL)	DR = 6.25SPS, FSR = ±2.048V[2]		10		ppm/FSR
Offset Error	FSR = ±2.048V, differential input		±30		μV
	FSR = ±2.048 V, single-ended input		±30		
Temperature offset drift	FSR = ±2.048 V		0.15		μV/°C
Gain Error[3]	FSR = ±2.048 V, T_A = 25°C		0.1	0.24	%
Gain drift over temperature[3]	FSR = ±0.256 V		1		ppm/°C
	FSR = ±2.048 V		1	5	
	FSR = ±6.144V [1]		1		
Long-term gain drift[3]	FSR = ±2.048V, T_A = 125°C, 1000hrs		±0.05		%
Gain Power Supply Rejection			40		ppm/V
Gain Match[3]	Matching between any two gains		0.02	0.1	%
Gain channel matching	A match between any two inputs		0.05	0.1	%
Common Mode Rejection Ratio (CMRR)	At DC, FSR = ±2.048V, DR = 1KSPS		125		dB
	fCM = 60Hz, DR = 6.25SPS		130		
	fCM = 50Hz, DR = 6.25SPS		130		
Power Supply Rejection Ratio (PSRR)	FSR = ±2.048V, DR = 1KSPS		109		dB

Technical Specifications (Continued)

VDD = 3.3 V, data rate = 6.25 SPS, full-scale input voltage range (FSR) = ±2.048 V (unless otherwise noted). Maximum and minimum specifications apply from T_A = − 40 °C to +125 °C. Typical specifications are at T_A = 25 °C.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
Digital Input/Output					
High level input voltage (V_{IH})		0.7VDD		VDD	V
Low level input voltage (V_{LH})		GND		0.3VDD	V
Low level output voltage (V_{OL})	I_{OL} = 3mA	GND	0.15	0.4	V
Input leakage current	GND < VDIG < VDD	−10		10	μA
Power supply					
Supply Current (I_{VDD})	Power-down mode, T_A = 25°C		0.5	2	μA
	Power-down mode			5	
	Operating mode, T_A = 25°C		150	200	
	Working Mode			300	
Power consumption (P_D)	VDD = 5.0V		0.9		mW
	VDD = 3.3V		0.5		
	VDD = 2.7V		0.3		

1. This parameter represents the full -scale range of the ADC scaling. The voltage applied to the analog input does not exceed VDD + 0.3V.
2. Best fit INL; covers 99% of full scale.
3. Includes all errors from the PGA and voltage reference.

5.6 SPI Timing Specifications

Over the operating ambient temperature range and VDD = 2.7 V to 5.5 V (unless otherwise noted).

		MIN	MAX	UNIT
t_{CSSC}	Delay time, $\overline{CS}$ falling edge to first SCLK rising edge[1]	100		ns
t_{SCCS}	Delay time, the final SCLK falling edge to $\overline{CS}$ rising edge	100		ns
t_{CSH}	Pulse duration, $\overline{CS}$ high	200		ns
t_{SCLK}	SCLK period	250		ns
t_{SPWH}	Pulse duration, SCLK high	100		ns
t_{SPWL}	Pulse duration, SCLK low[2]	100		ns
			28	ms
t_{DIST}	Setup time, DIN valid before SCLK falling edge	50		ns
t_{DIHD}	Hold time, DIN valid after SCLK falling edge	50		ns
t_{DOHD}	Hold time, SCLK rising edge to DOUT invalid	0		ns

1. If the serial bus is not shared with any other device, it $\overline{CS}$ can be pulled low permanently .
2. Holding SCLK low for more than 28 ms resets the SPI interface.

Timing requirements

SYMBOL	PARAMETER	MIN	MAX	UNIT
Propagation delay time, $\overline{CS}$ falling edge to DOUT driver	DOUT load = 20pF 100kΩ to GND		100	ns
Propagation delay time, SCLK rising edge to valid new DOUT	DOUT load = 20pF100kΩ to GND	0	50	ns
Propagation delay time, $\overline{CS}$ rising edge to DOUT high impedance	DOUT load = 20pF100kΩ to GND		100	ns

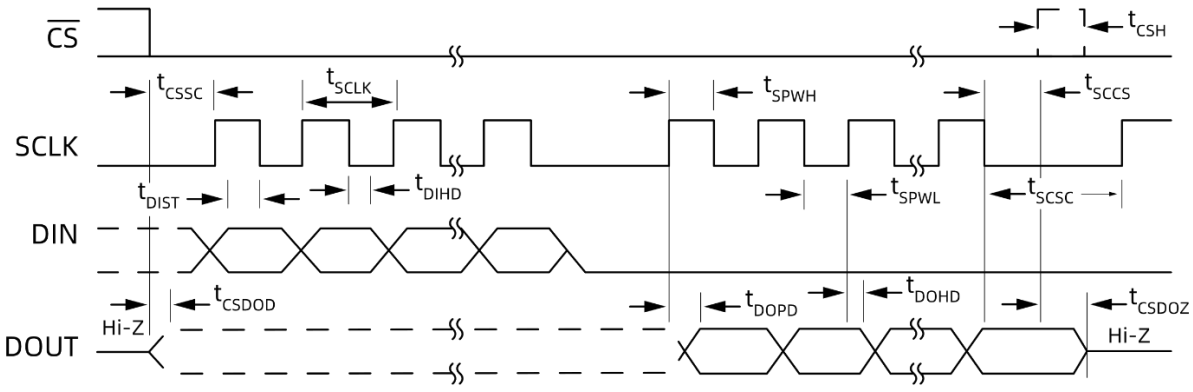


Figure 1. SPI Interface Timing

5.7 Typical Characteristics

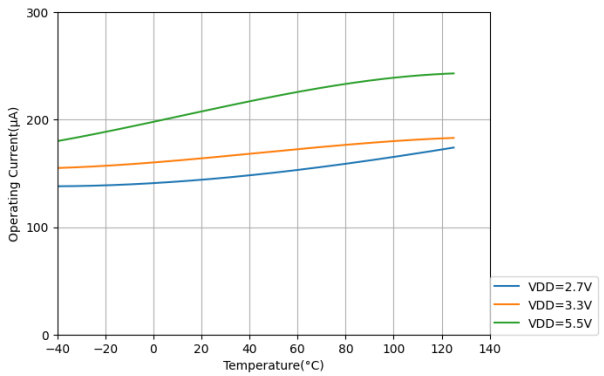


Figure 2. Operating Current vs. Temperature

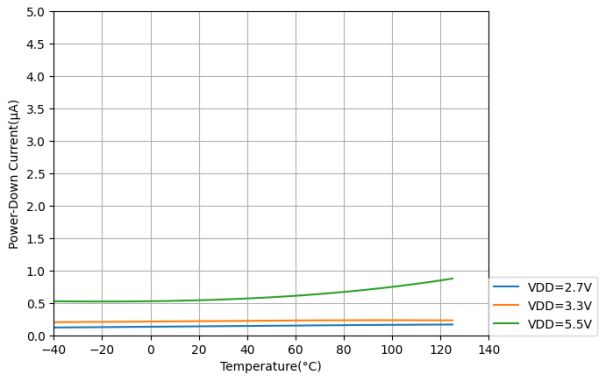


Figure 3. Power-Down Current vs. Temperature

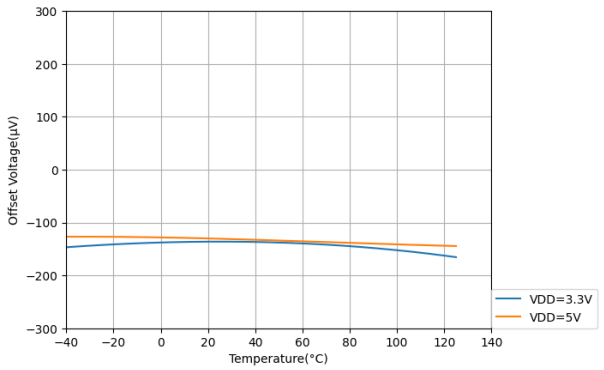


Figure 4. Offset Voltage vs. Temperature (FSR = ± 6.144V)

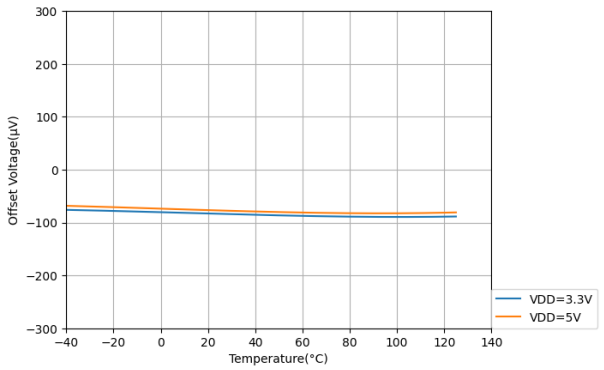


Figure 5. Offset Voltage vs. Temperature (FSR = ±4.096V)

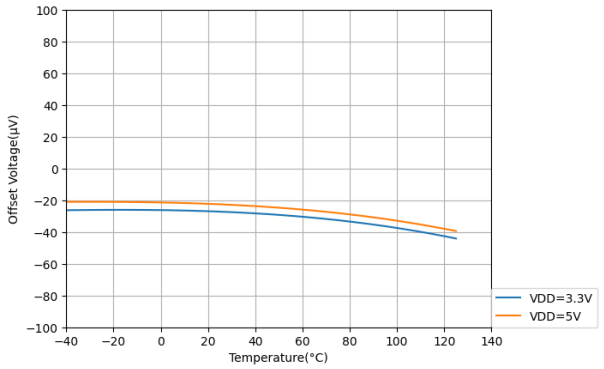


Figure 6. Offset Voltage vs. Temperature (FSR = ± 2.048V)

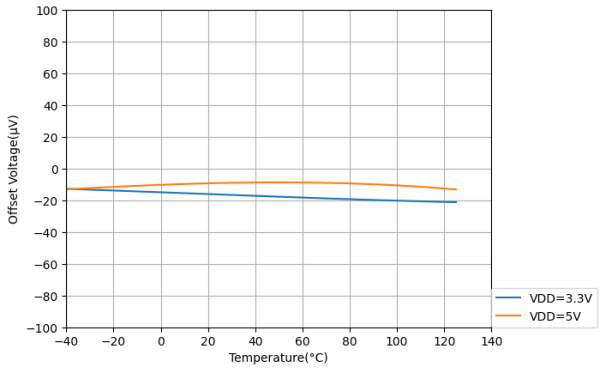


Figure 7. Offset Voltage vs. Temperature (FSR = ±1.024V)

Typical Characteristics (Continued)

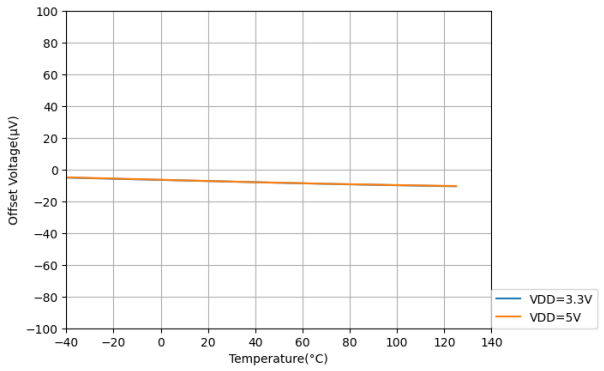


Figure 8. Offset Voltage vs. Temperature (FSR = ± 0.512V)

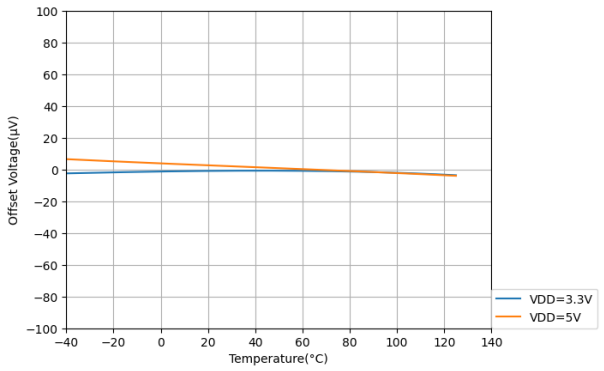


Figure 9. Offset Voltage vs. Temperature (FSR = ± 0.256V)

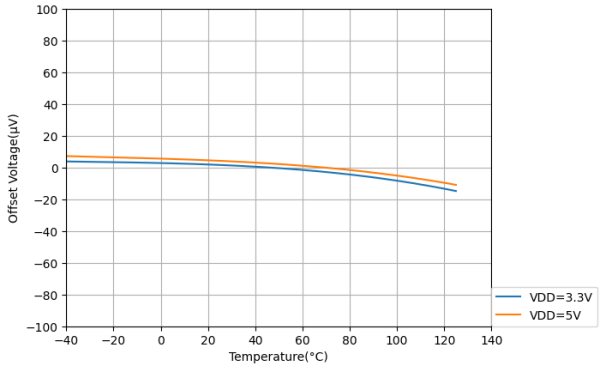


Figure 10. Offset Voltage vs. Temperature (FSR = ± 0.064V)

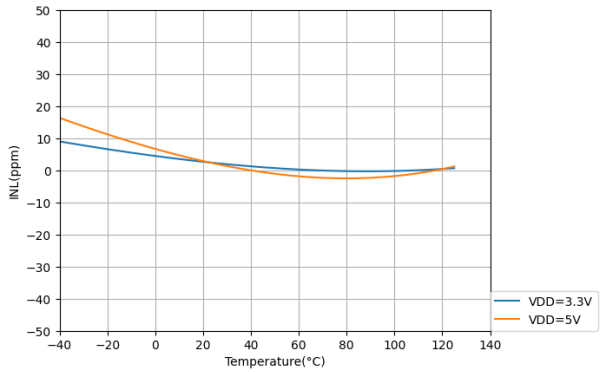


Figure 11. INL vs. Temperature (FSR = ±6.144V)

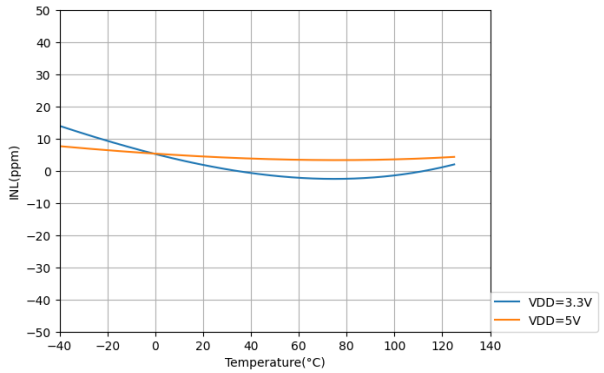


Figure 12. INL vs. Temperature (FSR = ±4.096V)

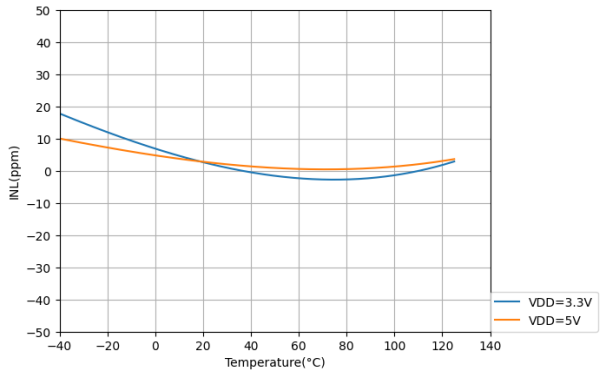


Figure 13. INL vs. Temperature (FSR = ±2.048V)

Typical Characteristics (Continued)

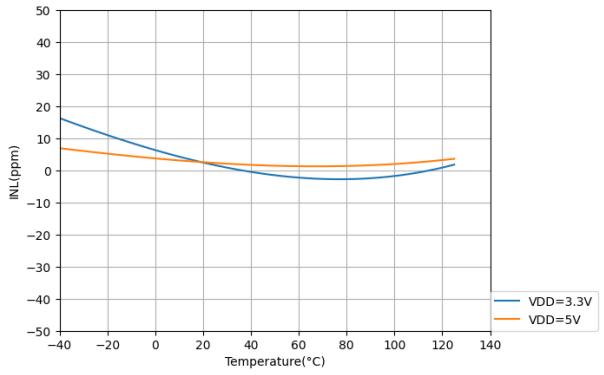


Figure 14. INL vs. Temperature (FSR = ±1.024V)

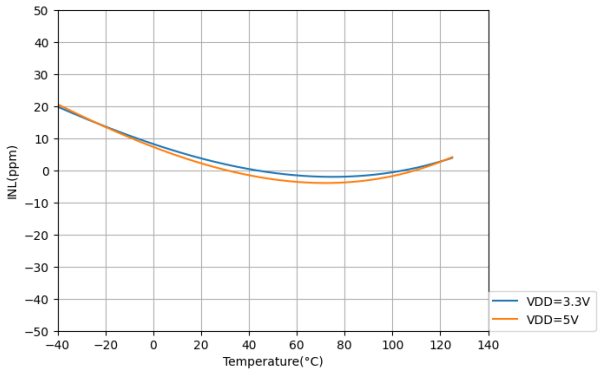


Figure 15. INL vs. Temperature (FSR = ±0.512V)

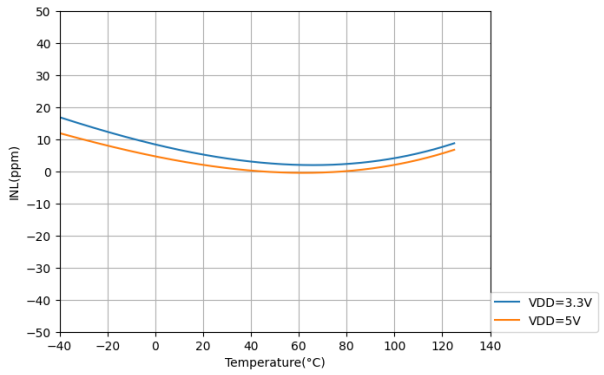


Figure 16. INL vs. Temperature (FSR = ±0.256V)

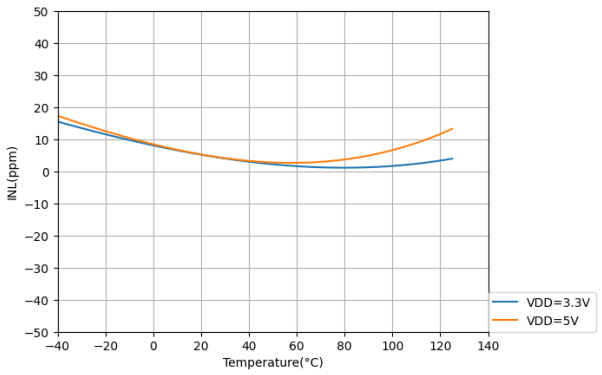


Figure 17. INL vs. Temperature (FSR = ±0.064V)

1. FSR = ±6.144 V The actual measured voltage range is ±VDD because the voltage applied to the analog input is less than VDD.
2. At VDD = 2.7 V (or 3.3 V), FSR = ±4.096 V. The actual measured voltage range is ±2.7 V (or ±3.3 V) because the voltage applied to the mode input is less than VDD.

6 Parameter Measurement Information

6.1 Noise Performance

Delta-sigma analog-to-digital converters (ADCs) are based on the principle of oversampling. The input signal to a delta-sigma ADC is sampled at a high frequency (the modulator frequency) and subsequently filtered and decimated in the digital domain to produce a conversion result at the corresponding output data rate. The ratio between the modulator frequency and the output data rate is called the oversampling ratio (OSR). By increasing the OSR, and thus reducing the output data rate, the noise performance of the ADC can be optimized. In other words, when the output data rate is reduced, the input referred noise decreases because more samples of the internal modulator are averaged to produce one conversion result. Increasing the gain can also reduce the input referred noise, which is particularly useful when measuring low-level signals.

Table 1 and Table 2 summarize the noise performance of the GD30AD3641. The data represent typical noise performance at T_A = 25 °C with the inputs shorted together externally. Table 1 shows the input referred noise in units of μVRMS for the conditions shown. Note that the μVPP values are shown in parentheses. Table 2 shows the effective resolution calculated from the μVRMS values using Equation(1). The noise-free resolution calculated from the peak-to-peak noise values using Equation(2).

$$\text{Effective Resolution} = \ln(FSR / V_{RMS\_Noise}) / \ln 2 \quad (1)$$

$$\text{Noise-Free Resolution} = \ln(FSR / V_{PP\_Noise}) / \ln 2 \quad (2)$$

Table 1. Noise in uV_{RMS} (uV_{PP}) at VDD = 3.3V

Data Rate (SPS)	FSR (Full-Scale Range)						
	±6.144 V	±4.096 V	±2.048 V	±1.024 V	±0.512 V	±0.256 V	±0.064 V
6.25	1.036 (3.662)	0.577 (2.441)	0.289 (1.465)	0.170 (0.732)	0.102 (0.488)	0.065 (0.275)	0.037 (0.183)
12.5	1.410 (8.057)	0.987 (4.883)	0.435 (2.197)	0.252 (1.343)	0.137 (0.732)	0.086 (0.458)	0.051 (0.259)
25	1.902 (11.719)	1.293 (7.813)	0.637 (3.418)	0.344 (1.953)	0.183 (0.977)	0.125 (0.763)	0.076 (0.511)
50	2.789 (17.578)	1.826 (9.766)	0.933 (5.859)	0.484 (3.052)	0.268 (1.709)	0.175 (1.099)	0.114 (0.664)
100	3.763 (24.170)	2.464 (19.043)	1.298 (7.813)	0.667 (5.127)	0.386 (2.625)	0.254 (1.678)	0.159 (1.068)
250	6.228 (44.678)	3.975 (26.367)	2.028 (14.160)	1.062 (8.057)	0.613 (5.066)	0.402 (2.716)	0.248 (1.862)
500	8.437 (61.524)	5.719 (41.016)	2.959 (20.752)	1.513 (10.864)	0.849 (6.958)	0.565 (4.333)	0.365 (2.632)
1000	12.558 (103.272)	8.544 (63.477)	4.410 (34.180)	2.289 (20.996)	1.270 (9.277)	0.832 (6.073)	0.532 (3.777)

Table 2. Effective Resolution (Noise-Free Resolution) When VDD = 3.3V

Data	FSR (Full-Scale Range)

Rate (SPS)	±6.144 V	±4.096 V	±2.048 V	±1.024 V	±0.512 V	±0.256 V	±0.064 V
6.25	23.500 (21.678)	23.758 (21.678)	23.756 (21.415)	23.522 (21.415)	23.265 (21.000)	22.915 (20.830)	21.725 (19.415)
12.5	23.055 (20.541)	22.985 (20.678)	23.167 (20.830)	22.955 (20.541)	22.837 (20.415)	22.500 (20.093)	21.264 (18.913)
25	22.623 (20.000)	22.595 (20.000)	22.617 (20.193)	22.507 (20.000)	22.414 (20.000)	21.963 (19.356)	20.688 (17.934)
50	22.071 (19.415)	22.097 (19.678)	22.066 (19.415)	22.014 (19.356)	21.868 (19.193)	21.478 (18.830)	20.103 (17.557)
100	21.639 (18.956)	21.665 (18.715)	21.589 (19.000)	21.551 (18.608)	21.340 (18.574)	20.941 (18.219)	19.617 (16.871)
250	20.912 (18.069)	20.975 (18.245)	20.946 (18.142)	20.879 (17.956)	20.673 (17.625)	20.280 (17.524)	18.977 (16.069)
500	20.474 (17.608)	20.450 (17.608)	20.401 (17.591)	20.368 (17.524)	20.203 (17.167)	19.791 (16.850)	18.418 (15.570)
1000	19.900 (16.860)	19.871 (16.978)	19.825 (16.871)	19.771 (16.574)	19.621 (16.752)	19.231 (16.363)	17.877 (15.049)

7 Detailed Description

7.1 Module Block Diagram

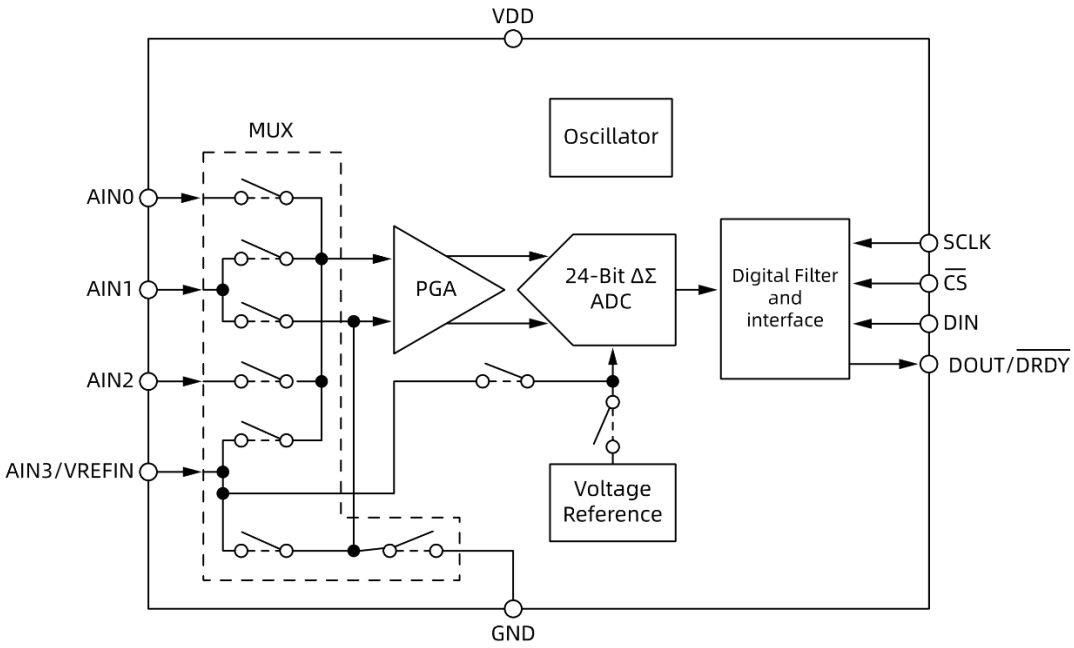


Figure 18. GD30A3641 Block Diagram

7.2 Operation

7.2.1 Overview

The GD30AD3641 is a very small, low-power 24-bit delta-sigma analog-to-digital converter (ADC). The GD30AD3641 contains a delta-sigma ADC core with an internal voltage reference, a clock oscillator, and an SPI interface. The GD30AD3641 also integrates a programmable gain amplifier (PGA) and a programmable digital comparator. Figure 18 shows the functional block diagram of the GD30AD3641.

GD30AD3641 ADC core measures the differential signal VIN, which is the difference between V(AINP) and V(AINN). The converter core consists of a differential switched capacitor delta-sigma modulator and a digital filter. The input signal is compared with an internal reference voltage. The digital filter receives a high-speed bit stream from the modulator and outputs data proportional to the input voltage.

The GD30AD3641 has two available conversion modes: single mode and continuous conversion mode. In single mode, the ADC performs one conversion on the input signal upon request, stores the conversion value to the internal conversion register, and then enters a power-down state. This mode is designed to provide significant power savings for systems that only require periodic conversions or have a long idle time between conversions. In continuous conversion mode, the ADC automatically starts conversion of the input signal as soon as the previous conversion is completed. The rate of continuous conversion is equal to the programmed data rate. Data can be read at any time and reflects the completed conversion in real time.

7.3 Features

7.3.1 Multiplexer

The GD30AD3641 contains an input multiplexer (MUX), as Figure 19 shown. Four single-ended signals or two differential signals can be measured. In addition, AIN0 and AIN1 may be measured differentially with AIN3. The multiplexer is configured by the MUX[2:0] bits in the Config register. When measuring single-ended signals, the negative input of the ADC is connected to GND through a switch inside the multiplexer.

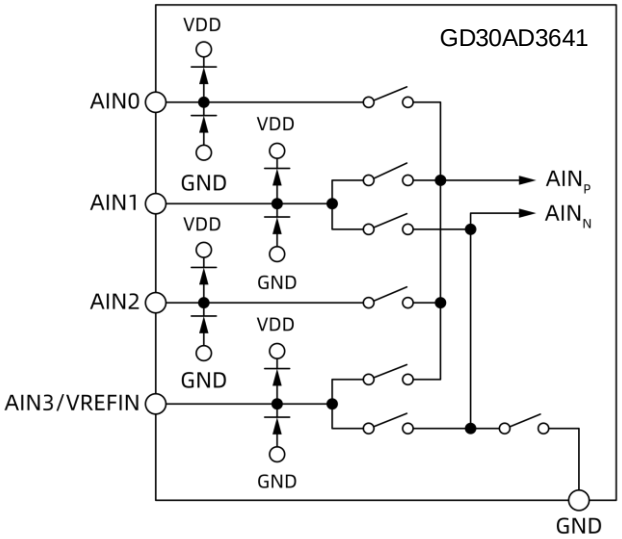


Figure 19. Input Multiplexer

When measuring single-ended inputs, the device does not output negative codes. These negative codes represent negative differential signals, that is, (V(AINP) - V(AINN)) < 0. Electrostatic discharge (ESD) diodes connected to VDD and GND protect the GD30AD3641 analog inputs. Keep the absolute voltage of any input form within the range shown in Equation (3) to prevent the ESD diodes from turning on.

$$GND - 0.3V < V_{(AINX)} < VDD + 0.3V \quad (3)$$

If the voltage on the input pin violates these conditions, use an external Schottky diode and series resistor to limit the input current to a safe value (see the *Absolute Maximum Ratings*).

7.3.2 Analog Input

The analog input has a high-impedance PGA with an impedance greater than 1GΩ . No additional driver amplifier is required.

7.3.3 Full Scale Range (FSR) and LSB Size

A programmable gain amplifier (PGA) is implemented before the delta-sigma ADC of the GD30AD3641. The full-scale range is configured by the PGA[2: 0] bits in the *Configuration Register* (Config Register) (P[1:0]=1h) [Reset = 058Bh] and can be set to ±6.144 V, ±4.096 V, ±2.048 V, ±1.024 V, ±0.512 V, ±0.256 V, ±0.064 V. Table 3 shows the FSR and the corresponding LSB size. Equation (4) shows how to calculate the LSB size from the selected full-scale range.

$$LSB = FSR / 2^{24} \quad (4)$$

Table 3. Full-Scale Range and Corresponding LSB Size

Full scale range	The size of the least significant bit
±6.144 V [1]	732n V
±4.096 V [1]	488nV
±2.048 V	244 nV
±1.024 V	122nV
±0.512 V	61 nV
±0.256 V	30.5 nV
±0.064 V	7.63nV

1. This parameter represents the full-scale range of the ADC scaling. Do not apply voltages exceeding VDD + 0.3 V to the analog inputs of the device.

The analog input voltage must not exceed the analog input voltage limits given in *Absolute Maximum Ratings*. If a VDD supply voltage greater than 4 V is used, the ± 6.144 V full-scale range allows the input voltage to extend to the supplies. Although in this case (or when the supply voltage is less than the full-scale range; for example, VDD = 3.3 V and the full-scale range = ±4.096 V), the full-scale ADC output value cannot be obtained. For example, when VDD = 3.3 V and FSR = ±4.096 V, only signals up to VIN = ±3.3 V can be measured, which in this case results in a loss of part of the measurement dynamic range.

7.3.4 Reference Voltage

GD30AD3641 integrated voltage reference. Errors associated with initial voltage reference accuracy and reference drift over temperature are included in the gain error and gain drift specifications in the electrical characteristics table.

Supports AIN3 as an external reference source.

7.3.5 Oscillator

The GD30AD3641 has an integrated oscillator that runs at 512 kHz. No external clock is required to operate these devices. The internal oscillator drifts with temperature and time. The output data rate is proportional to the oscillator frequency.

7.3.6 Output Data Rate and Conversion Time

The GD30AD3641 provides programmable output data rates. Use the DR[2:0] bits in the *Configuration Register* (Config Register) (P[1:0]=1h) [Reset = 058Bh]to select output data rates of 6.25 SPS, 12.5 SPS , 25 SPS, 50 SPS , 100 SPS, 250 SPS , 500 SPS , or 1000 SPS .

GD30AD3641 is stable within one cycle, therefore, the conversion time is equal to 1 / DR.

7.4 Functional Mode

7.4.1 Reset and Power-On

The GD30AD3641 is reset at power-on and sets all bits in the Config register to their respective default settings. The GD30AD3641 enters a power-off state after completing the reset process. The device interface and digital blocks are active, but no data conversion is performed. The initial power-off state of the GD30AD3641 can alleviate

power-critical systems from experiencing surges during power-on.

7.4.2 Operation Mode

The GD30AD3641 operates in one of two modes: continuous conversion mode or single-shot mode. The corresponding operation mode can be selected by the MODE bit in the *Configuration Register* (Config Register) (P[1:0]=1h) [Reset = 058Bh].

7.4.2.1 Single Mode

When the MODE bit in the Config register is set to 1, the GD30AD3641 enters a power-down state and operates in single-shot mode. This power-down state is the default state when the GD30AD3641 is first powered on. The device will respond to commands despite being powered off. The GD30AD3641 will remain in this power-down state until a 1 is written to the operating status (OS) bit in the *Config Register*. When the OS bit is set, the device powers up in approximately 25 µs, resets the OS bit to 0, and starts a single conversion. When the data conversion is complete, the device powers down again. Writing a 1 to the OS bit while a conversion is in progress has no effect. To switch to continuous conversion mode, write a 0 to the MODE bit in the *Config Register*.

7.4.2.2 Continuous Conversion Mode

In continuous conversion mode (MODE bit set to 0), GD30AD3641 performs conversions continuously. After the conversion is completed, GD30AD3641 places the result into the conversion register and immediately starts another conversion.

When programming new configuration settings, the conversion currently in progress is completed using the previous configuration settings. Thereafter, continuous conversions using the new configuration settings begin. To switch to single conversion mode, write a 1 to the MODE bit in the configuration register or reset the device.

7.4.3 Low Power Consumption Duty Cycle

A delta-sigma ADC generally improves when the output data rate is reduced because more samples of the internal modulator are averaged to produce one conversion result. In applications where power consumption is critical, the improved noise performance at low data rates may not be necessary. For these applications, the GD30AD3641 supports duty cycles, which significantly saves power by periodically requesting high data rate readings at an effectively lower data rate. For example, the power consumption of the GD30AD3641 set by the host controller at a data rate of 1000 SPS is 1/125 of the power consumption at a data rate of 8SPS, because it only takes about 1 ms to convert at a rate of 1000 SPS and about 125 ms to convert at a rate of 8 SPS, so that 8SPS will work 124 ms more than 1000 SPS. The host controller can arbitrarily define the sampling duty cycle. The GD30AD3641 provides lower data rates and also provides improved noise performance when needed.

7.5 Programming

7.5.1 SPI Interface

The SPI-compatible serial interface consists of four signals ($\overline{CS}$, SCLK, DIN, and DOUT / $\overline{DRDY}$) or three signals (in this case $\overline{CS}$ directly connected to low level). This interface is used to read conversion data, read and write registers, and control device operation.

7.5.2 Chip Select

The chip select pin ($\overline{CS}$) selects the GD30AD3641 for SPI communication. This feature is useful when multiple devices share the same serial bus. It is held $\overline{CS}$ low during serial communication . When $\overline{CS}$ pulled high, the serial interface is reset, SCLK is ignored, and DOUT / $\overline{DRDY}$ enters a high-impedance state. In this state, DOUT / $\overline{DRDY}$ no data-ready indication is provided . In the presence of multiple devices, it must be monitored DOUT / $\overline{DRDY}$ and periodically lowered $\overline{CS}$. At this point, the pin DOUT / $\overline{DRDY}$ either immediately goes high, indicating that no new data is available, or immediately goes low, indicating that new data is present in the conversion register and can be used for transmission. New data can be transmitted at any time without worrying about data corruption. When the transmission begins, the current result is locked into the output shift register and will not change until the communication is completed. This system avoids any possibility of data corruption.

7.5.3 Serial Clock

The serial clock (SCLK) has a Schmitt trigger input and is used to clock the data in and out of the DIN and DOUT / $\overline{DRDY}$ GD30AD3641. Even though the input has hysteresis, it is recommended to keep SCLK as clean as possible to prevent glitches from accidentally moving data. If SCLK is held low for 28ms, the serial interface is reset and the next SCLK pulse starts a new communication cycle. This timeout feature can be used to resume communication when a serial interface transmission is interrupted. When the serial interface is idle, keep SCLK low.

7.5.4 Data Entry

The data input pin (DIN) is used with SCLK to send data to the GD30AD3641. The device latches data on DIN on the falling edge of SCLK. The GD30AD3641 never drives the DIN pin.

7.5.5 Data Out and Data Ready

The data out and data ready pins (DOUT / $\overline{DRDY}$ active low) are used with SCLK to read conversion and register data from the GD30AD3641. DOUT / $\overline{DRDY}$ data on the GD30AD3641 is shifted out on the rising edge of SCLK. It is also used to indicate that the conversion is complete and new data is available. When new data is ready, the pin DOUT / $\overline{DRDY}$ goes low. DOUT / $\overline{DRDY}$ can also trigger the microcontroller to start reading data from the GD30AD3641. In continuous conversion mode, if no data is read from the device , DOUT / $\overline{DRDY}$ goes high again 8μs before the next data ready signal (DOUT / $\overline{DRDY}$ active low). This transition is shown in the figure below. The data transfer is completed before DOUT / $\overline{DRDY}$ returning high.

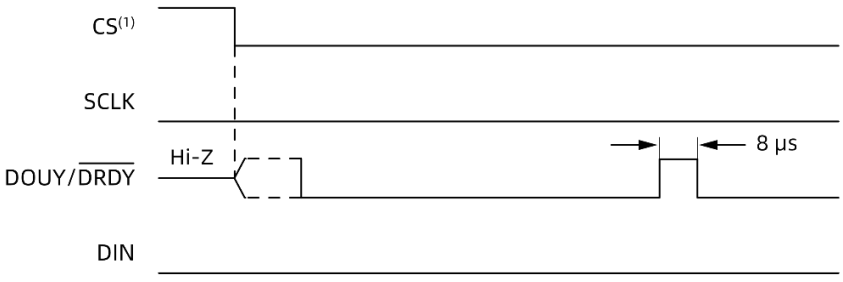


Figure 20. Schematic Diagram of Continuous Conversion Mode without Data Reading DOUT / $\overline{DRDY}$

When $\overline{CS}$ high, the default configuration of DOUT / $\overline{DRDY}$ has a weak internal pull-up resistor. This feature reduces the risk of DOUT / $\overline{DRDY}$ floating near the middle of the supply and causing leakage current in the master device . To disable this pull-up resistor and put the device in a high-impedance state, set the PULL_UP_EN bit in the *Config Register* to 0.

7.5.6 Data Format

The GD30AD3641 provides 24-bit data in two's complement format. A positive full-scale (+FS) input produces an output code of 7FFFFFh, and a negative full-scale (–FS) input produces an output code of 800000h. For signals

exceeding full-scale, data up to full-scale is displayed. Table 4 summarizes the ideal output codes for different input signals. The following figure shows the relationship between code transition and input voltage.

Table 4. Input Signals and Ideal Output Codes

Input Signal ($V_{INAINPAINN}$)	Ideal output code[1]
≥ +FS ($2^{23} - 1$)/2^{23}	7FFFFF
+FS/2^{23}	000001h
0	000000h
–FS/2^{23}	FFFFFFh
≤ –FS	800000h

1. Does not include the effects of noise, INL, offset, and gain errors.

7.5.7 Data Reading

For single and continuous conversion modes, data is written and read from the GD30AD3641 in the same way, without issuing any commands. The operating mode of the GD30AD3641 is selected by the MODE bit in the *Config Register*.

The device can be placed in continuous conversion mode by setting the MODE bit to 0. In continuous conversion mode, the device $\overline{CS}$ continuously initiates new conversions even when OUT is high .

For single-shot mode, set the MODE bit to 1. In single-shot mode, a new conversion is started simply by writing a 1 to the SS bit. Conversion data is always buffered, and the current data is retained until it is replaced by new conversion data. Therefore, data can be read at any time without worrying about data corruption. When DOUT / $\overline{DRDY}$ set low, it indicates that new conversion data is ready, and the conversion data is read by shifting the data out. The MSB (23rd bit) of the data upper in the DOUT / $\overline{DRDY}$ is output on the first SCLK rising edge. While the conversion result is being output from the DOUT / $\overline{DRDY}$, the new configuration register data is latched onto DIN on the SCLK falling edge.

GD30AD3641 also offers the possibility to directly read back the configuration register settings within the same data transfer cycle. A complete data transfer cycle consists of 32 bits (when using *Config Register* data readback) or 24 bits (only used when the line can be controlled and is not permanently pulled low).

7.5.8 48-bit Data Transfer Cycle - 24-bit ADC Data

48-bit data transmission contains 6 bytes. The first 3 bytes of DOUT are 24-bit ADC data. The optional last 3 bytes are the value of the read register. The register is 16 bits wide and is output in the last two bytes. The upper 8 bits are always zero.

The DIN data high 8 bits input 0. The low 16 bits input the value to be written to the register. If the input is always 0, no data is written. The write register sequence [2:1] bits are 01, indicating that the write is valid, otherwise the write is invalid.

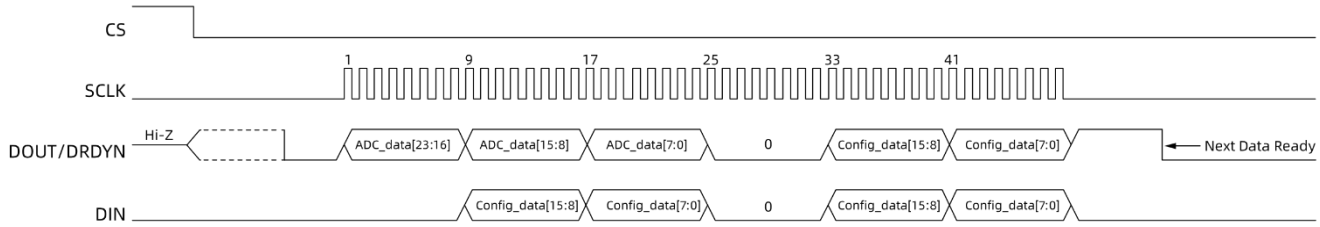


Figure 21. 24-Bit Data Transfer Cycle-Configuration Register

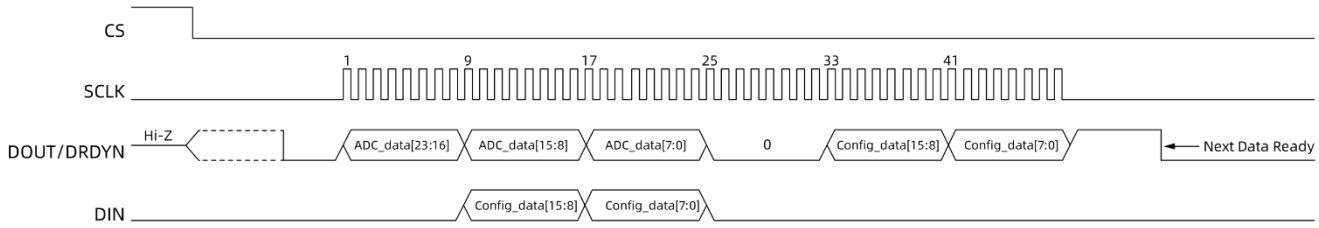


Figure 22. 24-Bit Data Transfer Cycle DIN Remains Low

7.5.9 24-bit Data Transfer Cycle-24 bit ADC Data

The 24-bit data transmission mode is similar to the 7.5.9, the difference is that ADC data format is 24 bits . The *Config Register* data is written in the lower 16 bits of DIN. If Din is all 0, it is not written. The write register sequence [2:1] bits are 01 to indicate that the write is valid, otherwise the write is invalid.

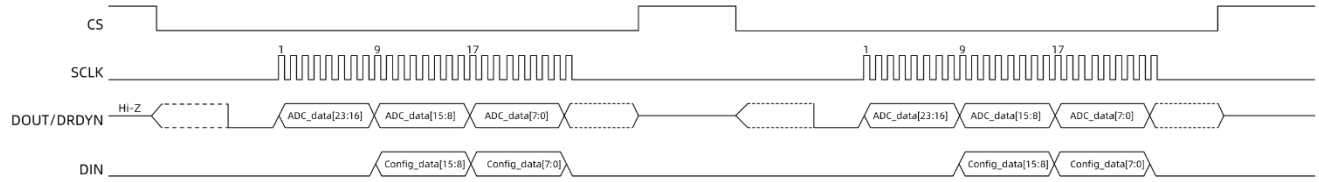


Figure 23. 24-Bit Data Transfer Cycle

7.5.10 Reset ADC

Sending specific data via SPI can reset the ADC, as shown in the following table. $\overline{CS}$ Sending the following data during the low level period can reset the entire chip. After the software reset command is executed, wait for 1ms before operating the ADC again.

MSB					LSB
0x8100	0x0012	0xACCA	0x8100	0x0014	0x0002

1. Before sending the above data, it is recommended to pull up CS to reset the SPI interface to ensure that the command is written effectively.

7.6 Register Map

The GD30AD3641 has two registers that can be accessed through the SPI interface using the address pointer register. The conversion register contains the result of the last conversion. The configuration register is used to change the operating mode of the GD30AD3641 and query the status of the device.

7.6.1 Conversion Register (P[1:0]=0h) [Reset=0000h]

The 24-bit conversion register contains the result of the last conversion in two's complement format. After power-up, the conversion register is cleared to 0 and remains at 0 until the first conversion is completed.

Table 5. Conversion Registers

23	22	21	20	19	18	17	16
D 23	D22	D21	D20	D19	D18	D17	D16
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
D15	D14	D13	D12	D11	D10	D9	D8
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
D7	D6	D5	D4	D3	D2	D1	D0
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Example: RW = read and write; R = read only; -n = reset value

Table 6. Conversion Register Field Description

Bit	Field	Type	Reset	Description
23:0	D[23:0]	R	000000h	24-bit conversion result

7.6.2 Configuration Register (Config Register) (P[1:0]=1h) [Reset = 058Bh]

A 24-bit configuration register controls the operating mode, input selection, data rate, full-scale range, and comparator mode.

Table 7. Configuration Registers

15	14	13	12	11	10	9	8
OS	MUX[2:0]			PGA[2:0]			MODE
R/W-0h	R/W-0h			R/W-2h			R/W-1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DR[2:0]			Reserved	PULL_UP_EN	N OP[1:0]		Reserved
R/W-4h			R/W-0h	R/W-1h	R/W-1h		R-1h

1. Example: RW = read and write; R = read only; -n = reset value

Table 8. Address Pointer Register Field Description

Bit	Field	Type	Reset	Description
15	OS	R/W	0h	**Run state or single conversion start** This bit determines the operating state of the device. The OS can only write to it in the power-down state and has no effect while a conversion is in progress. When writing: 0 = Invalid 1 = Start single conversion (in power-down state) When reading: 0 = The device is currently performing a conversion 1 = The device is not currently performing a conversion
14:12	MUX[2:0]	R/W	0h	**Input Multiplexer Configuration** These bits configure the input multiplexer. 000 = AINP is AIN0 and AINN is AIN1 (default) 001 = AINP is AIN0 and AINN is AIN3 010 = AINP is AIN1 and AINN is AIN3 011 = AINP is AIN2 and AINN is AIN3 100 = AINP is AIN0 and AINN is GND 101 = AINP is AIN1 and AINN is GND 110 = AINP is AIN2 and AINN is GND 111 = AINP is AIN3 and AINN is GND
11:9	PGA[2:0]	R/W	2h	**Programmable Gain Amplifier Configuration** These bits set the FSR of the programmable gain amplifier. 000 = FSR = ±6.144V 001 = FSR = ±4.096V 010 = FSR = ±2.048V (default) 011 = FSR = ±1.024V 100 = FSR = ±0.512V 101 = FSR = ±0.256 V 110 = FSR = ±0.064V
8	MODE	R/W	1h	**Device operation mode** This bit controls the operating mode of GD30AD3641. 0 = Continuous conversion mode 1 = Power-down and one-shot mode (default)
7:5	DR[2:0]	R/W	4h	**Data Rate** These bits control the data rate setting. 000 = 6.25SPS 001 = 12.5SPS 010 = 25SPS 011 = 50SPS 100 = 100SPS (default) 101 = 250SPS

Bit	Field	Type	Reset	Description
				110 = 500SPS 111 = 1000SPS
4	Reserved	R/W	0h	**Reserved** Writing 0 or 1 to this bit has no effect.
3	PULL _UP_EN	R/W	1h	DOUT / $\overline{DRDY}$ **Pin pull-up function enable bit** When high DOUT / $\overline{DRDY}$ only , this bit enables $\overline{CS}$ the weak internal pull-up resistor on the pin. When enabled, the internal 400kΩ resistor connects the bus line to the supply . When disabled , DOUT / $\overline{DRDY}$ the pin floats. 0 = Disable pull-up resistor on DOUT / $\overline{DRDY}$ pin 1 = Enable pull-up resistor on pin DOUT / $\overline{DRDY}$ (default)
2:1	NOP[1:0]	R/W	1h	**No Operation** The NOP [1:0] bits control whether data is written to the configuration register. For data to be written to the configuration register, the NOP[1:0] bits must be “01” . Any other value results in a NOP command. DIN can be held high or low during the SCLK pulse without data being written to the configuration register. 00 = Invalid data, do not update the contents of the Config register 01 = valid data, update Config register (default) 10 = Invalid data, do not update the contents of the Config register 11 = Invalid data, do not update the content configuration register
0	Reserved	R	1h	**Reserved** Writing 0 or 1 to this bit has no effect.

1. This parameter represents the full-scale range of the ADC scaling. Do not apply voltages exceeding VDD+0.3V to the ADC.

8 Application and Implementation

Example circuits and suggestions for using the GD30AD3641 in various situations.

8.1 SPI Basic Connection

SPI basic connection is shown in Figure 24:

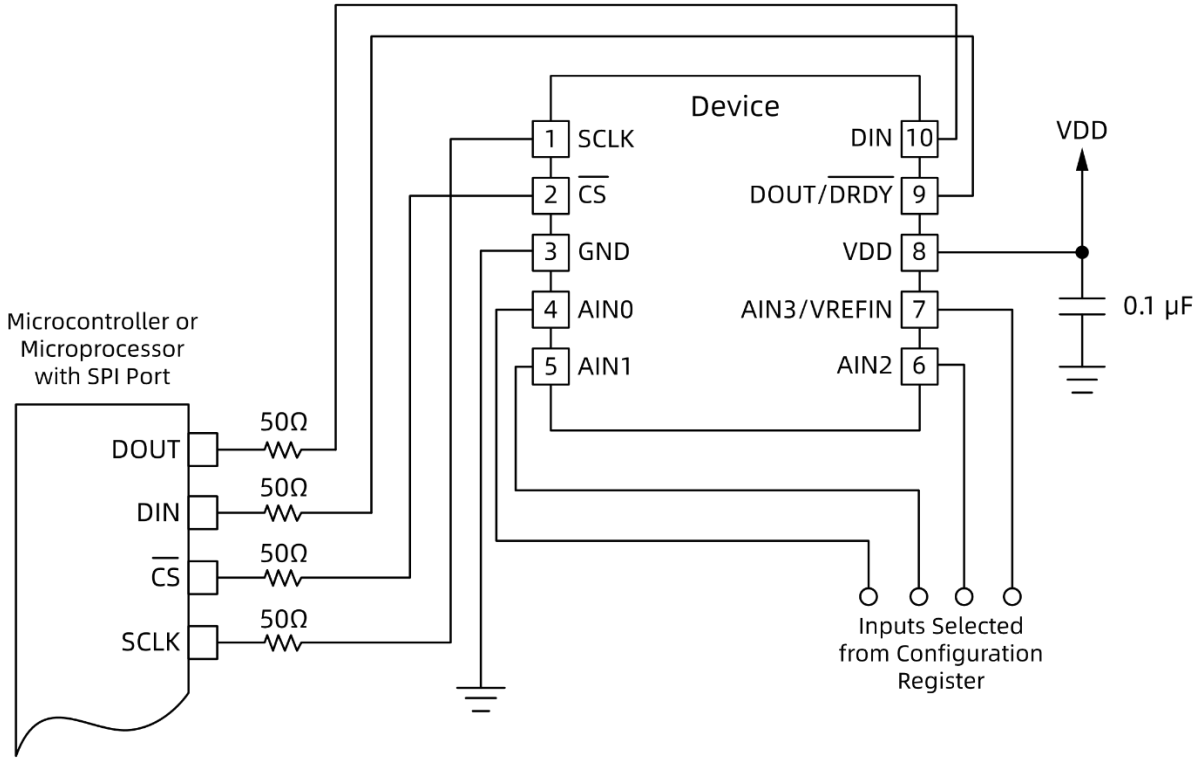


Figure 24. Typical Connections for GD30AD3641

Most microcontroller SPI peripherals can be used with the GD30AD3641. The interface operates in SPI Mode 1, where CPOL = 0 and CPHA = 1. In SPI mode, SCLK idles low and data is initiated or changed only on the rising edge of SCLK; data is latched or read by the master and slave on the falling edge of SCLK. Details can be found in the *SPI Timing Specifications*.

50Ω resistors in series with the series path of each data pin to provide some short circuit protection. Care must be taken to still meet all SPI timing requirements as these additional series resistors along with the bus parasitic capacitance present on the digital signal lines may alter the signal.

The GD30AD3641 are ideal for connecting to differential sources with moderately low source impedance (such as thermocouples and thermistors). Although the GD30AD3641 can read fully differential signals, the device cannot accept negative voltages on either input due to the presence of ESD protection diodes on each pin. When the inputs exceed the supplies or drop below ground, these diodes turn on to prevent any ESD damage to the device.

8.1.1 GPIO Ports for Communication

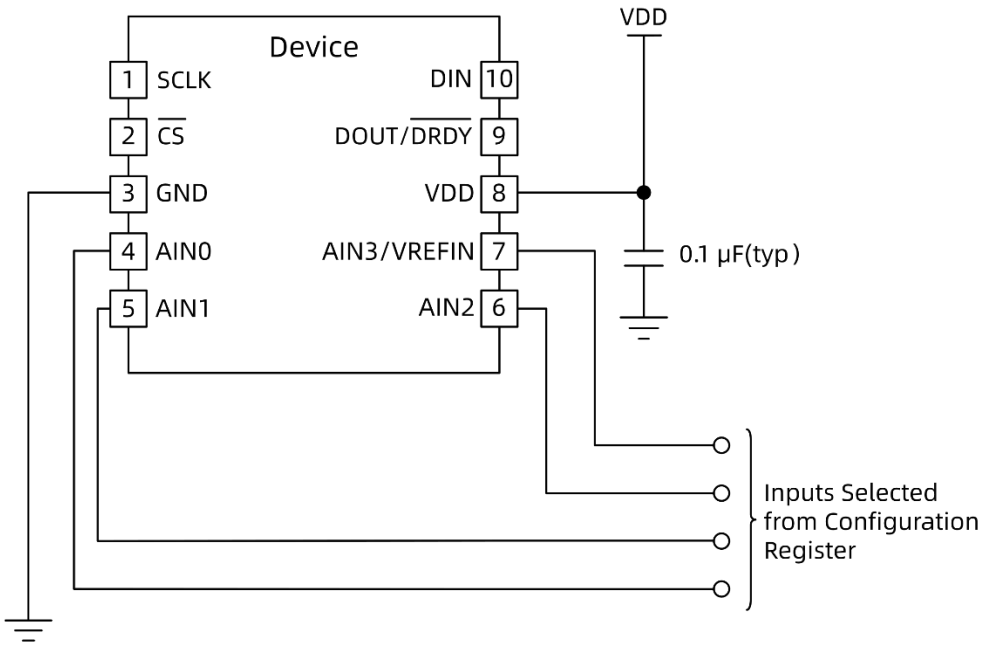
Most microcontrollers have programmable input and output IO pins that can be set as input or output in software.

If an SPI controller is not available, the GD30AD3641 can be connected to the GPIO pins and the SPI bus pins can simulate the protocol. Use the GPIO pins to generate SPI configured as push or pull input or output. If the SCLK low level exceeds 28 ms, the communication times out. This situation means that the GPIO port must be able to provide SCLK pulses with no more than 28 ms between pulses.

8.2 Single-Ended Input

The GD30AD3641 can measure up to four single-ended signals. The GD30AD3641 measures single-ended signals by appropriately configuring the MUX[2:0] bits in the *Config Register*. Figure 25 shows the single-ended connection scheme for the GD30AD3641. The single-ended signal range is from 0V to the positive supply or +FS, whichever is lower. Negative voltages cannot be applied to these devices because the GD30AD3641 can only accept positive voltages relative to ground. The GD30AD3641 does not lose linearity over the input range.

The GD30AD3641 provides a differential input voltage range of ±FSR. The single-ended configuration uses only one-half of the full-scale input voltage range. The differential configuration maximizes the dynamic range of the ADC and provides better common-mode noise rejection than the single-ended configuration.



NOTE: Digital pin connections omitted for clarity.

Figure 25. Measuring Single-Ended Input

The GD30AD3641 also allows AIN3 to be used as a common point for measurements by setting the MUX[2:0] bits appropriately. AIN0, AIN1, and AIN2 can all be measured relative to AIN3. In this configuration, the GD30AD3641 operates with inputs where AIN3 is used as a common point. This capability increases the usable range allowed, GND < V(AIN3) < VDD.

8.3 Input Protection

The GD30AD3641 is manufactured using a small footprint, low voltage process. The analog inputs have protection diodes connected to the power rails. However, the current handling capability of these diodes is limited, and the GD30AD3641 may be permanently damaged by analog input voltages exceeding approximately 300mV. One way

to prevent overvoltage is to place current limiting resistors on the input lines. The GD30AD3641 analog inputs can withstand up to 10mA of continuous current.

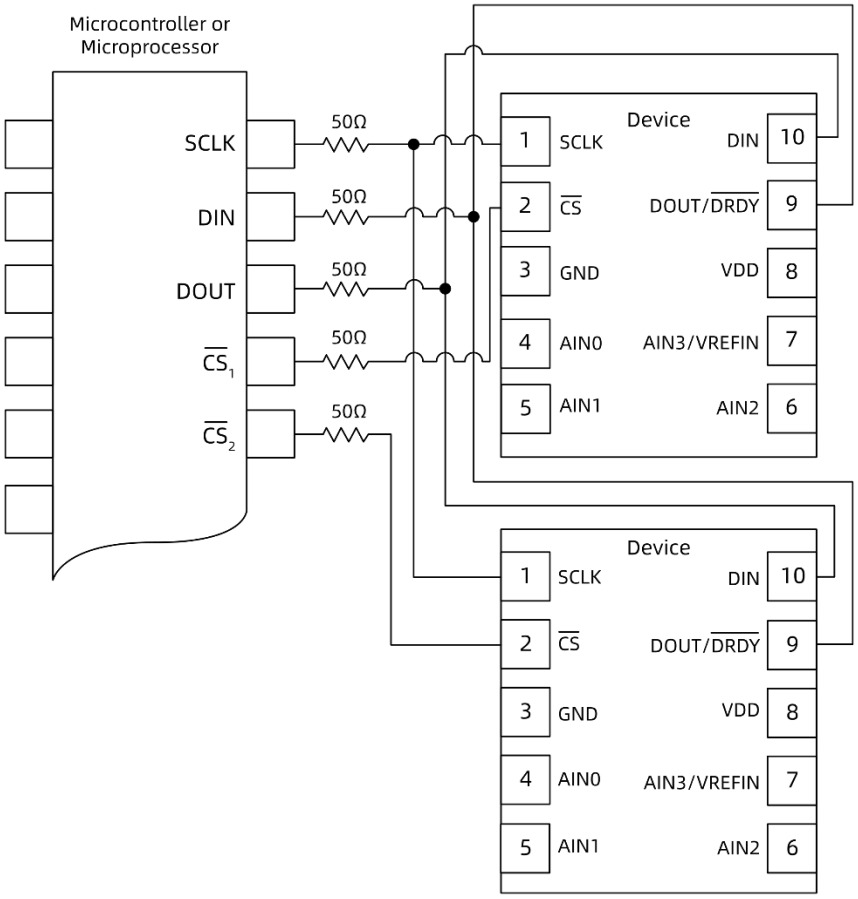
8.4 Unused Inputs and Outputs

Leave unused analog inputs floating, or connect unused analog inputs to midsupply or VDD. You can connect unused analog inputs to GND, but higher leakage current may result.

Leave the NC (not connected) pin unconnected, or connect the NC pin to GND. If the ALERT/RDY output pin is not used, leave it unconnected or connect it to VDD using a weak pull-up resistor.

8.5 Connecting Multiple Devices

Multiple GD30AD3641 devices to a single SPI bus, SCLK, DIN, and OUT can be safely shared DOUT / $\overline{\text{DRDY}}$ by using a dedicated chip select ($\overline{\text{CS}}$) for each SPI-capable device. By default, when $\overline{\text{CS}}$ goes high on the GD30AD3641 , DOUT / $\overline{\text{DRDY}}$ is pulled up to VDD by a weak pull-up resistor. This feature is intended to prevent DOUT / $\overline{\text{DRDY}}$ OUT from floating near mid-rail and causing excessive current leakage on the microcontroller inputs. If the PULL_UP_EN bit in the *Config Register* is set to 0, DOUT / $\overline{\text{DRDY}}$ enters tri-state mode when $\overline{\text{CS}}$ transitions high. When $\overline{\text{CS}}$ OUT is high, the GD30AD3641 cannot issue a data ready pulse on DOUT / $\overline{\text{DRDY}}$. To assess when the GD30AD3641 is ready for a new conversion when using multiple devices , the master device can periodically pull $\overline{\text{CS}}$ to low. When $\overline{\text{CS}}$ goes low, DOUT / $\overline{\text{DRDY}}$ is immediately driven high or low. If DOUT / $\overline{\text{DRDY}}$ is driven low when $\overline{\text{CS}}$ is low, new data is currently available for clocking out at any time. If DOUT / $\overline{\text{DRDY}}$ is driven high, no new data is available and the GD30AD3641 returns the last conversion result. Valid data can be read from the GD30AD3641 at any time without fear of data corruption. If a new conversion is available during a data transfer, that conversion is not available for readback until a new SPI transfer is initiated.



NOTE: GD30AD3641 power and input connections omitted for clarity.

Figure 26. Connecting Multiple GD30AD3641 Devices

9 Power Supply Recommendations

The device requires a unipolar power supply, VDD, to power the analog and digital circuits of the device.

9.1 Power Supply Timing

Wait approximately 50μs after VDD stabilizes before communicating with the device to complete the power-on reset process.

9.2 Power Supply Decoupling

Good power supply decoupling is important to achieve optimal performance. VDD must be decoupled using at least a 0.1 μF capacitor as shown in Figure 27. The 0.1μF bypass capacitor provides the instantaneous burst of additional current required from the power supply when the device is switching. Place the bypass capacitor as close as possible to the device's power pins using low impedance connections. Use multilayer ceramic chip capacitors (MLCCs) with low equivalent series resistance (ESR) and inductance (ESL) characteristics for power supply decoupling. For very sensitive systems or systems in harsh noisy environments, avoid using vias to connect capacitors to device pins to improve noise immunity. If vias must be used to connect capacitors to device pins, it is recommended to use multiple vias in parallel to reduce the overall inductance.

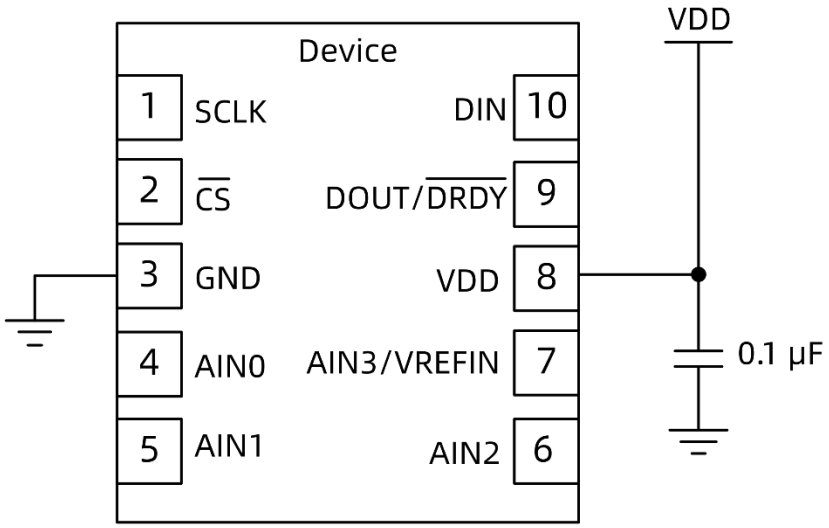


Figure 27. GD30AD3641 Power Supply Decoupling

10 Layout

10.1 Layout Guide

Employ best design practices when laying out the printed circuit board (PCB) for analog and digital components. For optimal performance, separate analog components [such as ADCs, amplifiers, references, digital-to-analog converters (DACs), and analog MUXs] from digital components [such as microcontrollers, complex programmable logic devices (CPLDs), field programmable gate arrays (FPGAs), radio frequency (RF) transceivers, universal serial bus (USB) transceivers, and switching regulators]. Figure 28 shows an example of good component placement. While Figure 28 provides a good example of component placement, the optimal placement for each application depends on the geometry, components, and PCB manufacturing capabilities employed. That said, no one layout will work perfectly for every design, and careful consideration must always be made when designing with any analog component.

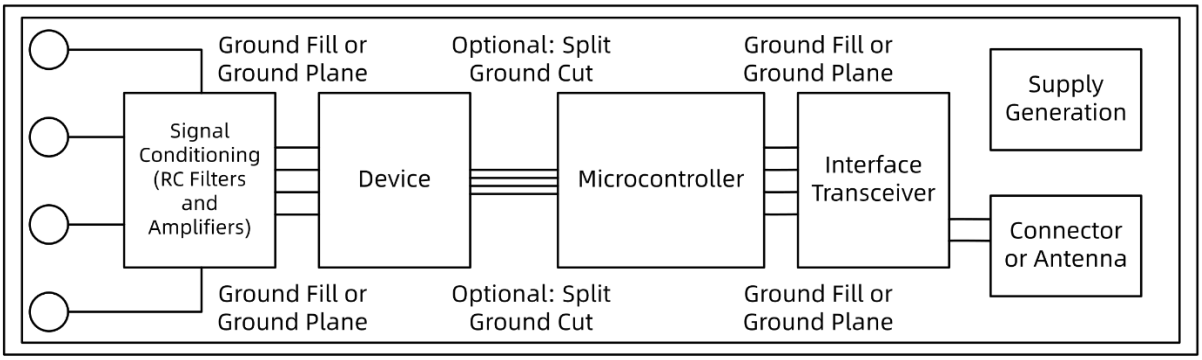


Figure 28. System Component Placement

Outlined below are some basic recommendations for the GD30AD3641 layout to get the best performance from the ADC. A good design can be ruined by poor circuit layout.

Separate analog and digital signals. First, divide the board into analog and digital sections as the layout allows. Keep digital lines away from analog lines. This prevents digital noise from coupling back into the analog signals.

Fill empty areas on signal layers with ground.

Provide a good ground return path. Signal return current flows on the path of least impedance. If the ground plane is cut or there are other traces preventing current from flowing next to the signal trace, it must find another path to return to the source and complete the circuit. If it is forced into a larger path, it increases the chance of signal radiation. Sensitive signals are more susceptible to EMI interference.

Use bypass capacitors on the power supplies to reduce high frequency noise. Do not place vias between the bypass capacitors and active devices. Placing bypass capacitors on the same layer close to active devices yields the best results.

Consider the resistance and inductance of the wiring. In general, the resistance of the input trace reacts with the input bias current and causes additional error voltage. Reduce the loop area enclosed by the source signal and return current to reduce the inductance in the path. Reduce inductance to reduce EMI pickup and reduce the high-frequency impedance seen by the device.

The two inputs going into the measurement source must be matched differential inputs.

Analog inputs with differential connections must place a capacitor at the input differentially. The best input combination for differential measurements uses adjacent analog input lines, such as AIN0, AIN1 and AIN2, AIN3. The differential capacitor must be of high quality. The best ceramic chip capacitor is C0G (NPO), which has stable characteristics and low noise characteristics.

10.2 Layout Examples

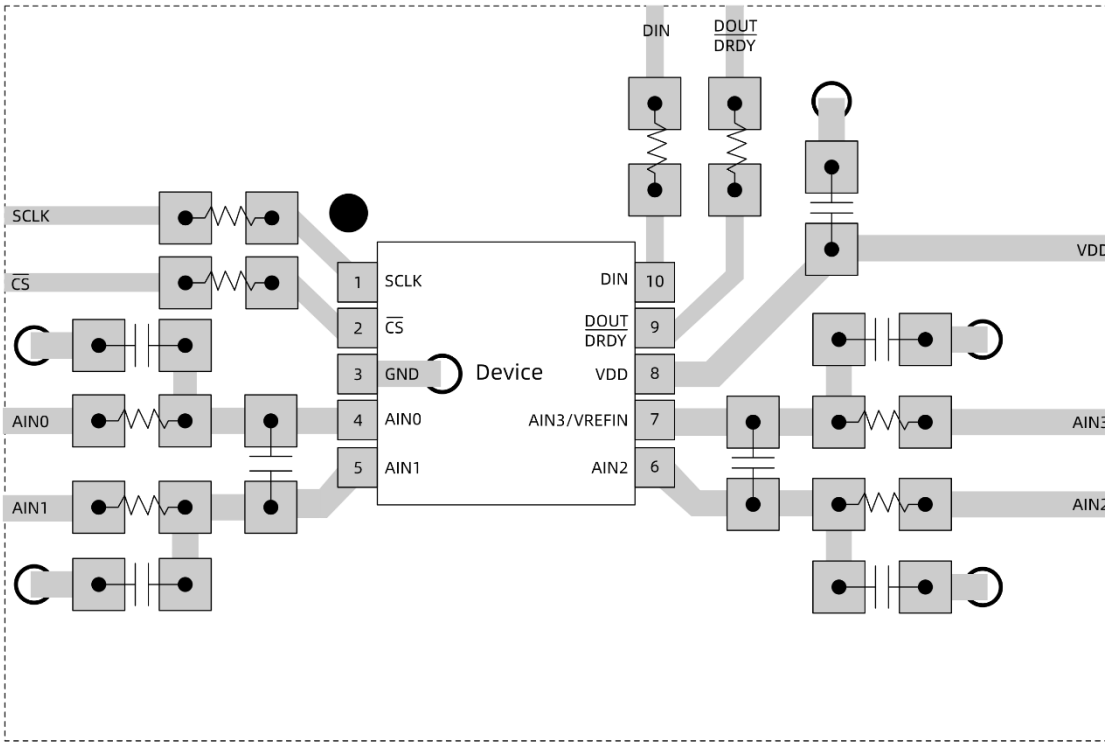
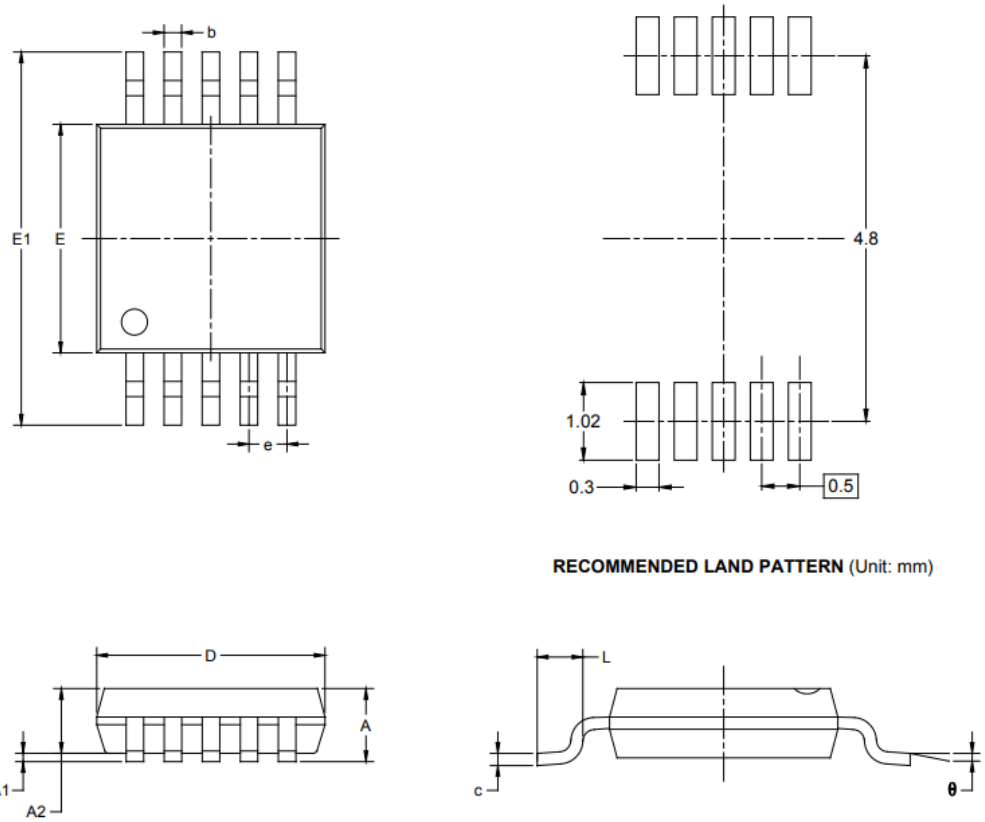


Figure 29. GD30AD3641 MSOP-10 Package

11 Packaging Information

11.1 Outline Dimensions

MSOP-10 Package



Note :

1. All dimensions are in millimeters.
2. Package dimensions does not include mold flash, protrusions, or gate burrs.
3. Refer to Table 9. MSOP-10 *Dimensions (mm).*

Table 9. MSOP-10 Dimensions (mm)

SYMBOL	MIN	NOM	MAX
A	0.820		1.100
A1	0.020		0.150
A2	0.750		0.950
b	0.180		0.280
c	0.090		0.230
D	2.900		3.100
E	2.900		3.100
E1	4.750		5.050
e	0.500 BSC		
L	0.400		0.800
θ	0°		6°

12 Ordering Information

Ordering Code	Package Type	ECO Plan	Packing Type	MOQ	OP Temp(°C)
GD30AD3641AMTR-I	MSOP10	Green	Reel	3000	−40°C to +125°C

13 Revision History

REVISION NUMBER	DESCRIPTION	DATE
1.0	Initial release and device details	2023

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