Ultra-Small, Low-Power 1KSPS, 24-bit ADC

1 Features

- Wide supply voltage: 2.7 V to 5.5 V
- Low power consumption: 150uA (continuous conversion mode)
- Programmable data rate: 6.25SPS to 1KSPS
- Single cycle stable
- Internal low drift voltage reference
- Internal Oscillator
- I2C interface: four pin-selectable addresses
- Four single-ended inputs or two differential inputs
- Programmable comparator
- Operating temperature range: −40 °C to +125 °C

2 Application

- Portable Instruments
- Battery voltage and current monitoring
- Temperature measurement system
- Consumer Electronics
- Factory Automation and Process Control

3 Description

GD30AD3640 device is an I2C-compatible, 24-bit, high-precision, low-power analog-to-digital converter (ADC) in a small MSOP-10 package.

The GD30AD3640 device integrates a low-drift voltage reference and oscillator. The GD30AD3640 also includes a programmable gain amplifier (PGA) and a digital comparator. These features, combined with a wide operating supply voltage range, make the GD30AD3640 ideal for power -constrained and space-constrained sensor measurement applications.

The GD30AD3640 can perform conversions at data rates up to 1000 samples per second (SPS). The PGA provides an input range from ±64 mV to ±6.144 V, enabling precise measurement of large and small signals. The GD30AD3640 has an input multiplexer (MUX) that enables two pairs of differential input measurements or four single-ended input measurements. Digital comparators can be used in the GD30AD3640 for undervoltage and overvoltage detection.

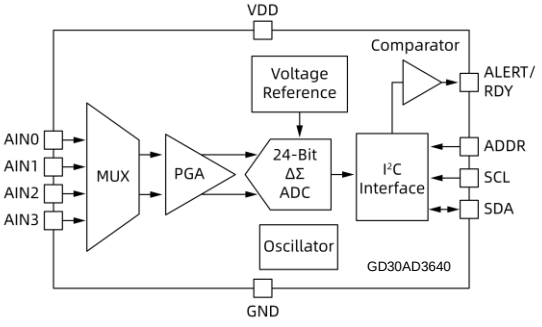
The GD30AD3640 can operate in either continuous conversion mode or single-shot mode. In single-shot mode, the devices automatically power down after one conversion; thus significantly reducing power consumption during idle periods.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
GD30AD3640	MSOP-10	3.00mm x 3.00mm

1. For packaging details, see *Packaging Information*section .

Simplified Block Diagram



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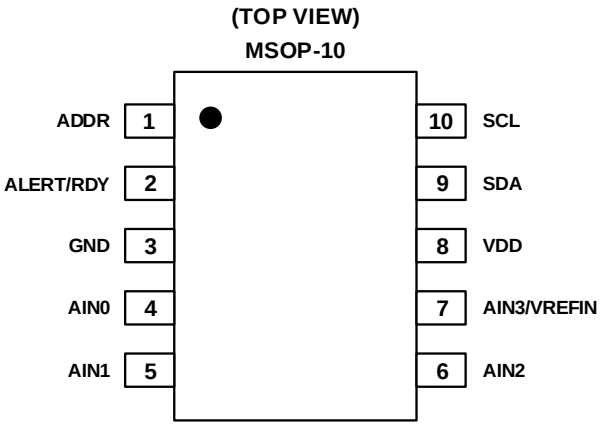
4 Device Overview

4.1 Pinout and Pin Assignment



4.2 Pin Description

PINS		PIN TYPE[1]	FUNCTION
NAME	NUM		
ADDR	1	DI	I2C slave address selection .
ALERT/RDY	2	DO	Digital comparator output or conversion complete, open-drain output.
GND	3	G	Ground.
AIN0	4	AI	Analog Input 0. Leave this pin unconnected or connect to VDD if not used.
AIN1	5	AI	Analog Input 1. Leave this pin unconnected or connect to VDD if not used.
AIN2	6	AI	Analog Input 2. Leave this pin unconnected or connect to VDD if not used.
AIN3/VREFIN	7	AI	Analog Input 3 or Reference Input. Leave this pin unconnected or connect to VDD if not used.
VDD	8	P	Power supply. Connect a 100nF power supply decoupling capacitor to GND.
SDA	9	I/O	Serial Data. Transmits and receives data .
SCL	10	D I	Serial Clock Input. Locks data on SDA .

1. P = Power, I /O = Input/Output, DI = Digital input, DO = Digital output, AI = Analog input, and GND = Ground.

5 Parameter Information

5.1 Absolute Maximum Ratings

T_A = 25°C, unless otherwise noted[1].

SYMBOL	PARAMETER	MIN	MAX	UNIT
Supply voltage	VDD to GND	−0.3	7	V
Analog input voltage	AIN0, AIN1, AIN2, AIN3	GND − 0.3	VDD + 0.3	V
Digital input voltage	SCL, SDA, A DDR, ALERT/RDY	GND − 0.3	VDD + 0.3	V
Continuous input current	Any pin except the power pin	−10	10	mA
T_A	Operating temperature	−40	125	°C
T_J	Operating junction temperature	−40	150	°C
T_{stg}	Storage temperature	−60	150	°C

1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to maximum rated voltage conditions for extended periods may affect device reliability.

5.2 Recommended Operating Conditions

T_A = 25°C, unless otherwise noted.

SYMBOL	PARAMETER	MIN	MAX	UNIT
VDD	VDD to GND	2.7	5.5	V
$V_{(AINP)} – V_{(AINN)}$ [1]	Full-scale input voltage range[2]	±0.064	±6.144	V
$V_{(AINx)}$ [1]	Analog input voltage	GND	VDD	V
V_{DIG}	Digital input voltage	GND	VDD	V
T_A	Operating temperature	−40	125	°C

1. AINP and AINN indicate the selected positive and negative inputs. AINx indicates one of the four available analog inputs.
2. This parameter represents the full-scale input voltage range of the ADC scaling. The analog inputs of the device cannot exceed VDD + 0.3V.

5.3 ESD Performance

SYMBOL	CONDITIONS	VALUE	UNIT
$V_{ESD(HBM)}$	Human-body model (HBM), ANSI/ESDA/JEDEC JS-001-2017[1]	±2000	V
$V_{ESD(CDM)}$	Charge-device model (CDM), ANSI/ESDA/JEDEC JS-002-2022[2]	±500	V

1. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing using standard ESD control processes.
2. JEDEC document JEP157 states that a 250-V CDM allows safe manufacturing using standard ESD control processes.

5.4 Thermal Resistance

SYMBOL[1]	CONDITIONS	MSOP-10	UNIT
Θ_{JA}	Junction to ambient thermal resistance	182.7	°C/W
$\Theta_{JC(TOP)}$	Junction to case (top) thermal resistance	67.2	°C/W
Θ_{JB}	Junction to board thermal resistance	103.8	°C/W
Ψ_{JB}	Junction-to-Board Parameters	102.1	°C/W
Ψ_{JT}	Junction to Top Parameters	10.2	°C/W

1. Thermal resistance characteristic parameter data is based on thermal simulation results and complies with JEDEC document JESD51-7.

5.5 Technical Specifications

VDD = 3.3 V, data rate = 6.25SPS, full-scale input voltage range (FSR) = ±2.048 V (unless otherwise noted). Maximum and minimum specifications apply for T_A = −40 °C to +125 °C. Typical specifications are for T_A = 25 °C.

PARAMETER	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNIT
Analog input impedance			1		GΩ
System Performance					
Resolution (no missing code)		24			Bits
Data rate (DR)		6.25, 12.5, 25, 50, 100, 250, 500, 1000			SPS
Data rate changes	All data rates	−5		5	%
Output Noise		See the *Noise Performance*section			
Integral Nonlinearity (INL)	DR = 6.25SPS, FSR = ±2.048V[2]		10		ppm/FSR
Offset Error	FSR = ±2.048V, differential input		±30		μV
	FSR = ±2.048 V, single-ended input		±30		
Temperature offset drift	FSR = ±2.048 V		0.15		uV/°C
Gain Error[3]	FSR = ±2.048 V, T_A = 25°C		0.1	0.25	%
Gain drift with temperature[3]	FSR = ±0.256 V		10		ppm/°C
	FSR = ±2.048 V		10	40	ppm/°C
	FSR = ±6.144 V[1]		10		ppm/°C
Long-term gain drift[3]	FSR = ±2.048 V, T_A = 125°C, 1000hrs		±0.05		%
Gain Power Supply Rejection			40		ppm/V
Gain Match[3]	Matching between any two gains		0.1		%
Gain channel matching	A match between any two inputs		0.02		%
Common Mode Rejection Ratio (CMRR)	at DC, FSR = ±0.256 V		105		dB
	at DC, FSR = ±2.048 V		100		dB
	at DC, FSR = ±6.144 V[1]		90		dB
	f_{CM} = 60 Hz, DR = 6.25 SPS		105		dB
	f_{CM} = 50 Hz, DR = 6.25 SPS		105		dB

Technical Specifications (Continued)

VDD = 3.3 V, data rate = 6.25 SPS, full-scale input voltage range (FSR) = ±2.048 V (unless otherwise noted). Maximum and minimum specifications apply for T_A = −40 °C to +125 °C. Typical specifications are for T_A = 25 °C.

PARAMETER	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNIT
Digital Input/Output					
High level input voltage (V_{IH})		0.7VDD		VDD	V
Low level input voltage (V_{LH})		GND		0.3VDD	V
Low level output voltage (V_{OL})	I_{OL} = 3 mA	GND	0.15	0.4	V
Input leakage current	GND < VDIG < VDD	−10		10	μA
Power Supply					
Supply Current (I_{VDD})	Power-down mode, T_A = 25 °C		0.5	2	μA
	Power-down mode			5	
	Operating mode, T_A = 25 °C		150	200	
	Working Mode			300	
Power consumption (P_D)	VDD = 5.0 V		0.9		mW
	VDD = 3.3 V		0.5		
	VDD = 2.7 V		0.3		

1. This parameter represents the full -scale range of the ADC scaling. The voltage applied to the analog input does not exceed VDD + 0.3V.
2. Best fit INL; covers 99% of full scale.
3. Includes all errors from the PGA and voltage reference.

5.6 I2C Timing Specifications

Over the operating ambient temperature range and VDD = 2.7V to 5.5V (unless otherwise noted).

		Fast Mode		High-speed modulus		UNIT
		MIN	MAX	MIN	MAX	
f_{SCL}	SCL clock frequency	0.01	0.4	0.01	3.4	MHz
t_{BUF}	Bus free time between START and STOP conditions	600		160		ns
t_{HDSTA}	Hold time after repeated Start condition. After this period, the first clock is generated.	600		160		ns
t_{SUSTA}	Setup time for a repeated start condition	600		160		ns
t_{SUSTO}	STOP condition setup time	600		160		ns
t_{HDDAT}	Data retention time	0		0		ns
t_{SUDAT}	Data creation time	100		10		ns
t_{LOW}	The low level period of the SCL clock pin	1300		160		ns
t_{HIGH}	The high period of the SCL clock pin	600		60		ns

		Fast Mode		High-speed modulus		UNIT
		MIN	MAX	MIN	MAX	
t_F	time of SDA and SCL signals1		300		160	ns
t_R	Fall time of SDA and SCL signals[1]		300		160	ns

1. For high-speed mode maximum, the capacitive loading on the bus must not exceed 400 pF.

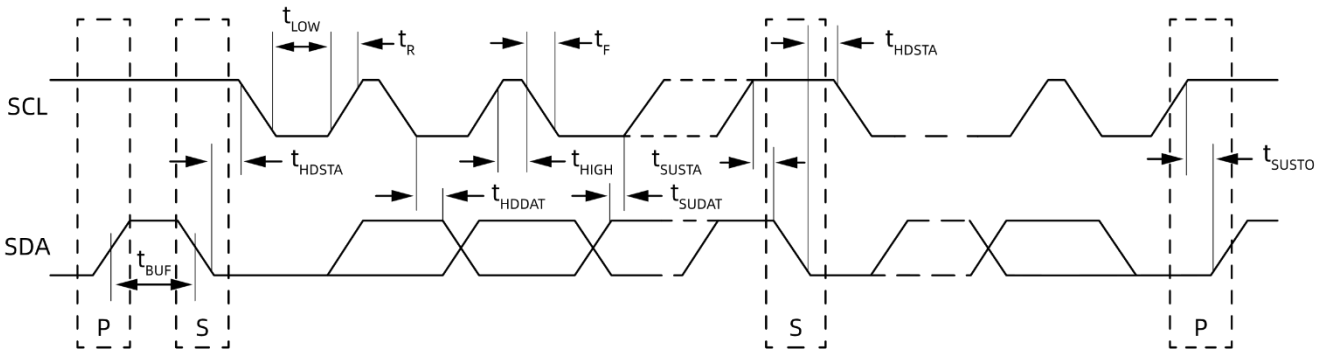


Figure 1. I2C Interface Timing

6 Parameter Measurement Information

6.1 Noise Performance

Delta-sigma analog-to-digital converters (ADCs) are based on the principle of oversampling. The input signal to a delta-sigma ADC is sampled at a high frequency (the modulator frequency) and subsequently filtered and decimated in the digital domain to produce a conversion result at the corresponding output data rate. The ratio between the modulator frequency and the output data rate is called the oversampling ratio (OSR). By increasing the OSR, and thus reducing the output data rate, the noise performance of the ADC can be optimized. In other words, when the output data rate is reduced, the input referred noise decreases because more samples of the internal modulator are averaged to produce one conversion result. Increasing the gain can also reduce the input referred noise, which is particularly useful when measuring low-level signals.

Table 1 and Table 2 summarize the noise performance of the GD30AD3640. The data represent typical noise performance at T_A = 25 °C with the inputs shorted together externally. Table 1 shows the input referred noise in μVRMS under the conditions shown . Note that the μVPP values are shown in parentheses. Table 2 shows the effective resolution calculated from the μVRMS values using Equation(1)The noise-free resolution calculated from the peak-to-peak noise values using Equation(2) is shown in parentheses.

$$\text{Effective Resolution} = \ln(FSR / V_{RMS\_Noise}) / \ln 2 \quad (1)$$

$$\text{Noise-Free Resolution} = \ln(FSR / V_{PP\_Noise}) / \ln 2 \quad (2)$$

Table 1. Noise in uV_{RMS} (uV_{PP}) at VDD = 3.3V

Data Rate (SPS)	FSR (Full-Scale Range)						
	±6.144 V	±4.096 V	±2.048 V	±1.024 V	±0.512 V	±0.256 V	±0.064 V
6.25	1.036 (3.662)	0.577 (2.441)	0.289 (1.465)	0.170 (0.732)	0.102 (0.488)	0.065 (0.275)	0.037 (0.183)
12.5	1.410 (8.057)	0.987 (4.883)	0.435 (2.197)	0.252 (1.343)	0.137 (0.732)	0.086 (0.458)	0.051 (0.259)
25	1.902 (11.719)	1.293 (7.813)	0.637 (3.418)	0.344 (1.953)	0.183 (0.977)	0.125 (0.763)	0.076 (0.511)
50	2.789 (17.578)	1.826 (9.766)	0.933 (5.859)	0.484 (3.052)	0.268 (1.709)	0.175 (1.099)	0.114 (0.664)
100	3.763 (24.170)	2.464 (19.043)	1.298 (7.813)	0.667 (5.127)	0.386 (2.625)	0.254 (1.678)	0.159 (1.068)
250	6.228 (44.678)	3.975 (26.367)	2.028 (14.160)	1.062 (8.057)	0.613 (5.066)	0.402 (2.716)	0.248 (1.862)
500	8.437 (61.524)	5.719 (41.016)	2.959 (20.752)	1.513 (10.864)	0.849 (6.958)	0.565 (4.333)	0.365 (2.632)
1000	12.558 (103.272)	8.544 (63.477)	4.410 (34.180)	2.289 (20.996)	1.270 (9.277)	0.832 (6.073)	0.532 (3.777)

Table 2. Effective Resolution (Noise-Free Resolution) at VDD = 3.3V

Data	FSR (Full-Scale Range)

Rate (SPS)	±6.144 V	±4.096 V	±2.048 V	±1.024 V	±0.512 V	±0.256 V	±0.064 V
6.25	23.500 (21.678)	23.758 (21.678)	23.756 (21.415)	23.522 (21.415)	23.265 (21.000)	22.915 (20.830)	21.725 (19.415)
12.5	23.055 (20.541)	22.985 (20.678)	23.167 (20.830)	22.955 (20.541)	22.837 (20.415)	22.500 (20.093)	21.264 (18.913)
25	22.623 (20.000)	22.595 (20.000)	22.617 (20.193)	22.507 (20.000)	22.414 (20.000)	21.963 (19.356)	20.688 (17.934)
50	22.071 (19.415)	22.097 (19.678)	22.066 (19.415)	22.014 (19.356)	21.868 (19.193)	21.478 (18.830)	20.103 (17.557)
100	21.639 (18.956)	21.665 (18.715)	21.589 (19.000)	21.551 (18.608)	21.340 (18.574)	20.941 (18.219)	19.617 (16.871)
250	20.912 (18.069)	20.975 (18.245)	20.946 (18.142)	20.879 (17.956)	20.673 (17.625)	20.280 (17.524)	18.977 (16.069)
500	20.474 (17.608)	20.450 (17.608)	20.401 (17.591)	20.368 (17.524)	20.203 (17.167)	19.791 (16.850)	18.418 (15.570)
1000	19.900 (16.860)	19.871 (16.978)	19.825 (16.871)	19.771 (16.574)	19.621 (16.752)	19.231 (16.363)	17.877 (15.049)

7 Detailed Description

7.1 Block Diagram

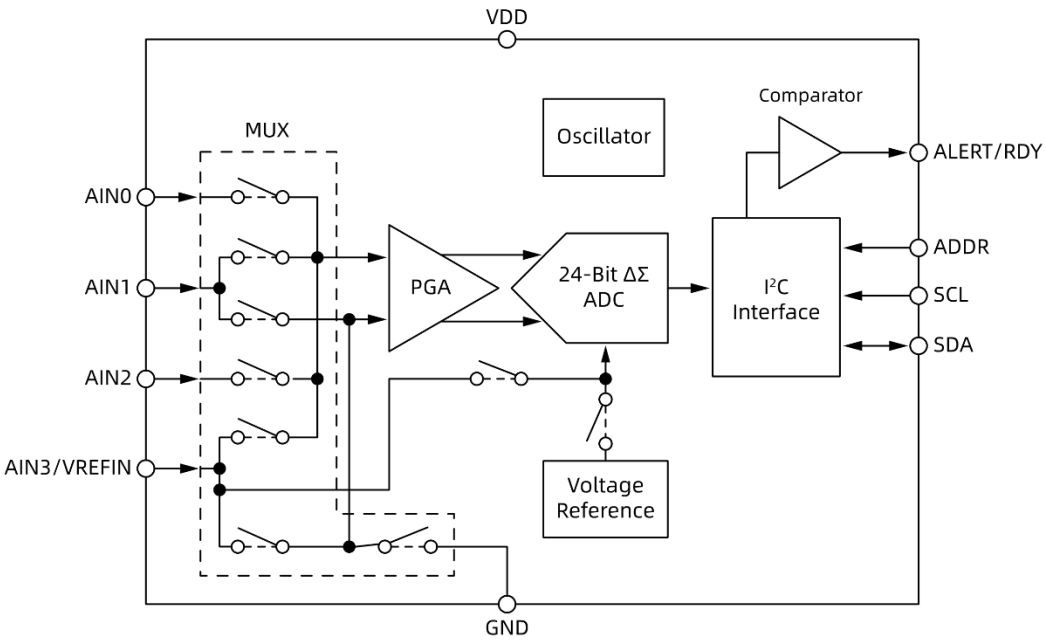


Figure 2. GD30AD3640 Block Diagram

7.2 Operation

7.2.1 Overview

The GD30AD3640 is a very small, low-power 24-bit delta-sigma analog-to-digital converter (ADC). The GD30AD3640 contains a delta-sigma ADC core with an internal voltage reference, a clock oscillator, and an I2C interface. The GD30AD3640 also integrates a programmable gain amplifier (PGA) and a programmable digital comparator. Figure 2 shows the functional block diagram of the GD30AD3640 .

The GD30AD3640 ADC core measures the differential signal VIN, which is the difference between V(AINP) and V(AINN). The converter core consists of a differential switched capacitor delta-sigma modulator and a digital filter. The input signal is compared with an internal reference voltage. The digital filter receives a high-speed bit stream from the modulator and outputs data proportional to the input voltage.

The GD30AD3640 has two available conversion modes: single mode and continuous conversion mode. In single mode, the ADC performs one conversion on the input signal upon request, stores the conversion value to the internal conversion register, and then enters a power-down state. This mode is designed to provide significant power savings for systems that only require periodic conversions or have long idle times between conversions. In continuous conversion mode, the ADC automatically starts conversion of the input signal as soon as the previous conversion is completed. The rate of continuous conversion is equal to the programmed data rate. Data can be read at any time and reflects the completed conversion in real time.

7.3 Features

7.3.1 Multiplexer

The GD30AD3640 contains an input multiplexer (MUX),as shown in Figure 3. Four single-ended signals or two differential signals can be measured. In addition, AIN0 and AIN1 may be measured differentially with AIN3. The multiplexer is configured by the MUX[2:0] bits in the *Configuration Register* (Config Register) (P[1:0]=1h)[Reset=8583h]. When measuring single-ended signals, the negative input of the ADC is connected to GND through a switch inside the multiplexer.

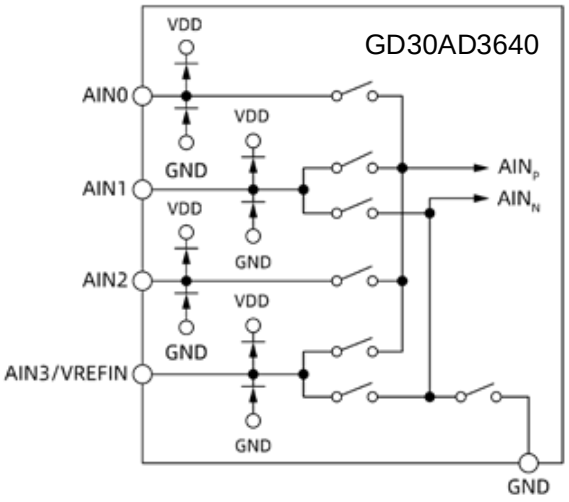


Figure 3. Input Multiplexer

When measuring single-ended inputs, the device does not output negative codes. These negative codes represent negative differential signals, that is, (V(AINP) - V(AINN)) < 0. Electrostatic discharge (ESD) diodes connected to VDD and GND protect the GD30AD3640 analog inputs. Keep the absolute voltage of any input form within the range shown in Equation (3)to prevent the ESD diodes from turning on.

$$GND - 0.3V < V_{(AINX)} < VDD + 0.3V \quad (3)$$

If the voltage on the input pin violates these conditions, use an external Schottky diode and series resistor to limit the input current to a safe value (see the *Absolute Maximum Ratings*).

7.3.2 Analog Input

The analog input has a high-impedance PGA with an impedance greater than 1GΩ . No additional driver amplifier is required.

7.3.3 Full Scale Range (FSR) and LSB Size

A programmable gain amplifier (PGA) is implemented before the delta-sigma ADC of the GD30AD3640. The full-scale range is configured by the PGA[2: 0] bits in the *Configuration Register* (Config Register) (P[1:0]=1h)[Reset=8583h] and can be set to ±6.144 V, ±4.096 V, ±2.048 V, ±1.024 V, ±0.512 V, ±0.256 V, ±0.064 V. Table 3 shows the FSR and the corresponding LSB size. Equation (4)shows how to calculate the LSB size from the selected full-scale range.

$$LSB = FSR / 2^{24} \quad (4)$$

Table 3. Full-Scale Range and Corresponding LSB Size

Full scale range	The size of the least significant bit
±6.144 V[1]	732 nV
±4.096 V[1]	488 nV
±2.048 V	244 nV
±1.024 V	122 nV
±0.512 V	61 nV
±0.256 V	30.5 nV
±0.064 V	7.63 nV

1. This parameter represents the full-scale range of the ADC scaling. Do not apply voltages exceeding VDD + 0.3 V to the analog inputs of the device.

The analog input voltage must not exceed the analog input voltage limits given in *Absolute Maximum Ratings*. If a VDD supply voltage greater than 4 V is used, the ± 6.144 V full-scale range allows the input voltage to extend to the supplies. Although in this case (or when the supply voltage is less than the full-scale range; for example, VDD = 3.3 V and the full-scale range = ±4.096 V), the full-scale ADC output value cannot be obtained. For example, when VDD = 3.3 V and FSR = ±4.096 V, only signals up to VIN = ±3.3 V can be measured, which in this case results in a loss of part of the measurement dynamic range.

7.3.4 Reference Voltage

The GD30AD3640 integrates a voltage reference. Errors associated with initial voltage reference accuracy and reference drift over temperature are included in the gain error and gain drift specifications in the table of *Technical Specifications*.

Supports AIN3 as an external reference source.

7.3.5 Oscillator

The GD30AD3640 has an integrated oscillator that runs at 512 kHz. No external clock is required to operate these devices. The internal oscillator drifts with temperature and time. The output data rate is proportional to the oscillator frequency.

7.3.6 Output Data Rate and Conversion Time

The GD30AD3640 provides programmable output data rates. Use the DR[2:0] bits in the *Configuration Register* (Config Register) (P[1:0]=1h)[Reset=8583h] to select output data rates of 6.25 SPS, 12.5 SPS , 25 SPS, 50 SPS , 100 SPS, 250 SPS , 500 SPS , or 1000 SPS .

GD30AD3640 settles within one cycle; therefore, the conversion time is equal to 1 / DR.

7.3.7 Digital Comparator

The GD30AD3640 has a programmable digital comparator that can issue an alert on the ALERT/RDY pin. The COMP_MODE bit in the *Configuration Register* (Config Register) (P[1:0]=1h)[Reset=8583h] configures the comparator as a traditional comparator or a window comparator. In traditional comparator mode, the ALERT/RDY pin is set (active low by default) when the conversion data exceeds the limit value set in the high threshold register

(Hi_thresh). The comparator is set high only when the conversion data is below the limit value set in the low threshold register (Lo_thresh). In window comparator mode, the ALERT/RDY pin is set when the conversion data exceeds the Hi_thresh register or is below the Lo_thresh register value.

In either window or traditional comparator modes, the comparator can be configured to latch after assertion by the COMP_LAT bit in the *Configuration Register* (Config Register) (P[1:0]=1h)[Reset=8583h]. This setting causes the assertion to remain even if the input signal does not exceed the range of the Threshold register. This latched assertion can only be cleared by issuing an SMBus ALERT response or reading the

Conversion Register (P[1:0]=0h) [Reset=0000h]. The ALERT/RDY pin can be configured as either active high or active low by the COMP_POL bit in the *Configuration Register* (Config Register) (P[1:0]=1h)[Reset=8583h]. Figure 4 shows the operation diagram for both comparator modes.

The comparator can also be configured to activate the ALERT/RDY pin only after successive readings exceed the threshold set in the threshold registers (Hi_thresh and Lo_thresh). The COMP_QUE[1:0] bits in the *Configuration Register* (Config Register) (P[1:0]=1h)[Reset=8583h] configure the comparator to wait for one, two, or four readings above the threshold before activating the ALERT/RDY pin. The COMP_QUE[1:0] bits can also disable the comparator function and set the ALERT/RDY pin in a high state.

7.3.8 Conversion Completed Pin

The ALERT/RDY pin can also be configured as a convert-ready pin. Set the most significant bit of the Hi_thresh register to 1 and the most significant bit of the Lo_thresh register to 0 to make this pin a convert-ready pin. The COMP_POL bit continues to work as expected. Set the COMP_QUE[1:0] bits to any 2-bit value other than 11 to keep the ALERT/RDY pin enabled and allow the convert-ready signal to appear at the ALERT/RDY pin output. The COMP_MODE and COMP_LAT bits no longer control any function. When configured as a convert-ready pin, ALERT/RDY still requires a pull-up resistor. In continuous conversion mode , the GD30AD3640 provides a convert-ready pulse of approximately 8μs on the ALERT/RDY pin at the end of each conversion, as shown in Figure 5. In single-shot mode, if the COMP_POL bit is set to 0, the ALERT/RDY pin is asserted low at the end of a conversion.

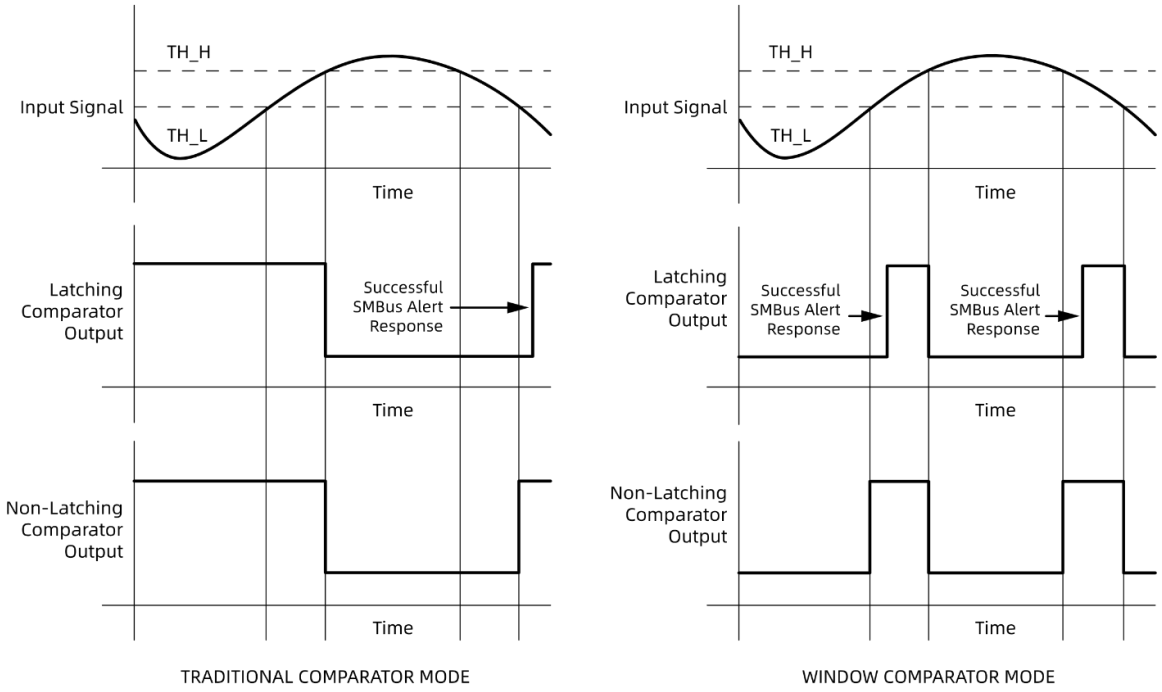


Figure 4. ALERT Pin Timing Diagram

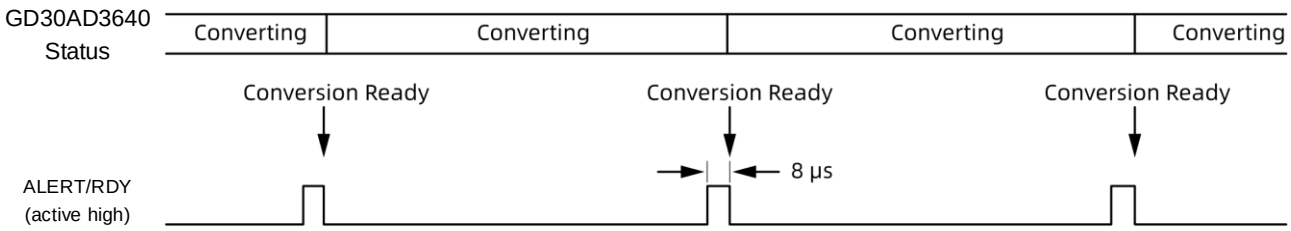


Figure 5. Convert-Ready Pulse in Continuous Conversion Mode

7.3.9 SMbus Alert Response

In latched comparator mode (COMP_LAT=1), the ALERT/RDY pin is asserted when the comparator detects a conversion that exceeds the upper or lower threshold. This assertion is latched and can only be cleared by reading the conversion data or by issuing a successful SMBus alert response and reading the I2C address of asserting device. If the conversion data exceeds the upper or lower threshold after being cleared, the pin is reasserted. This assertion does not affect conversions already in progress. The ALERT/RDY pin is an open-drain output. This architecture allows multiple devices to share the same interface bus. When disabled, the pin remains high so that the pin does not interfere with other devices on the same bus.

When the host detects that the ALERT/RDY pin is latched, the host issues an SMBus alert command (00011001) to the I2C bus. Any GD30AD3640 data converter on the I2C bus uses the ALERT/RDY pin to respond to commands with the slave address. If multiple GD30AD3640 on the I2C bus assert the latched ALERT/RDY pin, arbitration during the address response portion of the SMBus alert determines which device clears the assertion. The device with the lowest I2C address always wins arbitration. If a device loses arbitration, the device does not clear the comparator output pin assertion. The master device then repeats the SMBus alert response until all

devices have their respective assertions cleared. In window comparator mode, the SMBus alert status bit indicates 1 if the signal exceeds the high threshold and 0 if the signal exceeds the low threshold.

7.4 Functional Mode

7.4.1 Reset and Power-On

The GD30AD3640 is reset at power-on and sets all bits in the *Configuration Register* (Config Register) (P[1:0]=1h)[Reset=8583h] to their respective default settings. The GD30AD3640 enters a power-off state after completing the reset process. The device interface and digital blocks are active, but no data conversion is performed. The initial power-off state of the GD30AD3640 relieves power-critical systems from experiencing surges during power-on. The GD30AD3640 responds to an I2C general call reset command. When the GD30AD3640 receives a broadcast reset command (06h), an internal reset is performed, the same as a reset at device power-on.

7.4.2 Operation Mode

The GD30AD3640 operates in one of two modes: continuous conversion mode or single-shot mode. The corresponding operation mode can be selected by the MODE bit in the *Configuration Register* (Config Register) (P[1:0]=1h)[Reset=8583h].

7.4.2.1 Single Mode

When the MODE bit in the *Configuration Register* (Config Register) (P[1:0]=1h)[Reset=8583h] is set to 1, the GD30AD3640 enters a power-down state and operates in single-shot mode. This power-down state is the default state when the GD30AD3640 is first powered on. Despite being powered off, the device will still respond to commands. The GD30AD3640 will remain in this power-down state until a 1 is written to the operating status (OS) bit in the *Configuration Register* (Config Register) (P[1:0]=1h)[Reset=8583h]. When the OS bit is set, the device powers up in approximately 25 μs, resets the OS bit to 0, and starts a single conversion. When the data conversion is complete, the device powers down again. Writing a 1 to the OS bit while a conversion is in progress has no effect. To switch to continuous conversion mode, write a 0 to the MODE bit in the *Configuration Register* (Config Register) (P[1:0]=1h)[Reset=8583h].

7.4.2.2 Continuous Conversion Mode

In continuous conversion mode (MODE bit set to 0), the GD30AD3640 performs conversions continuously. After the conversion is completed, the GD30AD3640 places the result into the

Conversion Register (P[1:0]=0h) [Reset=0000h] and immediately starts another conversion.

When programming new configuration settings, the conversion currently in progress is completed using the previous configuration settings. Thereafter, continuous conversions using the new configuration settings begin. To switch to single conversion mode, write a 1 to the MODE bit in the *Configuration Register* (Config Register) (P[1:0]=1h)[Reset=8583h] or reset the device.

7.4.3 Low Power Consumption Duty Cycle

A delta-sigma ADC generally improves when the output data rate is reduced because more samples of the internal modulator are averaged to produce one conversion result. In applications where power consumption is critical,

the improved noise performance at low data rates may not be necessary. For these applications, the GD30AD3640 supports duty cycles, which significantly saves power by periodically requesting high data rate readings at an effectively lower data rate. For example, the power consumption of the GD30AD3640 set by the host controller at a data rate of 1000SPS is 1/125 of the power consumption at a data rate of 8 SPS, because the conversion at a rate of 1000 SPS only takes about 1ms, and the conversion at a rate of 8 SPS takes about 125 ms, so 8SPS will work 124 ms more than 1000 SPS. The host controller can arbitrarily define the sampling duty cycle. The GD30AD3640 provides lower data rates and also provides improved noise performance when needed.

7.5 Programming

7.5.1 I2C Interface

The GD30AD3640 communicates via the I2C interface. I2C is a two-wire open-drain interface that supports multiple devices and hosts on a single bus. Devices on an I2C bus drive the bus line low only by connecting it to ground; these devices never push the bus line high. Instead, the bus is pulled high by pull-up resistors, so that when no device drives the bus low, the bus is always high. Because of this configuration, two devices will not conflict. If two devices drive the bus at the same time, there is no driver contention. Communication on the I2C bus is always between two devices, one as a master device and the other as a slave device. Both master and slave can read and write, but the slave can only do it under the command of the master. Some I2C devices can act as a master or a slave, but the GD30AD3640 can only act as a slave. The I2C bus consists of two lines: SDA and SCL. SDA carries data and SCL provides the clock. All data is transmitted over the I2C bus in groups of 8 bits. To send a bit on the I2C bus, drive the SDA line to the appropriate level while SCL is low (a low level on SDA means the bit is zero and a high level means the bit is one). After the SDA line is stable, the SCL line is first pulled high and then pulled low. This pulse on SCL clocks the SDA bit into the receiving shift register. If the I2C bus remains idle for more than 25 ms, the bus times out. The I2C bus is bidirectional; that is, the SDA line is used for both sending and receiving data. The slave drives the data line when the master reads from the slave; the master drives the data line when the master sends to the slave. The master always drives the clock line. The GD30AD3640 cannot act as a master and therefore can never drive SCL.

Most of the time the bus is idle. No communication is happening and both lines are high; when communication is taking place, the bus is active. Only the master device can start communication and initiate a START condition on the bus. Normally, the data line is only allowed to change state when the clock line is low. If the data line changes state when the clock line is high, it is either a START condition or a STOP condition. The START condition occurs when the data line changes from high to low while the clock line is high. The STOP condition occurs when the clock line is high and the data line changes from low to high.

After the master issues a START condition, the master sends a byte indicating which slave device to communicate with. This byte is called the address byte. Each device on the I2C bus has a unique 7-bit address to respond to. The master sends an address in the address byte, along with a bit indicating whether the master wishes to read or write to the slave. Each byte (address and data) transmitted on the I2C bus is acknowledged by an acknowledge bit. When the master has finished sending a byte (8 data bits) to the slave, the master stops driving SDA and waits for the slave to acknowledge the byte. The slave acknowledges the byte by pulling SDA low. The master then sends a clock pulse to clock the acknowledge bit. Similarly, when the master has finished reading a byte, the master pulls SDA low to acknowledge this completion to the slave. The master then sends a clock pulse to clock the bit. The master always drives the clock line.

If a device is not present on the bus and the master attempts to address it, it receives a non-acknowledge because there is no device at that address pulling the line low. A non-acknowledge is performed by holding SDA high during the acknowledge cycle.

When the master device has finished communicating with the slave device, it may issue a STOP condition. When a STOP condition is issued, the bus becomes idle again. The master can also issue another START condition. Issuing a START condition while the bus is active is called a repeated START condition.

The Timing Requirements section (Figure 1. I2C Interface Timing) shows the timing diagram for the I2C communication of the GD30AD3640 .

7.5.1.1 I2C Address Selection

The GD30AD3640 has an address pin ADDR, which is used to configure the I2C address of the device. This pin can be connected to GND, VDD, SDA, or SCL, allowing four different addresses to be selected with one pin, as shown in Table 4. The state of the address pin ADDR is sampled continuously. First use the GND, VDD, and SCL address. If SDA is used as the device address, keep the SDA line low for at least 100 ns after the SCL line goes low to ensure that the device correctly decodes the address during I2C communication.

Table 4. ADDR Pin Connections and Corresponding Slave Addresses

Address pin connections	Slave Address
GND	1001000
VDD	1001001
SDA	1001010
SCL	1001011

7.5.1.2 I2C General Call

If the 8th bit is 0, the GD30AD3640 responds to the I2C general call address (0000000). The device acknowledges the general call address and responds to the command in the second byte. If the second byte is 00000110 (06h), the GD30AD3640 resets the internal registers and enters the power-down state.

7.5.1.3 I2C Speed Mode

The I2C bus operates at one of three speeds. Standard mode allows clock frequencies up to 100 kHz; Fast mode allows clock frequencies up to 400 kHz; High-speed mode (also known as Hs-mode) allows clock frequencies up to 3.4 MHz. The GD30AD3640 is fully compatible with all three modes.

No special operation is required to use the GD30AD3640 in standard or fast mode, but high-speed mode must be activated. To activate high-speed mode, send a special address byte 00001xxx after the START condition, where xxx is a bit unique to the Hs-capable master device. This byte is called the Hs master code and is different from the normal address byte; the 8th bit does not indicate the read or write status. The GD30AD3640 does not acknowledge this byte; the I2C specification prohibits acknowledging the Hs master code. After receiving the master code, the GD30AD3640 turns on the Hs mode filter and communicates at a frequency of up to 3.4 MHz. The GD30AD3640 exits Hs mode at the next STOP condition. For more information on high-speed mode, refer to the I2C specification.

7.5.2 Slave Mode Operation

The GD30AD3640 acts as a slave receiver or a slave transmitter. The GD30AD3640 cannot drive the SCL line as a slave device.

7.5.2.1 Receiving Mode

In slave receive mode, the first byte sent from the master to the slave consists of the 7-bit device address and the $R/\overline{W}$ bits. The next byte sent by the master is the address pointer register. The GD30AD3640 then acknowledges receipt of the address pointer register byte. The next two bytes are written to the address given by the register address pointer bits P[1:0] . The GD30AD3640 acknowledges each byte sent. Register bytes are sent most significant byte first, followed by least significant byte.

7.5.2.2 Send Mode

In slave transmit mode, the first byte sent by the master is the 7- bit slave address followed by a high bit. This byte puts the slave into transmit mode and indicates that the GD30AD3640 is being read. The next byte sent by the slave is the most significant byte of the register, indicated by the register address pointer bits P[1:0]. This byte is followed by an acknowledgment from the master. The slave then sends the remaining least significant bytes, followed by an acknowledgment from the master. The master can terminate the transfer after any byte by not acknowledging or issuing a START or STOP condition.

7.5.3 Writing and Reading Registers

To access a specific register from the GD30AD3640, the host must first write the appropriate value to the register address pointer bits P[1:0] in the address pointer register. The address pointer register is written directly after the slave address byte, the $R/\overline{W}$ bit, and a successful slave acknowledgement. After writing to the address pointer register, the slave acknowledges and the host issues a STOP or repeated START condition.

When reading from the GD30AD3640, the previous value written to bits P[1:0] determines the register that is read. To change which register is read, a new value must be written to P[1:0] . To write a new value to P[1:0] , the host issues a $R/\overline{W}$ slave address byte with one bit low, followed by the address pointer register byte. No additional data needs to be transmitted, and the host can issue a STOP condition. The host can now issue a START condition and send $R/\overline{W}$ a slave address byte with one bit high to begin reading. Figure 5 details this sequence. If repeated reads from the same register are required, the address pointer register does not need to be sent continuously, because the GD30AD3640 stores the value of P[1:0] until it is modified by a write operation. However, for each write operation, the address pointer register must be written with the appropriate value.

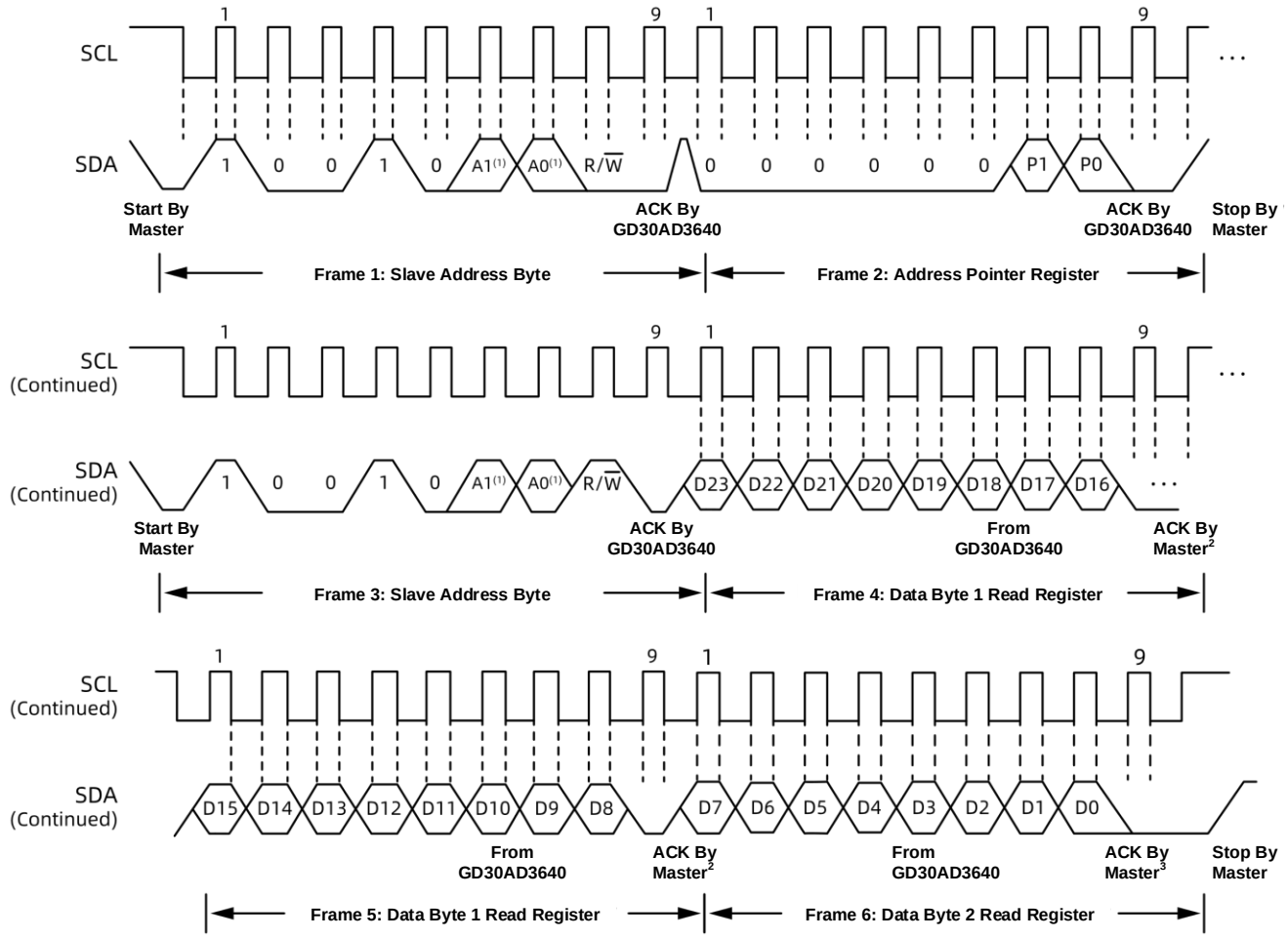


Figure 6. Timing Diagram of Reading from GD30AD3640

1. The values of A0 and A1 are determined by the ADDR pin.
2. The host can hold SDA high to terminate a single-byte read operation.
3. The host can hold SDA high to terminate a two-byte read operation.

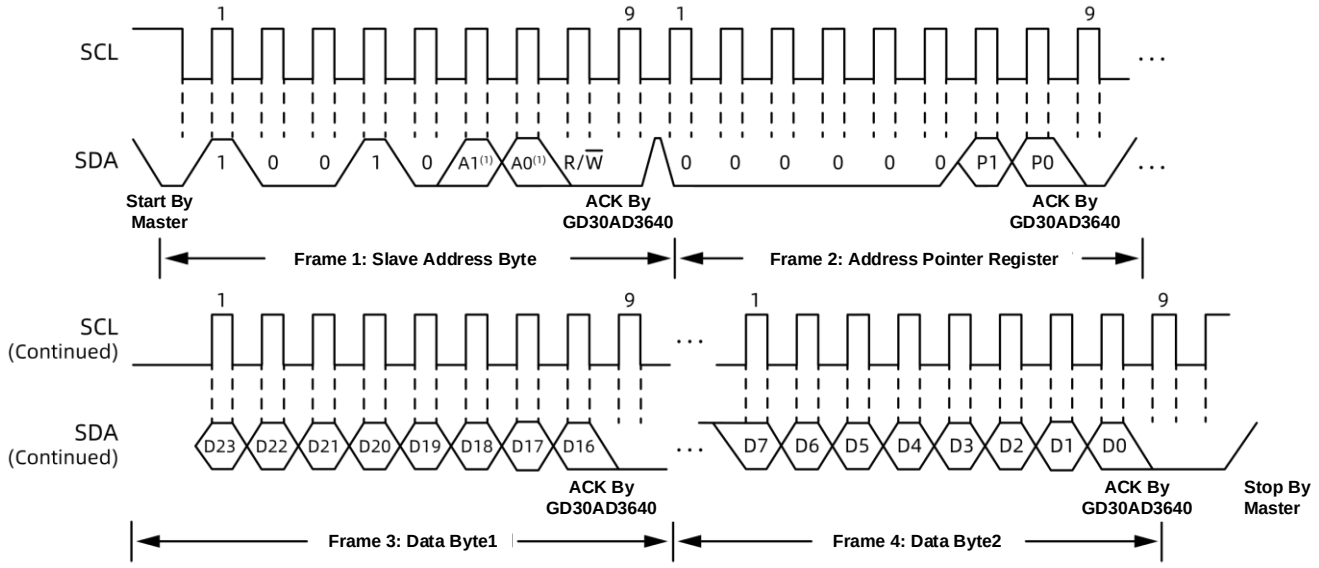


Figure 7. Timing Diagram of Writing to GD30AD3640

1. The values of A0 and A1 are determined by the ADDR pin.

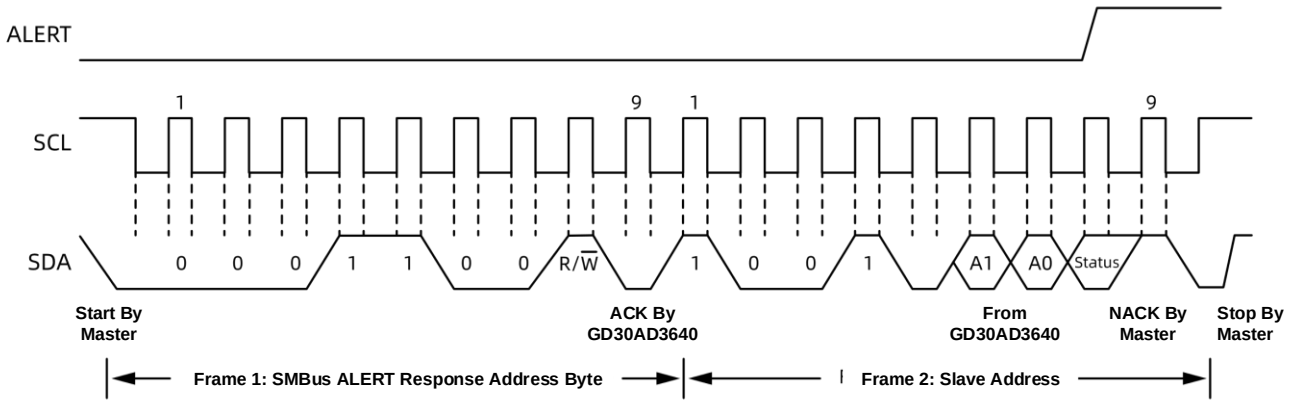


Figure 8. SMBus Alarm Response Feedback Timing Diagram

1. The values of A0 and A1 are determined by the ADDR pin.

7.5.4 Data Format

The GD30AD3640 provides 24-bit data in two's complement format . A positive full-scale (+FS) input produces an output code of 7FFFFFh, and a negative full-scale (–FS) input produces an output code of 800000h. For signals exceeding full-scale, data up to full-scale is displayed. Table 5 summarizes the ideal output codes for different input signals. Figure 9 shows the relationship between code transitions and input voltage.

Table 5. Input Signals and Ideal Output Codes

Input Signal ($V_{INAINPAINN}$)	Ideal output code[1]
≥ +FS (2^{23} – 1)/2^{23}	7FFFFFh
+FS/2^{23}	000001h
0	000000h
–FS/2^{23}	FFFFFFh
≤ –FS	800000h

1. Does not include the effects of noise, INL, offset, and gain errors.

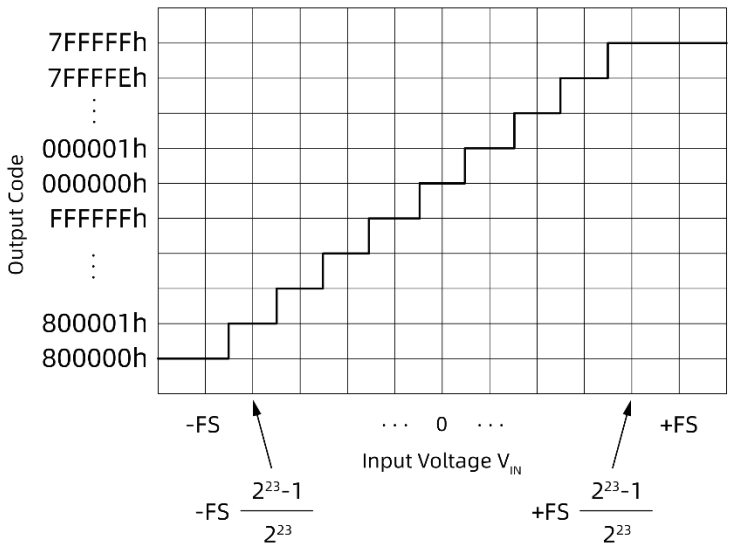


Figure 9. Code Conversion Diagram

7.6 Register Map

The GD30AD3640 has four registers that can be accessed through the I2C interface using the address pointer register. The conversion register contains the result of the last conversion. The Config register is used to change the operating mode of the GD30AD3640 and query the status of the device. The other two registers, Lo_thresh and Hi_thresh, set the thresholds used for the comparator function.

7.6.1 Address Pointer Register (address = NA) [reset = NA]

All four registers are accessed by writing to the Address Pointer register; see Table 6.

Table 6. Address Pointer Register

7	6	5	4	3	2	1	0
0	0	0	0	0	0	P[1:0]	
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	

Example: RW = read and write; R = read only; W = write only; -n = value after reset.

Table 7. Address Pointer Register Field Description

Bit	Field	Type	Reset	Description
7:2	Reserved	W	0h	Always write 0h
1:0	P[1:0]	W	0h	Register address pointer 00: conversion register 01: Configuration register 10: Lo_thresh register 11: Hi_thresh register

7.6.2 Conversion Register (P[1:0]=0h) [Reset=0000h]

The 24-bit conversion register contains the result of the last conversion in two's complement format. After power-up, the conversion register is cleared to 0 and remains at 0 until the first conversion is completed.

Table 8. Conversion Registers

23	22	21	20	19	18	17	16
D23	D22	D21	D20	D19	D18	D17	D16
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
D15	D14	D13	D12	D11	D10	D9	D8
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
D7	D6	D5	D4	D3	D2	D1	D0
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Example: RW = read and write; R = read only; -n = reset value

Table 9. Conversion Register Field Description

Bit	Field	Type	Reset	Description
23:0	D[23:0]	R	000000h	24-bit conversion result

7.6.3 Configuration Register (Config Register) (P[1:0]=1h)[Reset=8583h]

A 24-bit configuration register controls the operating mode, input selection, data rate, full-scale range, and comparator mode.

Table 10. Configuration Registers

15	14	13	12	11	10	9	8
OS	MUX[2:0]			PGA[2:0]			MODE
R/W-1h	R/W-0h			R/W-2h			R/W-1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DR[2:0]			COMP_MODE	COMP_POL	COMP_LAT	COMP_QUE[1:0]	
R/W-4h			R/W-0h	R/W-0h	R/W-0h	R/W-3h	

Example: RW = read and write; R = read only; -n = reset value

Table 11. Address Pointer Register Field Description

Bit	Field	Type	Reset	Description
15	OS	R/W	1h	**Run state or single conversion start** This bit determines the operating state of the device. The OS can only write to it in the power-down state and has no effect while a conversion is in progress. When writing: 0 = Invalid 1 = Start a single conversion (in power-down state) When reading: 0 = The device is currently performing a conversion 1 = The device is not currently performing a conversion
14:12	MUX[2:0]	R/W	0h	**Input Multiplexer Configuration** These bits configure the input multiplexer. 000 = AINP is AIN0 and AINN is AIN1 (default) 001 = AINP is AIN0 and AINN is AIN3 010 = AINP is AIN1 and AINN is AIN3 011 = AINP is AIN2 and AINN is AIN3 100 = AINP is AIN0 and AINN is GND 101 = AINP is AIN1 and AINN is GND 110 = AINP is AIN2 and AINN is GND 111 = AINP is AIN3 and AINN is GND
11:9	PGA[2:0]	R/W	2h	**Programmable Gain Amplifier Configuration** These bits set the FSR of the programmable gain amplifier. 000 = FSR = ±6.144V 001 = FSR = ±4.096V 010 = FSR = ±2.048V (default)

				011 = FSR = ±1.024V 100 = FSR = ±0.512V 101 = FSR = ±0.256 V 110 = FSR = ±0.064V
8	MODE	R/W	1h	**Device operation mode** This bit controls the operating mode of GD30AD3640. 0 = Continuous conversion mode 1 = Power-down and one-shot mode (default)
7:5	DR[2:0]	R/W	4h	**Data Rate** These bits control the data rate setting. 000 = 6.25SPS 001 = 12.5SPS 010 = 25SPS 011 = 50SPS 100 = 100SPS (default) 101 = 250SPS 110 = 500SPS 111 = 1000SPS
4	COMP_ MODE	R/W	0h	**Comparator Mode** This bit configures the comparator operating mode. 0 = Traditional comparator (default) 1 = Window comparator
3	COMP_ POL	R/W	0h	**Comparator Polarity** This bit controls the polarity of the ALERT/RDY pin. 0 = Active low (default) 1 = High level is valid
2	COMP_ LAT	R/W	0h	**Latched Comparator** This bit controls whether the ALERT/RDY pin is latched after assertion or cleared after a transition within margin of the upper and lower thresholds. 0 = Non-latching comparator. The ALERT/RDY pin does not latch when asserted (default). 1 = Latch the comparator. The asserted ALERT/RDY pin remains latched until the host reads the conversion data or the host sends an appropriate SMBus alert response. The device responds with its address, which is the lowest address on the bus that currently asserts ALERT/RDY.
1:0	COMP_ QUE[1:0]	R/W	3h	**Comparator Queues and Disabling** These bits perform two functions. When set to 11, the comparator is disabled and the ALERT/RDY pin is set to a high-impedance state. When set to any other value, the ALERT/RDY pin and comparator functions are enabled, and the setting value determines the

				number of consecutive conversions that exceed the upper or lower threshold before the ALERT/RDY pin is asserted. 00 = set after 1 conversion 01 = Set after 2 conversions 10 = Set after 4 conversions 11 = Disable comparator and set ALERT/RDY pin to high impedance (default)

1. This parameter represents the full-scale range of the ADC scaling. Do not apply voltages exceeding VDD+0.3V to the ADC.

7.6.4 Lo_thresh (P[1:0]=2h)[reset=8000h] and Hi_thresh (P[1:0]=3h)[reset=7FFFh] registers

The upper and lower thresholds used by the comparator are stored in two 16-bit registers in twos complement format. The comparator is implemented as a digital comparator; therefore, the values in these registers must be updated whenever the PGA settings are changed.

The conversion ready function of the ALERT/RDY pin is enabled by setting the Hi_thresh register MSB to 1 and the Lo_thresh register MSB to 0. To use the comparator function of the ALERT/RDY pin, the Hi_thresh register value must always be greater than the Lo_thresh register value. The threshold register format is shown in Table 13. When set to RDY mode, the ALERT/RDY pin outputs the OS bit in one-shot mode and provides continuous conversion ready pulses in continuous conversion mode.

Table 12. Lo_thresh Register

15	14	13	12	11	10	9	8
Lo_thresh15	Lo_thresh14	Lo_thresh13	Lo_thresh12	Lo_thresh11	Lo_thresh10	Lo_thresh9	Lo_thresh8
R/W-1h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Lo_thresh7	Lo_thresh6	Lo_thresh5	Lo_thresh4	Lo_thresh3	Lo_thresh2	Lo_thresh1	Lo_thresh0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Example: RW = read and write; R = read only; -n = reset value

Table 13. Hi_thresh Register

15	14	13	12	11	10	9	8
Hi_thresh15	Hi_thresh14	Hi_thresh13	Hi_thresh12	Hi_thresh11	Hi_thresh10	Hi_thresh9	Hi_thresh8
R/W-0h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Hi_thresh7	Hi_thresh6	Hi_thresh5	Hi_thresh4	Hi_thresh3	Hi_thresh2	Hi_thresh1	Hi_thresh0
R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h

Example: RW = read and write; R = read only; -n = reset value

Table 14. Lo_thresh and Hi_thresh Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	Lo_thresh[15:0]	R/W	8000h	Low Threshold
15:0	Hi_thresh[15:0]	R/W	7FFF	High Threshold

8 Application and Implementation

Example circuits and suggestions for using the GD30AD3640 in various situations.

8.1 I2C Basic Connections

The connection is shown in Figure 10:

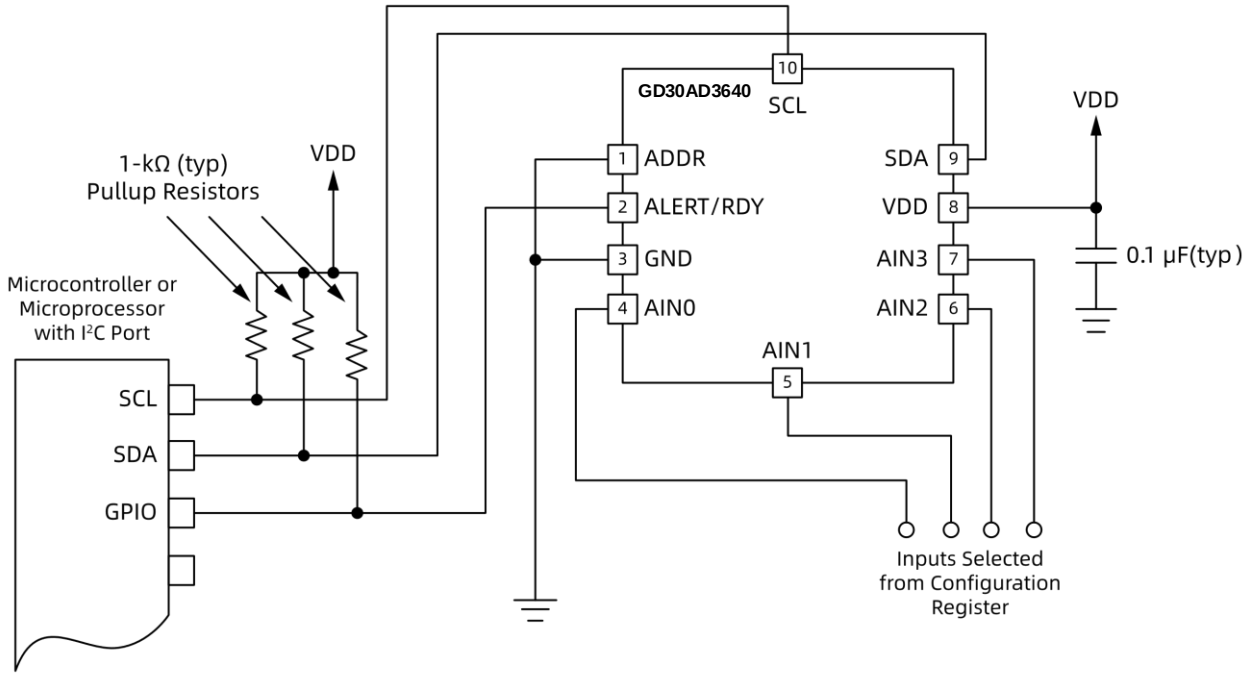


Figure 10. Typical Connections for GD30AD3640

The fully differential voltage inputs of the GD30AD3640 are ideal for connecting to differential sources with moderately low source impedance, such as thermocouples and thermistors. Although the GD30AD3640 can read bipolar differential signals, these devices cannot accept negative voltages on either input.

The GD30AD3640 draws transient current during conversion. A 0.1 µF power supply bypass capacitor can provide the instantaneous burst of extra current required by the power supply.

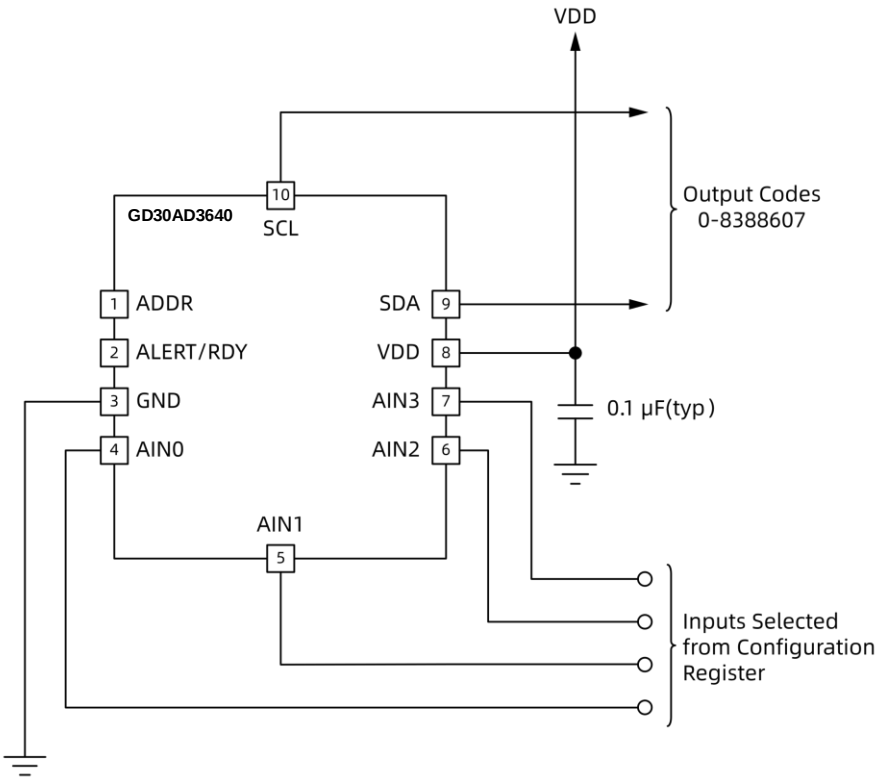
The GD30AD3640 directly connects to standard mode, microcontroller I2C peripherals, fast mode, and high-speed mode I2C controllers.

Includes both Master-Only and Single-Master I2C peripherals that work with the GD30AD3640. The GD30AD3640 does not perform clock stretching (i.e., the device never pulls the clock line low), so there is no need to provide this feature unless other clock stretching devices are on the same I2C bus. Pull-up resistors are required on both the SDA and SCL lines because the I2C bus drivers are open-drain. The size of these resistors depends on the speed at which the bus is operating and the capacitance of the bus lines. Higher value resistors consume less power but increase transition times on the bus, thus limiting bus speed. Lower value resistors allow higher speeds at the expense of higher power consumption. Long busses have higher capacitance and require smaller pull-up resistors to compensate. Do not use resistors that are too small because the bus driver may not be able to pull the bus low.

8.2 Single-Ended Input

The GD30AD3640 can measure up to four single-ended signals. The GD30AD3640 measures single-ended signals by appropriately configuring the MUX[2:0] bits in the *Configuration Register* (Config Register) (P[1:0]=1h)[Reset=8583h]. Figure 11 shows the single-ended connection scheme for the GD30AD3640. The single-ended signal range is from 0V to the positive power supply or +FS, whichever is lower. Negative voltages cannot be applied to these devices because the GD30AD3640 can only accept positive voltages relative to ground. The GD30AD3640 does not lose linearity within the input range.

The GD30AD3640 provides a differential input voltage range of ±FSR. The single-ended configuration uses only one-half of the full-scale input voltage range. The differential configuration maximizes the dynamic range of the ADC and provides better common-mode noise rejection than the single-ended configuration.



NOTE: Digital pin connections omitted for clarity.

Figure 11. Measuring Single-Ended Input

The GD30AD3640 also allows AIN3 to be used as a common point for measurements by setting the MUX[2:0] bits appropriately. AIN0, AIN1, and AIN2 can all be measured relative to AIN3. In this configuration, the GD30AD3640 operates with inputs where AIN3 is used as a common point. This capability increases the usable range allowed, GND < V(AIN3) < VDD.

8.3 Input Protection

The GD30AD3640 is manufactured using a small footprint, low voltage process. The analog inputs have protection diodes connected to the power rails. However, the current handling capability of these diodes is limited, and the GD30AD3640 may be permanently damaged by analog input voltages exceeding approximately 300mV. One way to prevent overvoltage is to place current limiting resistors on the input lines. The GD30AD3640 analog inputs can

withstand up to 10 mA of continuous current.

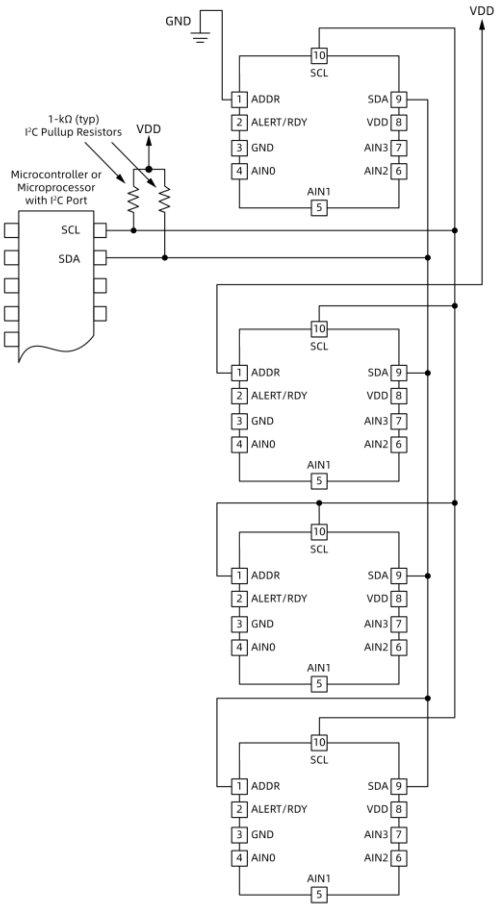
8.4 Unused Inputs and Outputs

Leave unused analog inputs floating, or connect unused analog inputs to midsupply or VDD. You can connect unused analog inputs to GND, but higher leakage current may result.

Leave the NC (not connected) pin unconnected, or connect the NC pin to GND. If the ALERT/RDY output pin is not used, leave it unconnected or connect it to VDD using a weak pull-up resistor.

8.5 Connecting Multiple Devices

Up to four GD30AD3640 devices can be connected to a single I2C bus, with each device using a different address pin configuration. Use the address pins to set the GD30AD3640 to one of four different I2C addresses. Begin with the GND, VDD, and SCL address. If SDA is used as the device address, hold the SDA line low for at least 100ns after the SCL line goes low to ensure that the device correctly decodes the address during I2C communication. Figure 12 shows an example of four GD30AD3640 devices on the same I2C bus. Each bus requires a set of pull-up resistors. It may be necessary to reduce the pull-up resistor value to compensate for the additional bus capacitance and increased line length caused by multiple devices.



NOTE: GD30AD3640 power and input connections omitted for clarity. The ADDR pin selects the I2C address.

Figure 12. Connecting Multiple GD30AD3640 Devices

9 Power Supply Recommendations

The device requires a unipolar power supply, VDD, to power the analog and digital circuits of the device.

9.1 Power Supply Timing

Wait approximately 50μs after VDD stabilizes before communicating with the device to complete the power-on reset process.

9.2 Power Supply Decoupling

Good power supply decoupling is important to achieve optimal performance. VDD must be decoupled using at least a 0.1μF capacitor as shown in Figure 13. The 0.1μF bypass capacitor provides the instantaneous burst of additional current required from the power supply when the device is switching. Place the bypass capacitor as close to the device's power pins as possible using low impedance connections. Use multilayer ceramic chip capacitors (MLCCs) with low equivalent series resistance (ESR) and inductance (ESL) characteristics for power supply decoupling. For very sensitive systems or systems in harsh noisy environments, avoid using vias to connect capacitors to device pins to improve noise immunity. If vias must be used to connect capacitors to device pins, it is recommended to use multiple vias in parallel to reduce the overall inductance.

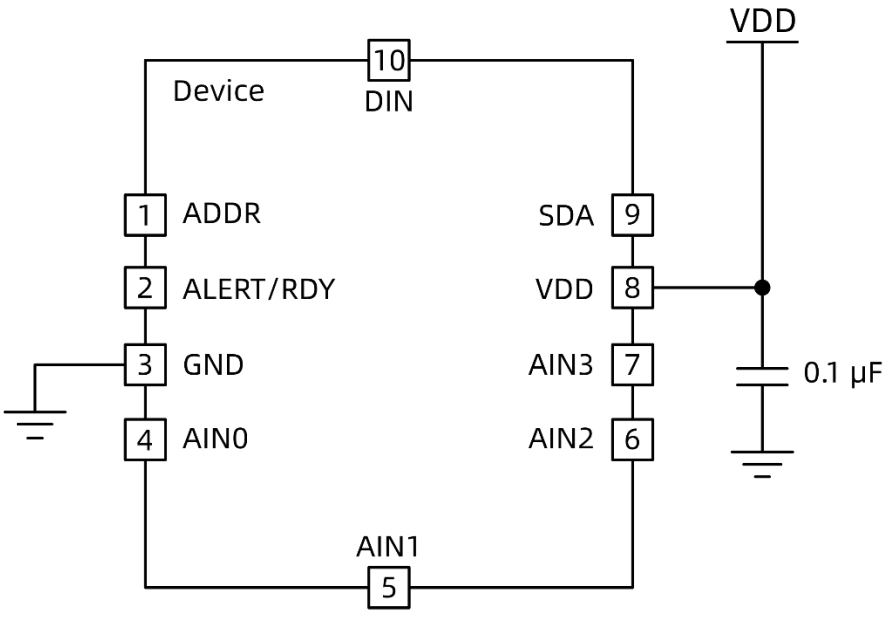


Figure 13. GD30AD3640 Power Supply Decoupling

10 Layout

10.1 Layout Guide

Employ best design practices when laying out the printed circuit board (PCB) for analog and digital components. For optimal performance, separate analog components [such as ADCs, amplifiers, references, digital-to-analog converters (DACs), and analog MUXs] from digital components [such as microcontrollers, complex programmable logic devices (CPLDs), field programmable gate arrays (FPGAs), radio frequency (RF) transceivers, universal serial bus (USB) transceivers, and switching regulators]. Figure 14 shows an example of good component placement. While Figure 14 provides a good example of component placement, the optimal placement for each application depends on the geometry, components, and PCB manufacturing capabilities employed. That said, no one layout will work perfectly for every design, and careful consideration must always be made when designing with any analog component.

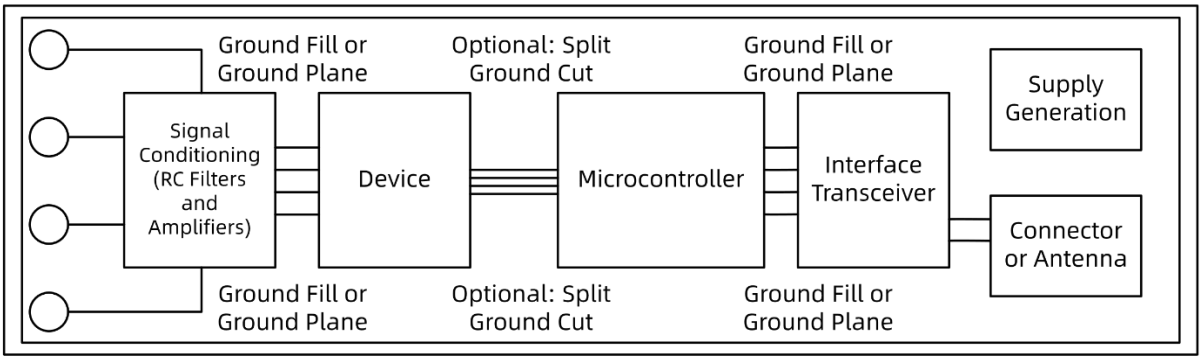


Figure 14. System Component Placement

Outlined below are some basic recommendations for the GD30AD3640 layout to get the best performance from the ADC. A good design can be ruined by poor circuit layout.

Separate analog and digital signals. First, divide the board into analog and digital sections as the layout allows. Keep digital lines away from analog lines. This prevents digital noise from coupling back into the analog signals.

Fill empty areas on signal layers with ground.

Provide a good ground return path. Signal return current flows on the path of least impedance. If the ground plane is cut or there are other traces preventing current from flowing next to the signal trace, it must find another path to return to the source and complete the circuit. If it is forced into a larger path, it increases the chance of signal radiation. Sensitive signals are more susceptible to EMI interference.

Use bypass capacitors on the power supplies to reduce high frequency noise. Do not place vias between the bypass capacitors and active devices. Placing bypass capacitors on the same layer close to active devices yields the best results.

Consider the resistance and inductance of the wiring. In general, the resistance of the input trace reacts with the input bias current and causes additional error voltage. Reduce the loop area enclosed by the source signal and return current to reduce the inductance in the path. Reduce inductance to reduce EMI pickup and reduce the high-frequency impedance seen by the device.

The two inputs going into the measurement source must be matched differential inputs.

Analog inputs with differential connections must place a capacitor at the input differentially. The best input combination for differential measurements uses adjacent analog input lines, such as AIN0, AIN1 and AIN2, AIN3. The differential capacitor must be of high quality. The best ceramic chip capacitor is C0G (NPO), which has stable characteristics and low noise characteristics.

10.2 Layout Examples

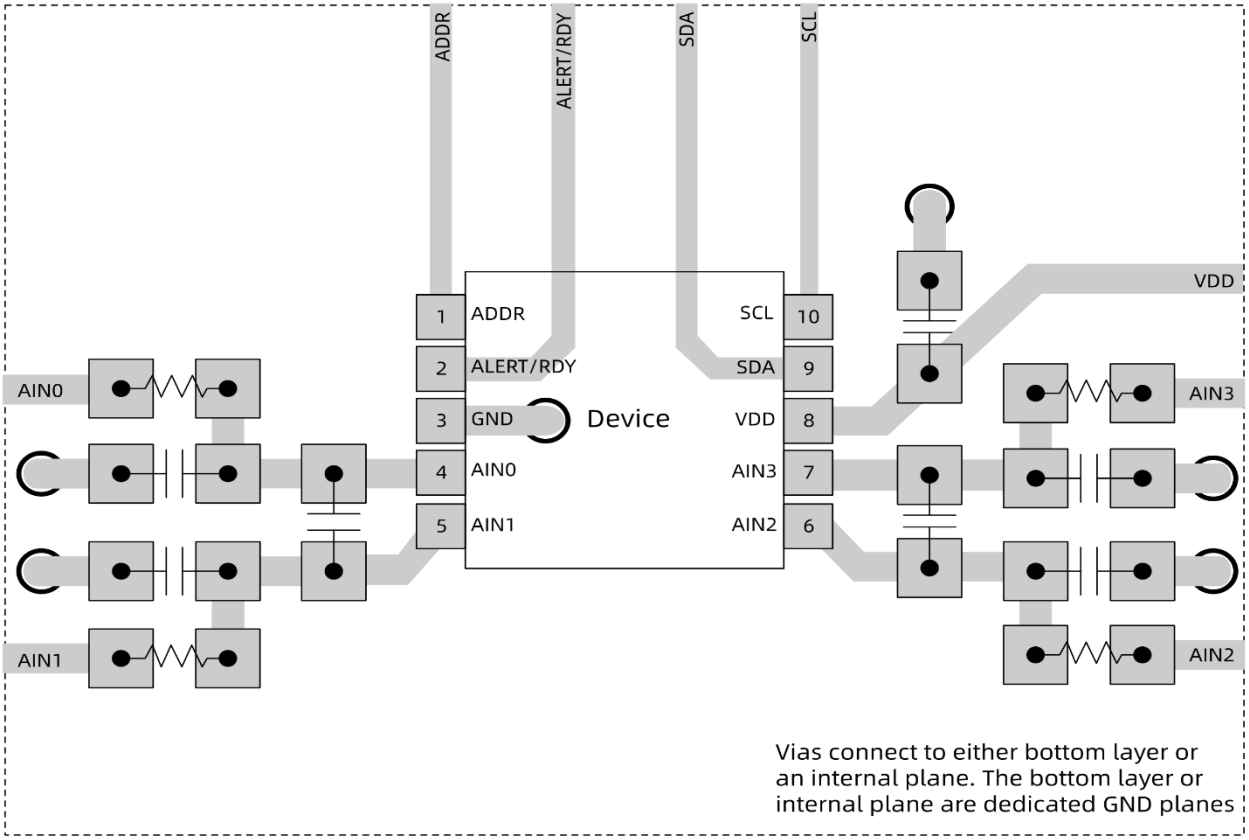
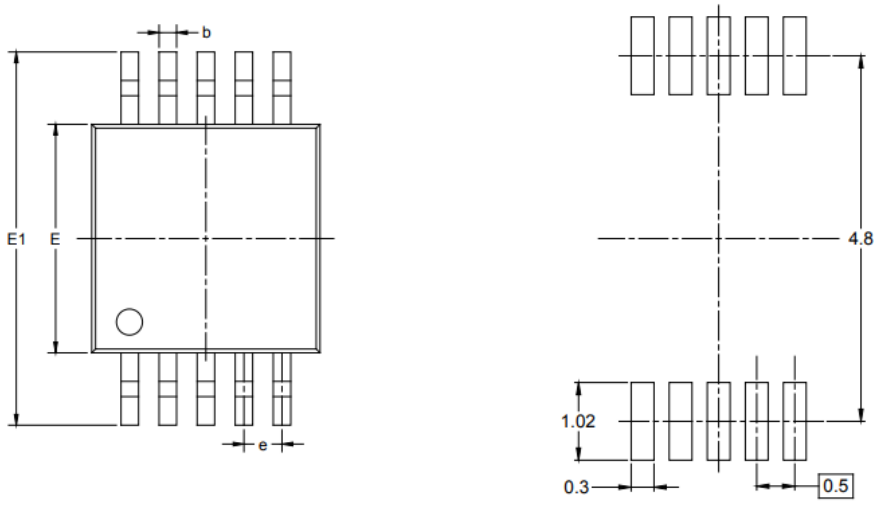


Figure 15. GD30AD3640 MSOP-10 Package

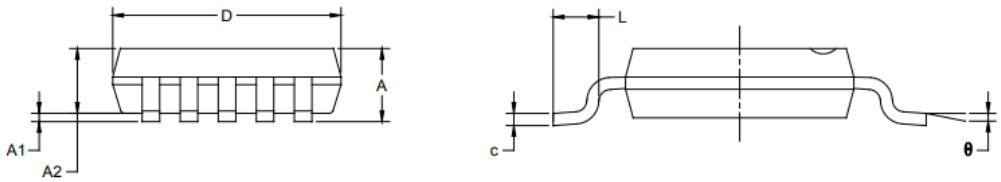
11 Packaging Information

11.1 Outline Dimensions

MSOP-10 Package



RECOMMENDED LAND PATTERN (Unit: mm)



Note :

1. All dimensions are in millimeters.
2. Package dimensions does not include mold flash, protrusions, or gate burrs.
3. Refer to Table 15. *MSOP-10 Dimensions (mm)*.

Table 15. MSOP-10 Dimensions (mm)

SYMBOL	MIN	TYP	MAX
A	0.820		1.100
A1	0.020		0.150
A2	0.750		0.950
b	0.180		0.280
c	0.090		0.230
D	2.900		3.100
E	2.900		3.100
E1	4.750		5.050
e	0.500 BSC		
L	0.400		0.800
θ	0°		6°

12 Ordering Information

Ordering Code	Package Type	ECO Plan	Packing Type	MOQ	OP Temp(°C)
GD30AD3640AMTR-I	MSOP10	Green	Reel	3000	−40°C to +125°C

13 Revision History

REVISION NUMBER	DESCRIPTION	DATE
1.0	Initial release and device details	2024

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