4.5V to 18V, 6A Synchronous Step Down Converter

1 Features

- Input Voltage Range: 4.5V to 18V
- Split Power Rail: 1.6V to 18V on PVIN
- 6A Constant Output Current
- 0.6V ±1% Voltage Reference Over Temperature
- Low 2.1μA Shutdown Quiescent Current
- Integrated 21mΩ / 16mΩ MOSFETs
- 200KHz to 1.6MHz Switching Frequency
- Synchronizes to External Clock
- Internal Soft-Start Limits the Inrush Current
- Cycle-by-Cycle Current Limit
- Hiccup for Overload and Over Temperature Protection
- Adjustable Slow Start/Power Sequencing
- Power Good Output Monitor
- Available in a QFN14 Package
- RoHS Compliant and Halogen-Free

2 Applications

- High Density Distributed Power System
- High Performance Point of Load Regulation
- Broadband, Networking and Optical Communication Infrastructure

3 Description

The GD30DC1309 is a highly efficient integrated power MOSFET synchronous buck DC-DC converter with a 4.5V to 18V wide input supply delivering up to 6A output current.

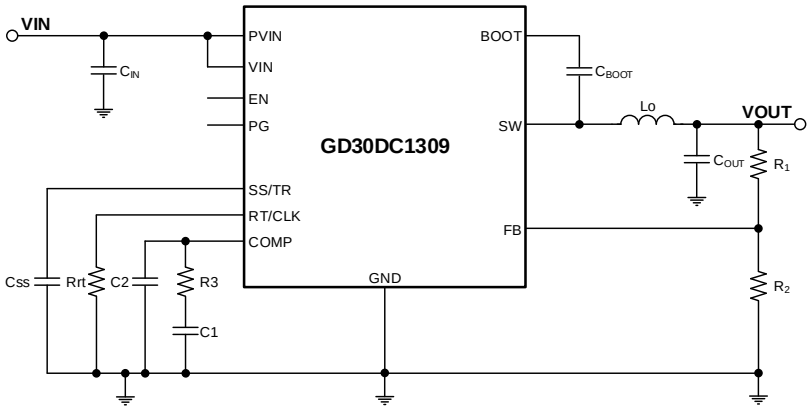
The GD30DC1309 current mode architecture with external compensation allows optimization of transient response over a wide range of loads and output capacitors. Cycle by cycle current limit provides protection against short-circuited output, soft start eliminates input surges during startup, and SS/TR pins can be used to control the output voltage to startup ramp or as an input for tracking. In addition, correctly configuring the Enable (EN) pin signal with the open drain power good (PG) pin signal also realizes multiple power supply sequence. When the device junction temperature exceeds the thermal shutdown temperature, the thermal shutdown protection is activated to prevent the device damaged.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
GD30DC1309	QFN14	3.50mm x 3.50mm

1. For packaging details, see *Package Information* section.

Simplified Application Schematic



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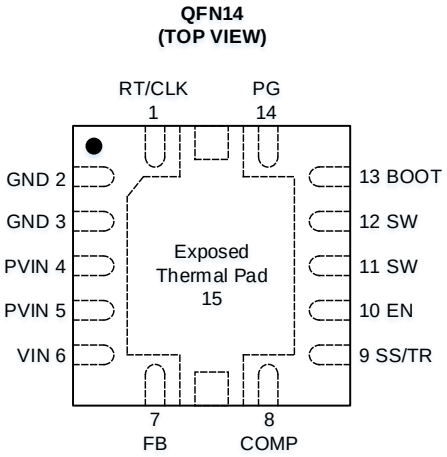
4 Device Overview

4.1 Pinout and Pin Assignment



4.2 Pin Description

PIN NUMBER		TYPE[1]	FUNCTION
NAME	NUM		
RT/CLK	1	I	RT Programming Resistor and External CLK Input. In RT mode, connecting a resistor from this pin to GND set the switching frequency; In CLK mode, the device synchronize to an external clock.
GND	2,3	G	Power ground of the device.
PVIN	4,5	P	Power Input. Supplies the power switches of the device.
VIN	6	P	Supplies the control circuitry and internal reference of the power converter.
FB	7	I	Converter Feedback Input. Connect to output voltage with feedback resistor divider.
COMP	8	O	Error Amplifier Output. Connect frequency compensation to this pin to stabilize the control loop.
SS/TR	9	O	Soft-Start and Tracking Input. An external capacitor connected to this pin set the soft-start period. The voltage on this pin overrides the internal reference. It can be used for tracking and sequencing.
EN	10	I	Enable Pin. Float to enable or pull-down to disable. Adjust the input under-voltage lockout with two resistors.
SW	11,12	O	Switch Node. Connected to the internal MOSFET switches and inductor terminal.
BOOT	13	O	Supply input for the high-side MOSFET gate drive circuit. Connect a 0.1-μF capacitor between BOOT and SW pins.
PG	14	G	Power Good Indicator Open-drain Output pin. See the *Power Good (PG)* section for more details.
Exposed Thermal Pad	15	G	Thermal pad of the package. The thermal pad must be soldered to a large PCB and connected to GND for minimum power dissipation.

1. I = input, P = power, G = Ground.

5 Parameter Information

5.1 Absolute Maximum Ratings

Exceeding the operating temperature range(unless otherwise noted)[1]

	PARAMETER	MIN	MAX	UNIT
Input Voltage	VIN	−0.3	20	V
	PVIN	−0.3	20	V
	BOOT	−0.3	27	V
	EN	−0.3	6	V
	PG	−0.3	6	V
	RT/CLK	−0.3	6	V
	FB	−0.3	3	V
	COMP	−0.3	3	V
	SS/TR	−0.3	3	V
Output Voltage	BOOT-SW	0	5.5	V
	SW	−1	20	V
	SW-10ns	−3	20	V
Source Current	RT/CLK	−100	100	μA
	SW	Current Limit		A
Sink Current	SW	Current Limit		A
	PVIN	Current Limit		A
	COMP	−200	200	μA
	PG	−0.1	5	mA
T_J	Operating junction temperature	−40	150	°C
T_{stg}	Storage temperature	−55	150	°C

1. The maximum ratings are the limits to which the device can be subjected without permanently damaging the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

5.2 Recommended Operation Conditions

SYMBOL[1,2]	PARAMETER	MIN	TYP	MAX	UNIT
VIN	VIN operating Input voltage	4.5		18	V
PVIN	PVIN operating input voltage	1.6		18	V
I_{OUT}	Output current	0		6	A
T_J	Operating junction temperature	−40		125	°C

1. The device is not guaranteed to function outside of its operating conditions.
2. Refer to the *Application Information* section for further information.

5.3 Electrical Sensitivity

SYMBOL	CONDITIONS	VALUE	UNIT
$V_{ESD(HBM)}$	Human-body model (HBM), ANSI/ESDA/JEDEC JS-001-2017[1]	±2000	V
$V_{ESD(CDM)}$	Charge-device model (CDM), ANSI/ESDA/JEDEC JS-002-2022[2]	±500	V

1. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
2. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.4 Thermal Resistance

SYMBOL[1]	CONDITIONS	QFN14	UNIT
Θ_{JA}	Natural convection, 2S2P PCB	TBD	°C/W
Θ_{JB}	Cold plate, 2S2P PCB	TBD	°C/W
$\Theta_{JC(top)}$	Cold plate, 2S2P PCB	TBD	°C/W
Ψ_{JB}	Natural convection, 2S2P PCB	TBD	°C/W
Ψ_{JT}	Natural convection, 2S2P PCB	TBD	°C/W
$\Theta_{JC(Bottom)}$	Cold plate, 2S2P PCB	TBD	°C/W

1. Thermal characteristics are based on simulation, and meet JEDEC document JESD51-7.

5.5 Electrical Characteristics

T_J = −40°C to 150°C, VIN = 4.5 to 18V, PVIN = 1.6V to 18V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY(VIN AND PVIN PINS)						
V_{PVIN}	PVIN operating input voltage		1.6		18	V
V_{VIN}	VIN operating input voltage		4.5		18	V
I_Q	Quiescent current	No switching		750	850	μA
I_{SHDN}	Shutdown current	EN = 0V		2.1	5	μA
V_{UVLO}	Under voltage lockout	V_{IN} rising		4	4.5	V
V_{UVLO_HYS}	Under voltage lockout hysteresis			150		mV
ENABLE(EN PIN)						
V_{EN_RISE}	Rising enable threshold			1.21	1.26	V
V_{EN_FALL}	Falling enable threshold		1.1	1.17		V
I_{EN}	EN input current	V_{EN} = 1.1V		1.15		μA
I_{HYS}	Hystersis current	V_{EN} = 1.3V		3.4		μA
VOLTAGE REFERENCE						
V_{FB}	Feedback voltage	0A≤IOUT≤6A	0.594	0.6	0.606	V
INTEGRATED POWER MOSFETS						
	High-side FET on resistance	Measured at pins		21	46	mΩ
	Low-side FET on resistance	Measured at pins		16	36	mΩ

Electrical Characteristics(continued)

T_J = −40°C to 150°C, VIN = 4.5 to 18V, PVIN = 1.6V to 18V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
ERROR AMPLIFER(EA)						
Gm	Error amplifier transconductance	−2μA<Icomp<2μA, Vcomp=1V		1300		μA/V
A_{DC}	Error amplifier DC gain	V_{FB} = 0.6 V	1000	3100		V/V
	Error amplifier Source/Sink	Vcomp = 1 V,100mV input overdrive		±110		μA
	Start switching threshold			0.36		V
	COMP to I_{SWITCH} gm			16		A/V
CURRENT LIMIT						
	High-side current limit threshold[1]			16		A
	Low-side switch sourcing current limit[1]			11		A
	Low-side switch sinking current limit[1]			3		A
	Hiccup wait time			512		Cycles
	Hiccup time before restart			16384		Cycles
THERMAL SHUTDOWM						
T_{TSD}	Thermal shutdown temperature			160		°C
T_{HYS}	Thermal shutdown hysteresis			10		°C
	Thermal shutdown hiccup time			16384		Cycles
TIMING RESISTOR AND EXTERNAL CLOCK(RT/CLOCK PIN)						
f_{SW}	Minimum switching frequency	R_{rt} = 240K(1%)	160	200	240	KHz
	Switching frequency	R_{rt} = 100K(1%)	400	480	560	KHz
	Maximum switching frequency	R_{rt} = 29K(1%)	1440	1600	1760	KHz
	Minimum pulse width			20		ns
	RT/CLK high threshold				2	V
	RT/CLK low threshold		0.8			V
	RT/CLK falling edge to SW rising edge dealy	Measured at 500KHz with RT resistor in series		70		ns
	Switching frequency range(RT mode set point and PLL mode)		200		1600	KHz
SWITCHING REGULATOR (SW PIN)						
t_{ON_MIN}	Minimum on time	Measured at 90% of VIN, 25°C, I_{SW} = 2A		105	145	ns
t_{OFF_MIN}	Minimum off time	BOOT-SW ≥ 3V		0		ns
BOOT(BOOT PIN)						
	BOOT-SW UVLO			2.1	3	V

Electrical Characteristics(continued)

T_J = −40°C to 150°C, VIN = 4.5 to 18V, PVIN = 1.6V to 18V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
SOFT-START AND TRACKING(SS/TR PIN)						
I_{SS}	SS charge current			2.3		μA
$V_{SSOFFSET}$	SS/TR to VFB matching	V_{SS_TR} = 0.4V		20	60	mA
POWER GOOD(PG PIN)						
	V_{FB} threshold	Falling		92		$\%V_{REF}$
	V_{FB} rising(Good)	Rising		94		$\%V_{REF}$
	V_{FB} rising (Fault)	Rising		106		$\%V_{REF}$
	V_{FB} falling(Good)	Falling		104		$\%V_{REF}$
	Output high leakage	V_{FB} = V_{REF}, V_{PG} = 5.5V		30	100	nA
	Output low	I_{PG} = 2mA			0.41	V
	Minimum VIN for valid output	V_{PG} < 0.5V at 100μA		0.6	1.5	V
	Minimum SS/TR voltage for PG				1.4	V

6 Functional Description

6.1 Block Diagram

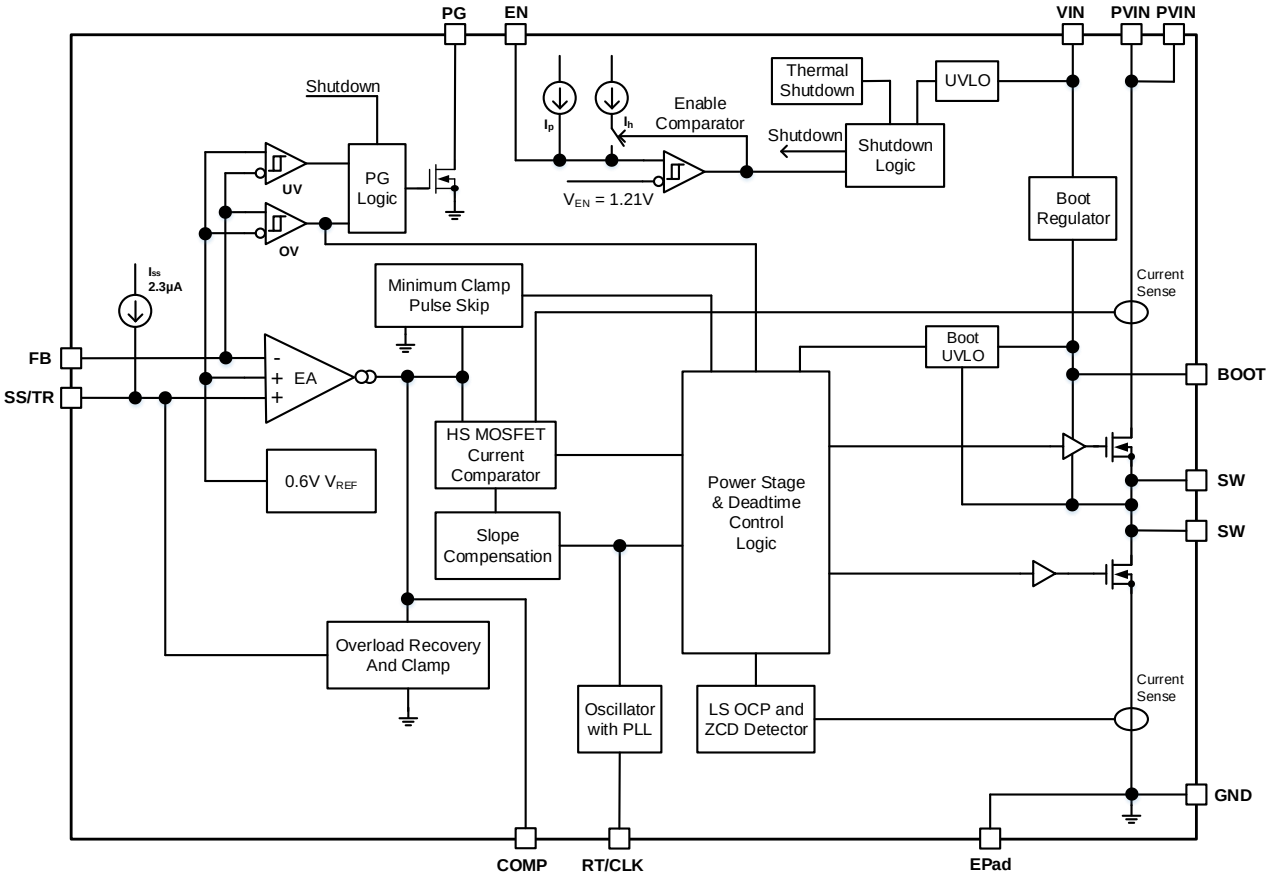


Figure 1. GD30DC1309 Functional Block Diagram

6.2 Operation

The GD30DC1309 is an integrated two n-channel power MOSFETs high efficiency synchronous buck converter with a 4.5V to 18V wide input supply that delivers up to 6A output current. The minimum output voltage of the device is equal to the internal reference voltage (0.6V typical). The device implements a constant frequency, peak current mode control which improve the performance of the dynamic response of the circuit, and the wide switching frequency range from 200KHz to 1600KHz optimizes the efficiency and size of the converter.

A resistor is placed between the RT/CLK pins to the ground to adjust the internal switching frequency. In addition, the device's internal phase-locked loop (PLL) is able to synchronize the switching frequency to the external clock falling edge.

The device has a safe monotonic start under the condition of output pre-bias. If the VIN is greater than V_{IN_UVLO}(4.0V typical), the system power up by default. The EN internal pull-up current source and two divider resistors (connected to VIN or PVIN to GND) can adjust the UVLO threshold. In addition, the device is enabled when the EN pin is externally pull-up or floating, and the device quiescent current (no switching and without load) is about 633μA. When the device is turned off, the power shutdown current is generally less than 2.1μA.

The integrated MOSFET has been dimensional adjusted to improve the efficiency of the power supply at low duty cycle and can continuously output up to 6A.

The bias voltage of the integrated high-side MOSFET is provided by the BOOT capacitor between the BOOT and SW pins. The BOOT capacitor voltage is monitored by the BOOT-SW UVLO. If the BOOT capacitor voltage is higher than the BOOT-SW UVLO (2.1V typical), the device can operate at 100% duty cycle and the output voltage can be reduced to a reference voltage. If the BOOT capacitor voltage is lower than the BOOT-SW UVLO, allowing the SW pin to be pulled low to recharge the boot capacitor.

The device has a power good (PG) open-drain output pin that indicates the state of the output voltage by comparing the FB voltage with the internal reference voltage. It is pulled down when the FB pin voltage is less than or greater than 92% or 106% of the reference voltage V_{REF}, and it remains high when the FB pin voltage is 94% to 104% of V_{REF}.

The SS/TR(Soft Start/Tracking Input) pin uses a low-value capacitor to minimize inrush current or a resistance divider using the front voltage rail during power-up for power sorting. When the power supply is used in tracking mode, it is the input pin that follows the output voltage.

GD30DC1309 has output overvoltage protection, overcurrent protection and thermal shutdown functions. The device uses the overvoltage detection circuit to reduce the output voltage transient effectively. When an output overvoltage occurs, the high-side MOSFET is forced turn off and allowed to turn on again only if the VOUT falls below 104% of its nominal value. The device implements both high-side MOSFET overload protection and bidirectional low-side MOSFET overload protection, which help to control inductor current and avoid current runaway.

If the junction temperature is above the thermal shutdown trip point (T_{SD}, 160°C), the device will also shut down. When the junction temperature drops by 10°C(T_{HYS}), the device restarts automatically under the control of the soft start circuit.

6.2.1 Constant Frequency PWM

The GD30DC1309 can be adjusted to a fixed frequency by setting an external resistor or synchronizing an external clock. By adopting the peak current control mode, the output of the error amplifier is transformed into the current reference, which is compared with the current of the high-side power switching. The high-side MOSFET turn on until the switching power supply current signal reaches the comp voltage determined by the EA. If the switching current does not reach the reference value generated from the COMP voltage at the end of one cycle, the high-side switch turn on for the next cycle until the current meets the reference value. When the power switch current reaches the current reference generated by the Comp voltage level, the high-side power switch is turned off and the low-side power switch is turned on.

6.2.2 Continuous Current Mode Operation (CCM)

Under all load conditions, the device normally operates in continuous conduction mode (CCM) (forced PWM). For light loads, when the low-side switch is turned on, the inductor current can be negative. If the current reaches the valley current limit, the low-side switch will be forced to turn off.

6.2.3 VIN and PVIN Pins

The device allows VIN and PVIN pins can be used together or separately for a variety of applications. The VIN pin voltage supplies the internal control and reference circuitry of the device. The PVIN pin voltage provides the main power to device system and internal switches.

When VIN and PVIN pins are tied together, both pins can operate between 4.5V and 18V. When VIN and PVIN pins are used separately, VIN pins must be ranged from 4.5V to 18V, and PVIN pins can be as low as 1.6V to 18V. A voltage divider connected to the EN pin allows appropriate adjustment of the input voltage UVLO. Adjusting the input voltage UVLO on the PVIN pin helps provide consistent power up performance.

6.2.4 Reference Voltage

The voltage reference system produces a precise 0.6V reference voltage over temperature by scaling the output of a temperature stable bandgap circuit. The reference voltage tolerance over the whole temperature range is ±1%.

6.2.5 Output Voltage Setting

An external resistor divider is used to set output voltage according to Equation(1). By selecting R1 and R2, the output voltage is programmed to the desired value. Use resistors with 1% tolerance or better for good output accuracy. When the output voltage is regulated, the typical reference voltage at the FB pin is 0.6V (V_{REF}).

$$R1 = \frac{V_{OUT} - V_{REF}}{V_{REF}} \times R_2 \quad (1)$$

To ensure system performance, choose the value of resistors carefully. Since a large resistor make FB sensitive to noise and a small resistor increase power loss. Referring to the feedback resistor divider diagram of Figure 2, start with a 10kΩ for R2 and use Equation(1) to calculate R1. It can achieves a balance between system stability and low current consumption.

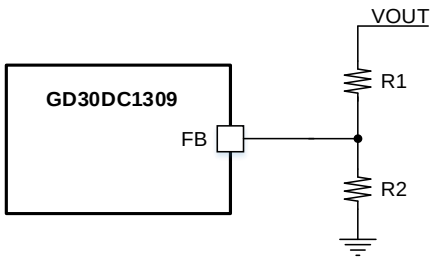


Figure 2. Feedback resistor divider diagram

6.2.6 Enable Operation

The EN pin provides electrical control to turn on/off the regulator. When VEN exceeds the threshold voltage 1.21V, the regulator starts operation. If VEN is below the shutdown threshold voltage 1.17V, the regulator shut down and enters to low quiescent current about 2.1μA.

Additionally, the EN pin, due to the pull-up current source inside the device, allows the user to enable the device when the EN pin floats. If the application needs to control the EN pin, an external MOSFET or BJT can be added to implement digital control from the EN pin to the ground.

To prevent the malfunction of too low supply voltage, the device implements an internal UVLO circuit on the VIN pin. The device is disabled when the VIN pin voltage is below the internal VIN UVLO threshold, and the internal VIN-UVLO hysteresis threshold is 150mV.

If an application requires either a higher UVLO threshold on the VIN pin or a secondary UVLO on the PVIN pin, even a UVLO on both the VIN and PVIN pins, then EN pin can be configured as shown in Figure 3, Figure 4 and Figure 5.

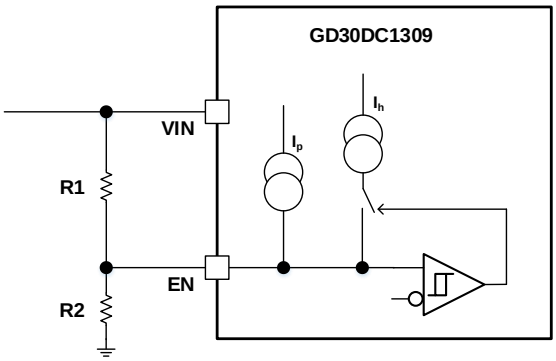


Figure 3. VIN UVLO Setting

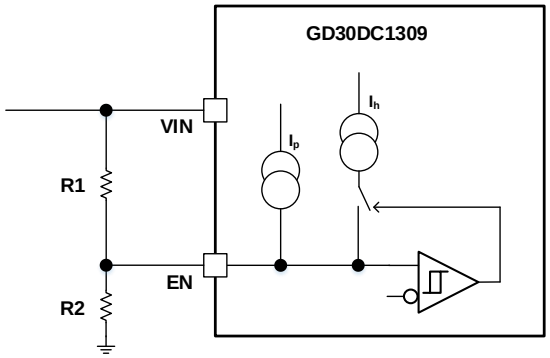


Figure 4. PVIN UVLO Setting (VIN≥4.5V)

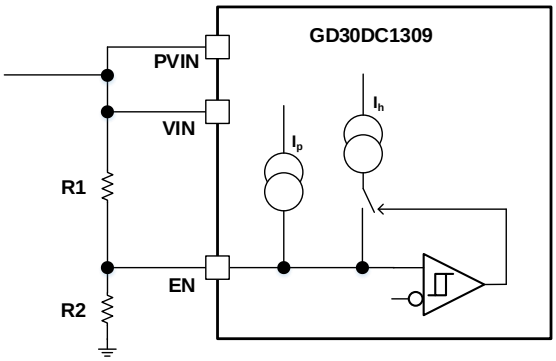


Figure 5. VIN and PVIN UVLO Setting

Without external components, the internal pull-up current Ip sets the EN pin default status to Enable. The pull-up current is also used to control the voltage hysteresis for the UVLO function, which increases Ih when the EN pin voltage exceeds the enable threshold.

The UVLO thresholds can be calculated using Equation(2) and Equation(3).

$$R1 = \frac{V_{START} \times (\frac{V_{EN\_FALLING}}{V_{EN\_RISING}}) - V_{STOP}}{I_p \times (1 - \frac{V_{EN\_FALLING}}{V_{EN\_RISING}}) + I_h} \quad (2)$$

$$R2 = \frac{R1 \times V_{EN\_FALLING}}{V_{STOP} - V_{EN\_FALLING} + R1 \times (I_p + I_h)} \quad (3)$$

Where I_h = 3.4μA, I_p = 1.15μA, V_{EN_RISING} = 1.21V, $V_{EN\_FALLING}$ = 1.17V

6.2.7 Soft-Start (SS/TR)

The device uses the lower voltage between the internal V_{REF} and SS/TR pins as the reference for regulator the output, the soft start time is programmed by the external capacitor between the SS/TR pin and GND, and an internal 2.3μA pull-up current source charges the external soft start capacitor. If a 10nF capacitor is used to set the soft-start, the period can be 4ms.The calculations for external charge capacitor C_{SS} and soft start time T_{SS} are shown in Equation :

$$T_{SS}(ms) = \frac{C_{SS}(nF) \times V_{REF}(V)}{I_{SS}(\mu A)} \quad (4)$$

Whre V_{REF} = 0.6V, I_{SS} = 2.3μA.

When the input voltage drops below the UVLO threshold of 1.21V or the OTP is triggered, the device stops switching and the SS/TR pin starts to discharge. During subsequent power-on, the device does not start switching until the shutdown event is cleared and the SS/TR pin has been discharged to the ground to ensure proper soft start behavior.

6.2.8 Pre-Bias Startup

The device is designed to prevent low-side MOSFET from discharging a pre-biased output. During monotonic pre-biased startup, the low-side MOSFET is not allowed to sink current as long as the SS/TR pin voltage is below 1.4V.

6.2.9 Adjustable Switching Frequency and Synchronization (RT/CLK)

The RT/CLK pin has two operating modes to set the switching frequency of the device.

In RT mode, a resistor (RT resistor) is connected between the RT/CLK pin and GND. The switching frequency of the device is adjustable from 200kHz to 1600kHz by placing a maximum of 240kΩ and minimum of 29kΩ, respectively.

In CLK mode, the external clock is directly connected to the RT/CLK pin and the internal switching frequency is synchronized with the CLK by the PLL. The CLK mode overrides the RT mode. The device automatically detects the external input clock and switches from RT mode to CLK mode.

6.2.10 Power Good (PG)

The power-good circuit monitors the voltage at the feedback pin to indicate the status of the output voltage, such as thermal shutdown, dropout, over voltage, EN shutdown, or during soft start. When the feedback pin voltage is lower than 92% or above 106% of the reference voltage, the PG pin open-drain output engages and pulls the PG pin close to GND. By connecting a pull-up resistor to an external supply, any downstream device can receive power-good as a logic signal that can be used for sequencing. Make sure that the external pull-up supply voltage results in a valid logic signal for the receiving device or devices. Using a pull-up resistor from 10kΩ to 100kΩ to a voltage source that is 5.5V or less is recommended. The state of PG is valid only if the VIN input voltage is greater than 1V. The PG achieves full current sinking capability when the VIN input voltage is above 4.5 V. Once the FB pin is between 94% and 104% of the internal voltage reference the PG pin pulled high.

6.2.11 Error Amplifier

The device has a trans-conductance amplifier as the error amplifier. The error amplifier compares the FB pin voltage to the lower of the SS/ TR pin voltage or the internal reference voltage (0.8V). The trans-conductance of the error amplifier in normal operation is 1300 μA/V typically. The frequency compensation components are placed internal between the output of the error amplifier and ground.

6.2.12 Slope Compensation

To ensures stability within a constant frequency architecture, the device adds a compensating slope to the signal of switch current, which prevents sub-harmonic oscillations when the duty cycles greater than 50%. Generally, the peak current of the inductor remains constant after slope compensation is added under the whole the duty

cycle range.

6.2.13 Output Over-Voltage Protection (OVP)

The device provides an output overvoltage protection(OVP) circuit to minimize output voltage overshoot when recovering from output fault conditions or strong unload transients. The OVP circuit minimizes overshoot by comparing the FB pin voltage to the OVP threshold. When the FB pin voltage is higher than 106% × V_{REF}, the high-side MOSFET will be forced off. When the FB pin voltage falls below 104% × V_{REF}, the high-side MOSFET will be enabled again.

6.2.14 High-Side MOSFET Over-Current Protection

The over-current protection(OCP) of high-side MOSFET is implemented in this device, which uses the COMP voltage output by the internal error amplifier to control the turn-off of high-side MOSFET on a cycle-by-cycle. Each cycle, the current reference generated by the internal COMP voltage is compared with the inductor current. If the peak current value exceeds the set current limit threshold, the high-side MOSFET is turns off.

6.2.15 Low-Side MOSFET Over-Current Protection

The device not only implements the high-side overcurrent protection, but also provides over source current protection and over sink current protection for low-side MOSFET. When the low-side MOSFET is turned on, the internal circuit continuously monitored the inductor current. In normal operation, the low-side MOSFET sources current to the load. At the end of every clock cycle, the low-side MOSFET sourcing current is compared to the sourcing current limit set internally. When the inductor valley current is higher than the source current limit, the high-side MOSFET is turned off, and the low-side MOSFET kept on for the next cycle. The high-side MOSFET turned on again only when the inductor valley current is below the source current limit at the start of a cycle as shown in Figure 6.

In some operating states, the low-side MOSFET may also sink current from the load. If the low-side MOSFET sink current exceeded the typical limit of 3A, the low-side MOSFET will be turned off immediately, in which case both MOSFETs remain off until the next cycle begins.

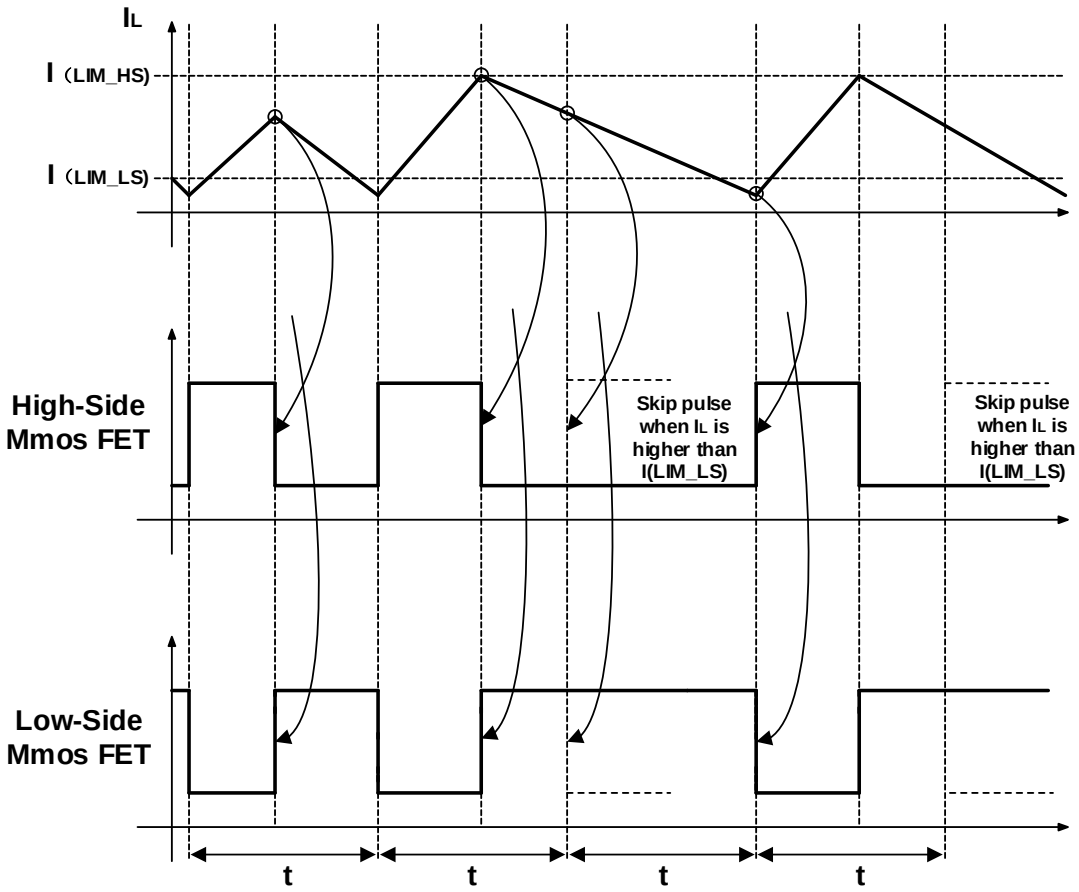


Figure 6. Overcurrent Protection for Both MOSFETs

6.2.16 Over-Temperature Protection

The internal thermal shutdown circuitry forces the device to stop switching if the junction temperature exceeds 160°C(typical), both the high-side and low-side FETs are turned off. Once the device temperature falls below the threshold with hysteresis 25°C (typical), the internal hiccup timer will start to count. The device returns to normal operation after the built-in thermal shutdown hiccup time(16384 cycles) is over.

6.2.17 Small Signal Model for Loop Response

The equivalent small signal model of the control loop is shown in Figure 7, which is conducive to the analysis of frequency response and transient response.

The trans-conductance amplifier as the error amplifier, and the compensation network (R3, C1 and C2) is placed at the EA output with a gm of 1300μA/V. The EA can be simplified as an ideal voltage-controlled current source. The resistance Roea (2.38MΩ) and capacitance Coea (20.7pF) model the open-loop gain and frequency response of the error amplifier. To measure the frequency response, the loop is broken at nodes a and b to insert a small 1mV AC signal. The a/c, c/b, and a/b represent power stage gain, frequency compensation gain, and loop gain, respectively. To measure the dynamic loop response, the load R_L can be replaced with a dynamic current source that can adjust the load step amplitude and step rate depending on the application.

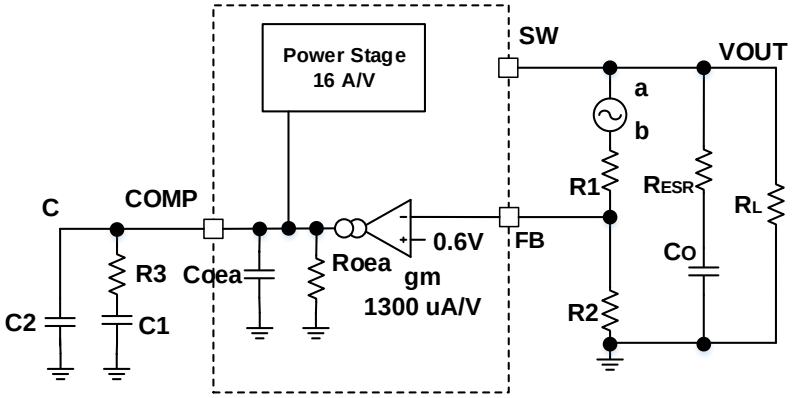


Figure 7. Small Signal Model for Loop Response

6.2.18 Simple Small Signal Model for Peak Current Mode Control

Figure 8 shows a simplified small-signal model for designing a frequency compensation network. The device power stage can be approximated as a volt-controlled current source (VCCS) providing current to the output capacitor and load resistor. The control-output transfer function is shown in Equation(5) and consists of a DC gain (Adc), a dominant pole (fp, see Equation(7)), and an ESR zero (fz, see Equation(8)). Power stage trans-conductance (gm_{ps}) is the ratio of the output current change to the control voltage (VCOMP) change, that is 16A/V for this device. Under resistive loads, the DC gain of the power stage is the product of gm_{ps} and the load resistance (R_L), as shown in Figure 9. As the load resistance decreases, the DC gain decreases. Since the dominant pole moves with the load resistance (see Equation(6)). As the increase of the load resistance, the gain increases and the pole frequency decreases, and the 0-dB crossover frequency is kept constant under different load conditions, making the frequency compensation design easier.

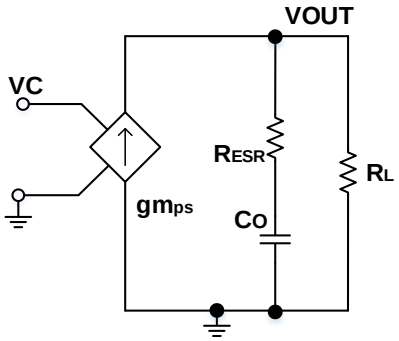


Figure 8. Small Signal Model for Loop Response

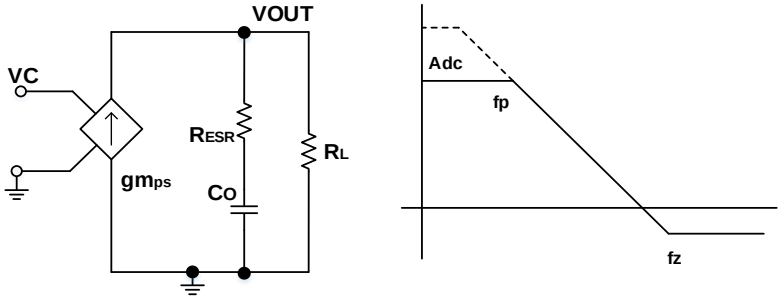


Figure 9. Small Signal Model for Loop Response

$$\frac{VOUT}{VC} = Adc \times \frac{(1+\frac{s}{2\pi \times fz})}{(1+\frac{s}{2\pi \times fp})} \quad (5)$$

$$Adc = gm_{ps} \times R_L \quad (6)$$

$$f_p = \frac{1}{C_O \times R_L \times 2\pi} \quad (7)$$

$$f_Z = \frac{1}{C_O \times R_{ESR} \times 2\pi} \quad (8)$$

Where

- gm_{ea} is the GM amplifier gain (1300μA/V).
- gm_{ps} is the power stage gain (16A/V).
- R_L is the load resistance.
- C_O is the output capacitance.
- R_{ESR} is the equivalent series resistance of the output capacitor.

6.2.19 Small Signal Model for Frequency Compensation

The GD30DC1309 supports two common Type II and Type III frequency compensation circuits, as shown in Figure 10. Type 2A compensation has an extra high frequency pole (by C2) to attenuate high frequency noise. In Type III, additional C11 capacitors is added in parallel at crossover frequency to the upper feedback resistance divider for phase boost. An extra resistor can be used in series with the C11 for better control of the phase boost.The following design guide is for advanced users who prefer to use the general method of compensation. The below equations only apply to designs whose ESR zero is higher than the bandwidth of the control loop. This usually applies to ceramic output capacitors. For low frequency ESR-zeros (High ESR capacitors), see the *Application Information* section.

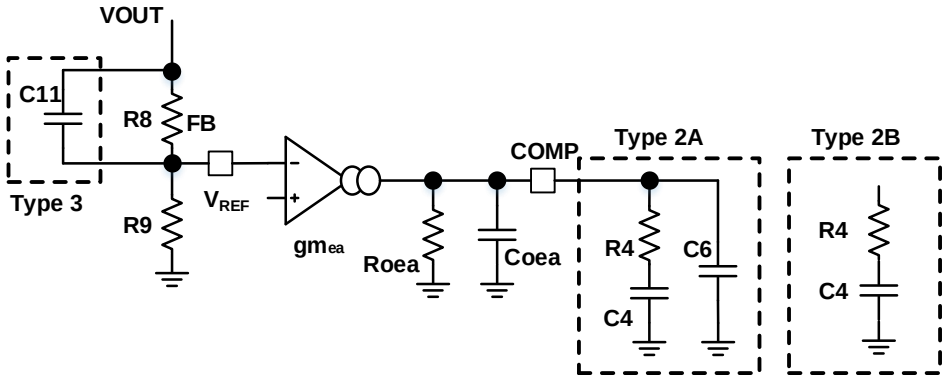


Figure 10. Types of Frequency Compensation

The general design guideline for device loop compensation are as follows:

1. Determine the crossover frequency, fc. A good starting point is 1/10th of the switching frequency, fsw.
2. R4 can be determined by:

$$R4 = \frac{2\pi \times fc \times V_{OUT} \times C_O}{gm_{ea} \times V_{REF} \times gm_{ps}} \quad (9)$$

Where:

- gm_{ea} is the GM amplifier gain (1300μA/V).
- gm_{ps} is the power stage gain (16A/V).
- V_{REF} is the reference voltage (0.6V)

3. Place a compensation zero at the dominant pole: $fp = \frac{1}{C_O \times R_L \times 2\pi}$

C4 can be determined by:

$$C4 = \frac{R_L \times C_O}{R_4} \quad (10)$$

4. C6 is optional. It can be used to cancel the zero from the ESR (Equivalent Series Resistance) of the output capacitor Co.

$$C6 = \frac{R_{ESR} \times C_O}{R_4} \quad (11)$$

5. Type III compensation can be implemented with the addition of one capacitor, C11. This allows for slightly higher loop bandwidths and higher phase margins. If used, C11 is calculated from Equation(12).

$$C11 = \frac{1}{2\pi \times R8 \times fc} \quad (12)$$

6.3 Device Mode Description

6.3.1 Switching Frequency Setting (RT Mode)

Selection of the operating frequency is a tradeoff between efficiency and component size. To determine the RT resistance for a given switching frequency, use Equation(13) or the curve Figure 11.

$$R_{rt}(k\Omega) = \frac{49187}{F_{SW}(kHz)} - 1(K\Omega) \quad (13)$$

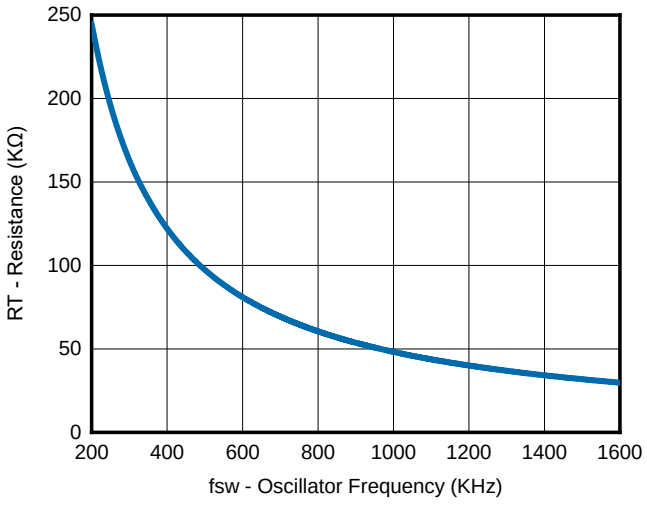


Figure 11. RT Set Resistor vs. Switching Frequency

6.3.2 Synchronization (CLK Mode)

The device uses an internal phase-locked loop (PLL) to allow the RT/SYNC pin to synchronize the external clock, ranging from 200KHz to 1.6MHz. The synchronous clock duty cycle must be from 20% to 80%, and the signal amplitude must be lower than 0.8V and higher than 2.0V. The start of the SW switching cycle is synchronized with the falling edge of the RT/SYNC pin signal.

When no external clock is present, the device operates in RT mode and at the original switching frequency set by the RT resistor. The CLK mode overrides the RT mode when a synchronous clock signal is provided. When the SYNC pin is pulled above the RT/CLK high threshold (2.0V) for the first time, the device switches modes. When the PLL begins to lock to the frequency of the external clock, the RT/CLK pin becomes a high-impedance state. Switching back to RT mode from CLK mode is not recommended because the internal switching frequency first drops to 100khz before returning to the switching frequency set by the RT resistor.

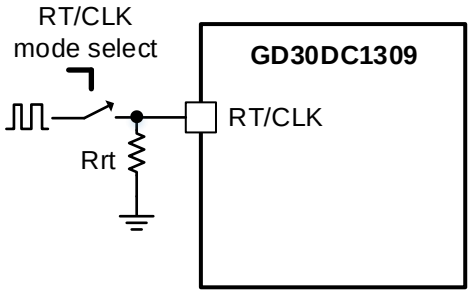


Figure 12. Using RT and CLK Modes Together

6.3.3 Bootstrap Voltage (BOOT) and Operation with Low Dropout (100% Duty Cycle)

The GD30DC1309 has an integrated BOOT regulator and requires a 0.1μF ceramic capacitor to be connected between the BOOT and SW pins to provide the gate drive voltage for the high-side MOSFET. A ceramic capacitor with of X7R or X5R grade is recommended to ensure stable characteristics over temperature and voltage ranges.

To improve dropout, the device is designed to operate at 100% duty cycle when the voltage from BOOT to SW pin is greater than the typical 2.1V value. When the voltage between BOOT and SW drops below the BOOT-SW UVLO threshold the high-side MOSFET is turned off and the low-side MOSFET is turned on allowing the boot capacitor to be recharged. In applications with split input voltage rails, 100% duty cycle operation can be achieved as long as (VIN – PVIN) > 4 V.

6.3.4 Startup Sequencing (SS/TR)

The different connections of SS/TR, EN, and PG pins enable a variety of common power sequencing methods.

Figure 13 shows a simple sequencing method using two GD30DC1309 devices, where the first device on the left is coupled to the EN pin of the second device on the right, enabling the second power supply when the first power supply reaches voltage regulation.

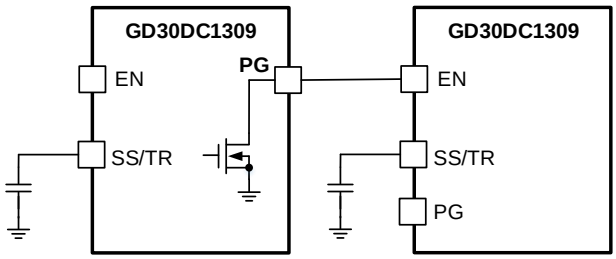


Figure 13. Sequential Start-Up Sequence

Figure 14 shows the method implementing ratiometric sequencing by connecting the SS/TR pins of the two devices together. The regulator output rises and reaches regulation at the same time. When calculating the slow start time, the pull-up current source must be doubled in Equation(4).

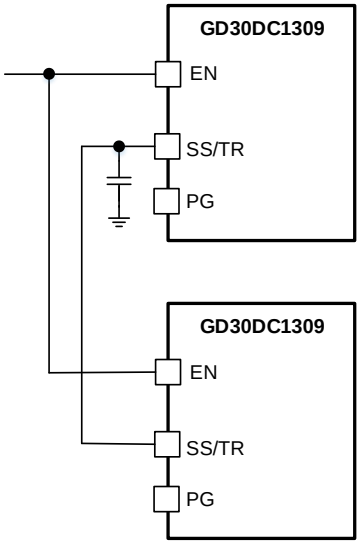


Figure 14. Ratiometric Start-Up Sequence

Ratiometric and simultaneous power supply sequencing can be implemented by using a resistor divider as shown in Figure 15.

In order to design a ratiometric start-up, the Equation(14) and Equation(15) calculate by selecting the appropriate R1 and R2 resistors VOUT2 can ramp up and achieve adjustment at the same rate as V_{OUT1} or at a slightly faster or slower rate. If VOUT2 adjustment is implemented in an application where V_{OUT2} is slightly lower than V_{OUT1}, the result of Equation(16) is positive. Otherwise, result is negative. When sequenced simultaneously, ΔV is zero. In order to reduce the effect of SS/TR inherent in the slow start circuit on the V_{FB} bias (vssofset, 29 mV) and the bias generated by the pull-up current source (I_{SS}, 2.3 μA) and tracking resistance, V_{SS_offset} and I_{SS} were included as variables in the Equation(17).

$$R1 = \frac{V_{OUT2} + \Delta V}{V_{REF}} \times \frac{V_{SS\_offset}}{I_{SS}} \tag{14}$$

$$R2 = \frac{V_{REF} \times R1}{V_{OUT2} + \Delta V - V_{REF}} \tag{15}$$

$$\Delta V = V_{OUT1} - V_{OUT2} \tag{16}$$

$$R1 > 2800 \times V_{OUT1} - 180 \times \Delta V \quad (17)$$

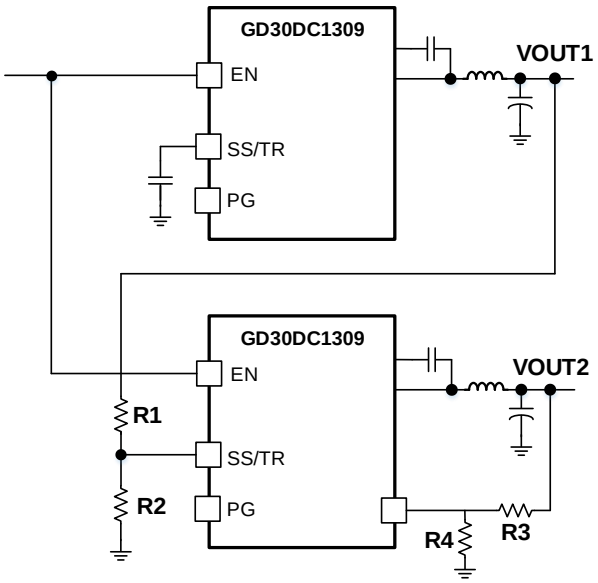


Figure 15. Ratiometric and Simultaneous Start-Up Sequence

7 Application Information

The schematic of a typical application circuit that is used for GD30DC1309 evaluation module is given in Figure 16.

7.1 Typical Application Circuit

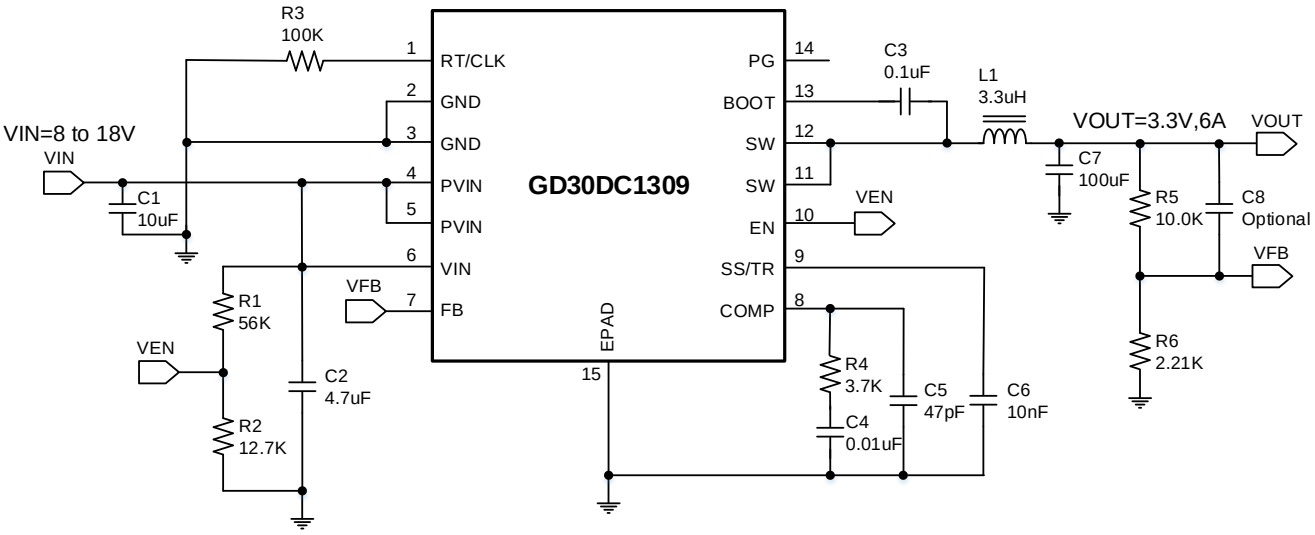


Figure 16. 3.3V, 6A Reference Design

7.2 Design Example

For this design example, use the parameters in Table 1.

Table 1. Design Parameters

PARAMETER	EXAMPLE VALUE
Input Voltage	8V to 18V, 12V(NOM)
Output Voltage	3.3V
Maximum Output Current	6A
Transient Response 1A load step	$\triangle V_{OUT}$ = 5%
Input Start-Up Voltage (Vin_rising)	6.54V
Input Shut-Down Voltage (Vin_falling)	6.07V
Switching Frequency	480KHz

Table 2 lists the recommended parameters values for common output voltages.

Table 2. Component selection for common output voltages

V_{OUT}(V)	R1(KΩ)	R1(KΩ)	R4(KΩ)	C4(pF)	C5(pF)	C7(μF)	L(μH)
5	10	1.37	3.7	47	10	100	3.3
3.3	10	2.21	3.7	47	10	100	3.3
2.5	10	3.16	3.7	47	10	100	3.3
1.8	10	4.99	3.7	47	10	100	3.3

7.3 Detailed Design Description

7.3.1 Operating Frequency

The first step in designing a switch power supply is usually to confirm the switching frequency of the regulator. A higher switching frequency allows the use of lower inductors and smaller inductors. However, higher switching frequency cause extra switching losses, resulting in lower regulator efficiency and thermal performance, so there is a trade-off between higher and lower switching frequencies. In this design, a moderate switching frequency of 480KHz is selected to achieve a small solution size and high-efficiency operation.

7.3.2 Inductor Selection

The inductor selection trade-offs among size, cost, efficiency, and transient response requirements. Three key inductor parameters are specified for operation with the device: inductance value (L), inductor saturation current (ISAT), and DC resistance (DCR). In general, inductors with larger inductance and low DCR values provide much more output and hight conversion efficiency, and smaller inductance values can give batter load transient response.

A good compromise between size and loss is to choose the peak-to-peak ripple current equals to 20% to 40% of the IC rated current. And the peak inductor current can be calculated by Equation(18) and Equation(19). Ensure that the peak inductor current is below the maximum switch current.

$$\Delta I_L = (0.2 \text{ to } 0.4) \times I_{OUT(MAX)} \tag{18}$$

$$I_{L(peak)} = I_{OUT(MAX)} + \frac{\Delta I_L}{2} \tag{19}$$

The switching frequency, input voltage, output voltage, and selected inductor ripple current determines the inductor value according to Equation(20). Once an inductor value is chosen, the peak inductor current is determined by Equation(19). Attention that the inductor should not saturate under the inductor peak current.

$$L = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN} \times F_{SW} \times \Delta I_L} \tag{20}$$

7.3.3 Input Capacitor Selection

Input capacitance, C_{IN}, is needed to filter the pulsating current at the drain of the high-side power MOSFET. C_{IN} should be sized to do this without causing a large variation in input voltage. The input capacitance value determines the input voltage ripple of the converter. For most applications, a 10μF capacitor is sufficient.

The peak-to-peak voltage ripple on input capacitor can be estimated with Equation(21):

$$\Delta V_{IN} = \frac{I_{OUT}}{F_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \tag{21}$$

For best performance, ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. To compensate the derating of the ceramic capacitors, the voltage rating of capacitor should be twice of the maximum input voltage. The input capacitor also requires an adequate

ripple current rating since it absorbs the input switching current.

The input ripple current can be estimated with Equation(22):

$$I_{CIN} = I_{OUT} \times \sqrt{D \times (1-D)} \quad (22)$$

Where D is the duty cycle of converter. The worst-case condition occurs at $V_{IN} = 2V_{OUT}$. At this point, the input ripple current of input capacitance is equal to half of output current. For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

7.3.4 Output Capacitor Selection

The output capacitor stabilizes the DC output voltage, it directly affects the steady state, output voltage ripple, loop stability, and output voltage overshoot and undershoot during load current transient.

The output voltage ripple can be estimated with Equation(23):

$$\Delta V_{OUT} = \Delta I_L \times \left(C_{ESR} + \frac{1}{8 \times F_{SW} \times C_{OUT}} \right) \quad (23)$$

The output capacitor ripple is essentially composed of two part. One part is caused by the inductor ripple current flowing through the ESR of output capacitors, another part is caused by the inductor ripple current charging and discharging output capacitors. For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. And when using ceramic capacitors, the capacitance dominates the impedance at the switching frequency and causes most of the output voltage ripple.

The output capacitance must be large enough to supply the current when a large load step occurs. But if the output capacitor value is too high, the output voltage will not be able to reach the design value during the soft start time. A 100μF ceramic capacitor is recommended in this application.

7.3.5 Soft-Start Capacitor Selection

The soft-start capacitor determines the minimum time required for the output voltage to reach the nominal programmed value of the device during power-up. In many applications, it is useful to control the slew rate of the output voltage. For example, the output capacitor is very large, and a large amount of current needs to be drawn from the input to quickly charge the capacitor to the output voltage level or excessive current drawn from the input power supply may lead to input voltage rail sag, you can also choose to adjust the output voltage slew rate to solve such problems. The soft-start capacitor value can be calculated by Equation. In this case, the output capacitance value is relatively small and the soft start time is not important because it does not require much charging at 3.3V output voltage. However, it is best to set a small arbitrary value, such as C_{SS} = 22nF, which results in a boot time of 6.6ms.

$$C5(nF) = \frac{T_{SS}(ms) \times I_{SS}(\mu A)}{V_{REF}(V)} \quad (24)$$

7.3.6 Bootstrap Capacitor Selection

A 0.1-μF ceramic capacitor (X5R or better grade dielectric) with 10V or higher voltage rating must be connected between the BOOT-SW pin for proper operation.

7.3.7 UVLO Setting

Undervoltage lock (UVLO) can be setted from a VIN or PVIN by an external voltage divider network. In this example design, when the input voltage is higher than 6.54V (Vin_rising), the power supply should turn on and begin switching. After the regulator starts working, the input voltage below 6.07V (Vin_falling) will turn off and stop switching. Equation(2) and Equation(3) can be used to calculate the resistors. For the stop voltages specified the nearest standard resistor value for R1 is 56kΩ and R2 is 12.7kΩ.

7.3.8 Minimum Output Voltage

Due to the internal of the GD30DC1309 has a minimum on-time limit, there is a minimum output voltage limit for any given input voltage, the output voltage cannot be less than the internal reference voltage (0.8V), above 0.8V, the minimum output voltage can be given by the Equation(25).

$$V_{OUT\_MIN} = t_{ON\_MIN} \times f_{s\_MAX} \left(V_{IN\_MAX} + I_{OUT\_MIN} \left(R_{DS2\_MIN} - R_{DS1\_MIN} \right) \right) - I_{OUT\_MIN} \left(R_L + R_{DS2\_MIN} \right) \quad (25)$$

Where

- V_{OUT_MIN} = minimum achievable output voltage.
- t_{ON_MIN} = minimum controllable on-time (135ns maximum).
- f_{s_max} = maximum switching frequency including tolerance.
- V_{IN_MAX} = maximum input voltage.
- I_{OUT_MIN} = minimum load current.
- R_{DS1_MIN} = minimum high-side MOSFET on-resistance (36 to 32 mΩ typical).
- R_{DS2_MIN} = minimum low-side MOSFET on-resistance (19 mΩ typical).
- R_L = series resistance of output inductor.

7.3.9 Loop Compensation Design

Several techniques are used by engineers to compensate a DC/DC regulator. The recommended calculation method here is quite simple and yields results with high phase margins. In this method the effects of the slope compensation are ignored.

Because of this approximation, the actual cross over frequency is usually lower than the calculated value.

First, the converter pole (fP) and ESR-zero (fZ) are calculated from Equation(26) and Equation(27). For COUT, the worst derated value of 75μF should be used. Equation(28) and Equation(29) can be used to find an estimation for closed-loop crossover frequency (fC) as a starting point (choose the lower value).

$$f_p = \frac{I_{OUT}}{2\pi \times V_{OUT} \times C_{OUT}} \quad (26)$$

$$f_Z = \frac{1}{2\pi \times R_{ESR} \times C_{OUT}} \quad (27)$$

$$f_{CO} = \sqrt{f_P \times f_Z} \quad (28)$$

$$f_{CO} = \sqrt{f_P \times \frac{f_{SW}}{2}} \quad (29)$$

Having the crossover frequency, the compensation network (R4 and C4) can be calculated. R4 sets the gain of the compensated network at the crossover frequency and can be calculated by Equation(31).

$$R_4 = \frac{2\pi \times f_{CO} \times V_{OUT} \times C_{OUT}}{gm_{EA} \times V_{REF} \times gm_{PS}} \quad (30)$$

C4 sets the location of the compensation zero along with R4. To place this zero on the converter pole, use Equation(31).

$$C_4 = \frac{V_{OUT} \times C_{OUT}}{I_{OUT} \times R_4} \quad (31)$$

From Equation(31) and Equation(31) the standard selected values are R4 = 3.7kΩ and C4 = 10nF.

A high frequency pole can also be added by a parallel capacitor if needed (not used in this example). The pole frequency can be calculated from Equation(32).

$$f_p = \frac{1}{2\pi \times R_4 \times C_5} \quad (32)$$

7.4 Power Dissipation

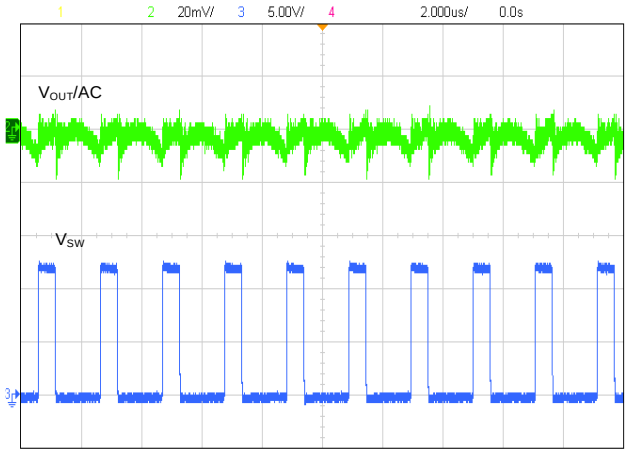
For DC/DC, these is still some power deposited on the chip and converted into heat, in spite of switch mode power supplies have considerably higher efficiency when compared to linear regulators. The device power dissipation includes conduction loss, switching loss, gate charge loss and quiescent current losses. The maximum allowable continuous power dissipation at any ambient temperature is calculated by Equation(33):

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{\theta_{JA}} \quad (33)$$

Where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature and θ_{JA} is the junction to ambient thermal resistance. Once exceeding the maximum allowable power, The device enters thermal shutdown to avoid permanent damage.

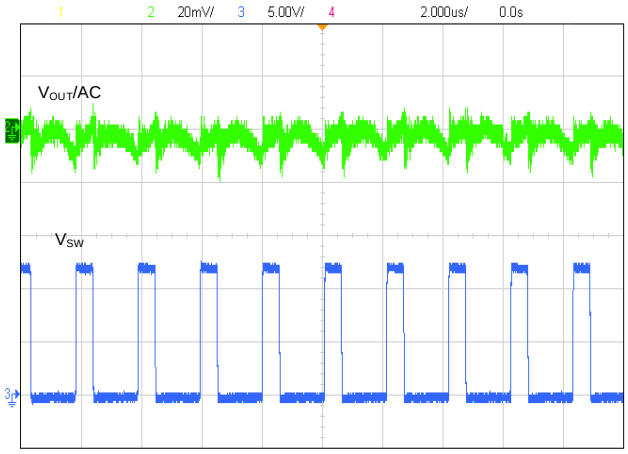
7.5 Typical Application Curves

V_{IN} = 12V, V_{OUT} = 3.3V, L = 3.3uH, T_A = 25°C, unless otherwise noted.



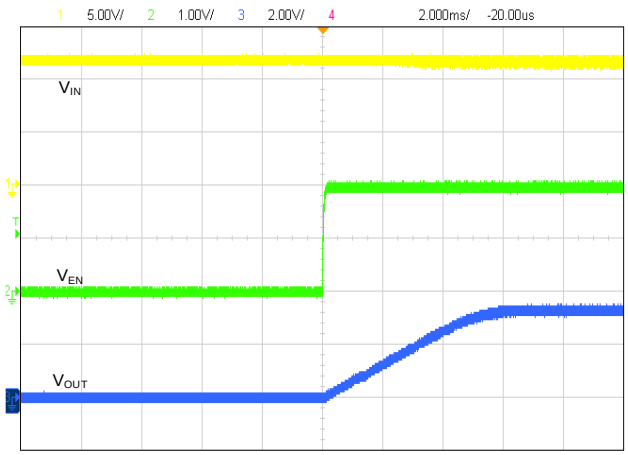
I_{OUT} = 0A

Figure 17. Output Ripple



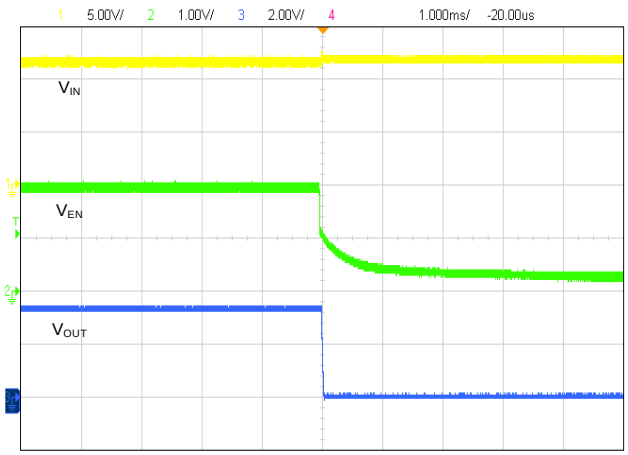
I_{OUT} = 6A

Figure 18. Output Ripple



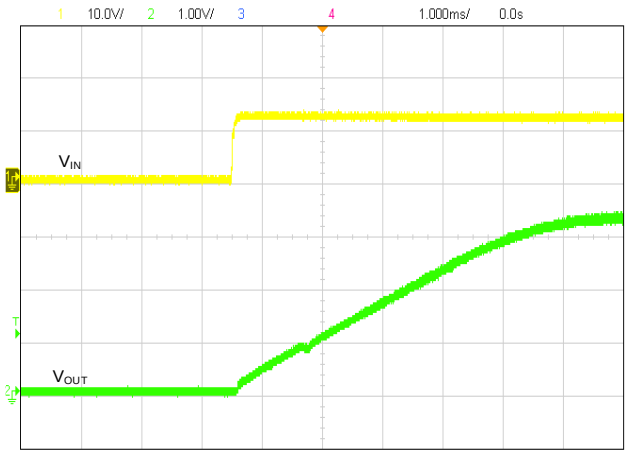
I_{OUT} = 6.0A

Figure 19. EN Startup with Load



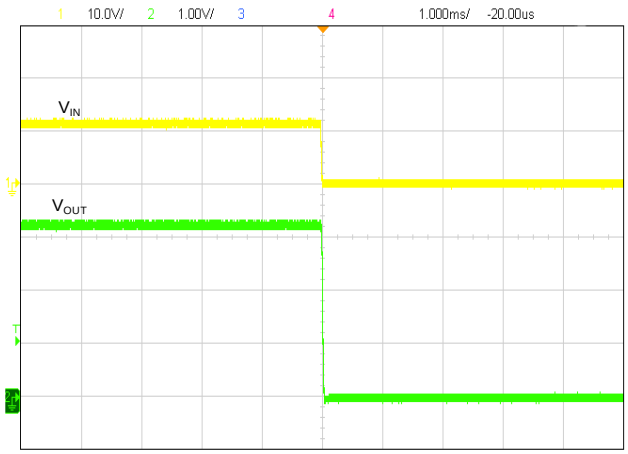
I_{OUT} = 6.0A

Figure 20. EN Shutdown with Load



I_{OUT} = 6.0A

Figure 21. VIN Startup with Load

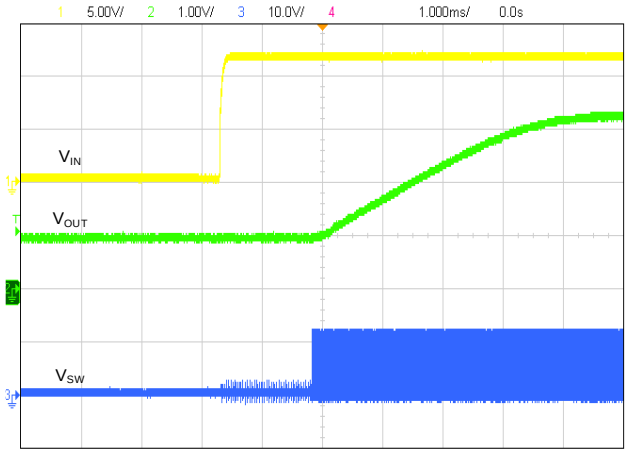


I_{OUT} = 6.0A

Figure 22. VIN Shutdown with Load

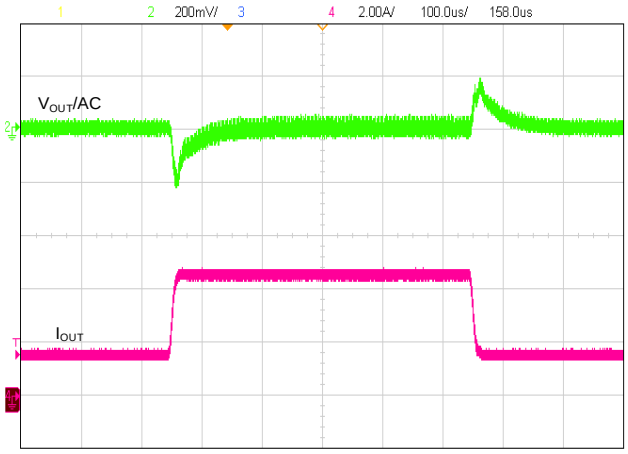
Typical Application Curves (continued)

V_{IN} = 12V, V_{OUT} = 3.3V, L = 3.3uH, T_A = 25°C, unless otherwise noted.



I_{OUT} = 2.0A

Figure 23. Pre-Bias Startup



I_{OUT} = 1.5A to 4.5A, 2.5A/us slew rate

Figure 24. Load Transient

8 Layout Guidelines and Example

Efficient PCB layout is critical for stable operation. For the high-frequency switching converter, a poor layout design can result in poor line or load regulation and stability issues.

- Make traces of the high current paths as short and wide as possible.
- Put the input capacitor as close as possible to the device pins (VIN and PVIN).
- The SW node encounters high frequency voltage swings so it should be kept in a small area. Keep sensitive components away from the SW node to prevent noise couple.
- Sensitive signals like FB, COMP, EN, RT/CLK traces must be placed away from high dv/dt nodes and not inside any high di/dt loop. The ground of these signals should be connected to GND pin and separated with power ground.
- The thermal pad should be connected to a strong ground plane for heat sinking and noise protection. For better power dissipation, adding thermal vias near thermal pad to connect between different layers is recommended.
- Connect PVIN, GND and exposed pad pins to large copper areas to increase heat dissipation and long-term reliability. Keep SW area small to avoid emission issue.

For best results, follow the layout example below.

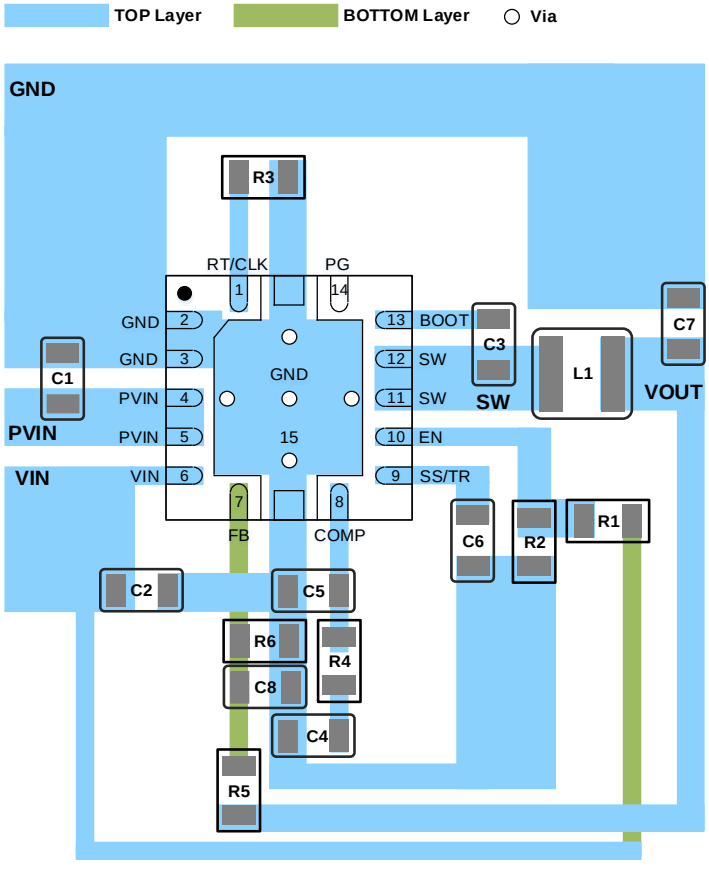
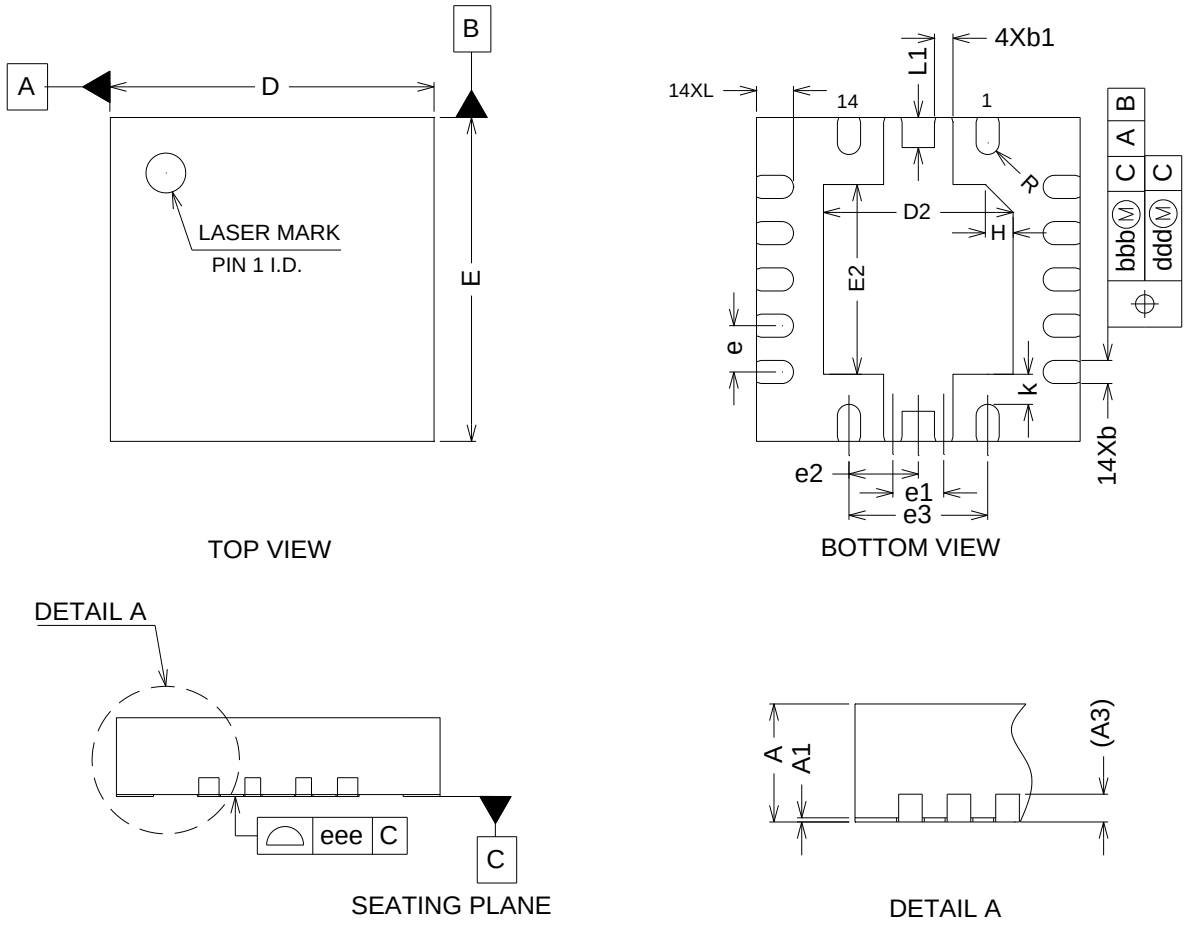


Figure 25. Typical GD30DC1309 Example Layout

9 Package Information

9.1 Outline Dimensions

QFN14 Package Outline



NOTES:

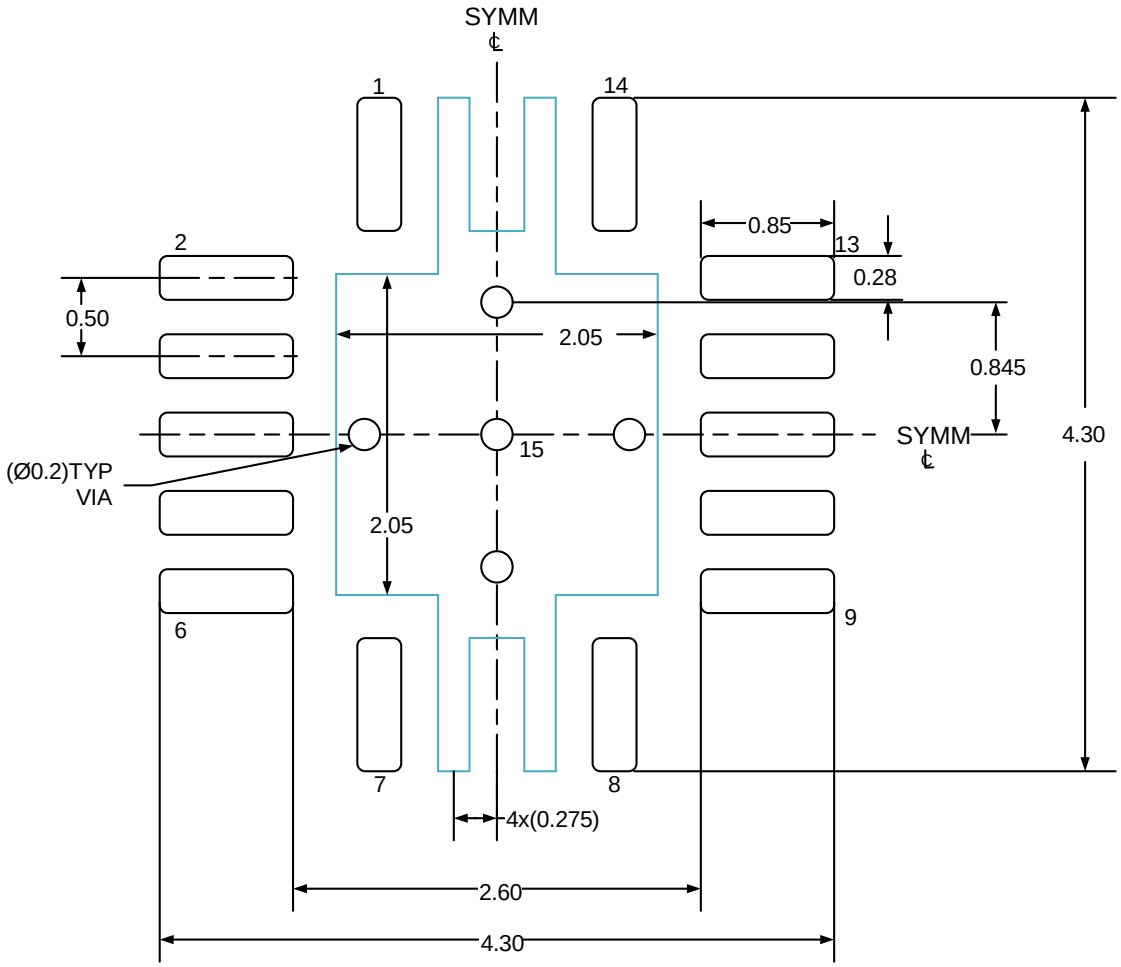
1. All dimensions are in millimeters.
2. Package dimensions does not include mold flash, protrusions, or gate burrs.
3. Refer to the Table 3 *QFN14 dimensions(mm)*.

Table 3. QFN14 dimensions(mm)

SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
A3		0.20 REF	
b	0.20	0.25	0.30
b1	0.15	0.20	0.25
D	3.40	3.50	3.60
E	3.40	3.50	3.60
D2	1.95	2.05	2.15
E2	1.95	2.05	2.15
e		0.50 BSC	
e1		0.55 BSC	
e2		0.75 BSC	
e3		1.50 BSC	
H		0.30 REF	
K	0.225	0.325	0.425
L	0.30	0.40	0.50
L1	0.225	0.325	0.425
R	0.09		
bbb		0.10	
ddd		0.05	
eee		0.08	

9.2 Recommended Land Pattern

QFN14 Land Pattern Example



NOTES: (continued)

1. Refer to the IPC-7351 can also help you complete the designs.
2. Exposed metal shown.
3. Drawing is 20X scale.

10 Ordering Information

Ordering Code	Package Type	ECO Plan	Packing Type	MOQ	OP Temp(°C)
GD30DC1309ZUTR-I	QFN14	Green	Tape & Reel	3000	−40°C to +125°C

11 Revision History

REVISION NUMBER	DESCRIPTION	DATE
1.0	Initial release and device details	2024

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