GD25LR256F

DATASHEET

Contents

1 FEATURES

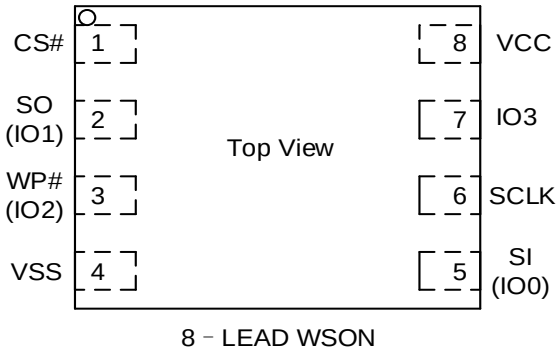
- 256M-bit Serial NOR Flash Memory
  - 32M-Byte
  - 256 Bytes per programmable page
- Standard, Dual, Quad SPI, QPI
  - Standard SPI: SCLK, CS#, SI, SO, WP#, RESET#
  - Dual SPI: SCLK, CS#, IO0, IO1, WP#, RESET#
  - Quad SPI: SCLK, CS#, IO0, IO1, IO2, IO3, RESET#
  - QPI: SCLK, CS#, IO0, IO1, IO2, IO3, RESET#
  - 3 or 4-Byte Address Mode
- High Speed Clock Frequency
  - 104MHz for fast read
  - Dual I/O Data transfer up to 208Mbits/s
  - Quad I/O Data transfer up to 416Mbits/s
  - QPI Mode Data transfer up to 416Mbits/s
- Software/Hardware Write Protection
  - Write protect all/portion of memory via software
  - Enable/Disable protection with WP# Pin
  - Individual Block Protection
- RPMC Function
  - Four 32-bit Monotonic Counters
  - Volatile HMAC Key Register
  - Non-volatile Root Key Register
- Fast Program/Erase Speed
  - Page Program time: 0.25ms typical
  - Sector Erase time: 30ms typical
  - Block Erase time: 0.12/0.15s typical
  - Chip Erase time: 75s typical
- Flexible Architecture
  - Sector of 4K-Byte
  - Block of 32/64K-Byte
  - Erase/Program Suspend/Resume
- Low Power Consumption
  - 16μA typical stand-by current
  - 3μA typical power-down current
- Advanced Security Features
  - 128-bit Unique ID
  - 3x4K-Byte Security Registers With OTP Lock
- Single Power Supply Voltage
  - Full voltage range: 1.65~2.0V
- Endurance and Data Retention
  - Minimum 100,000 Program/Erase Cycles
  - 20-year data retention typical
- Package Information
  - WSON8 (6x5mm)
  - WSON8 (8x6mm)
  - TFBGA-24ball (5x5 Ball Array)
  - SOP16 300mil

2 GENERAL DESCRIPTIONS

The GD25LR256F (256M-bit) Serial NOR Flash supports the standard Serial Peripheral Interface (SPI), and the Dual/Quad SPI: Serial Clock, Chip Select, Serial Data I/O0 (SI), I/O1 (SO), I/O2, I/O3. The Dual I/O data is transferred with speed of 208Mbit/s, and the Quad I/O data is transferred with speed of 416Mbit/s.

CONNECTION DIAGRAM AND PIN DESCRIPTION

Figure 1 Connection Diagram for WSON8 package



8 – LEAD WSON

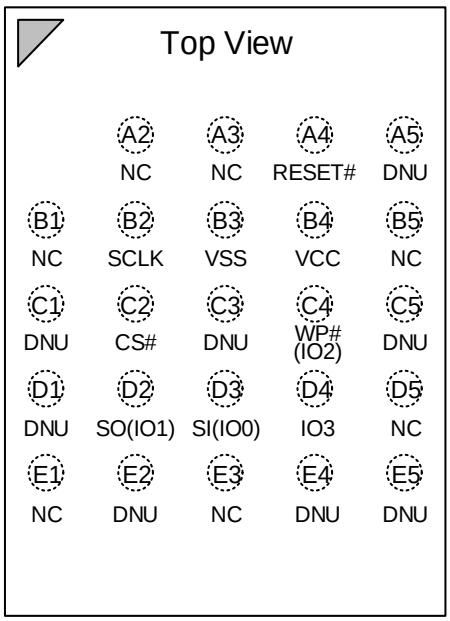
Table 1 Pin Description for WSON8 package

Pin No.	Pin Name	I/O	Description
1	CS#	I	Chip Select Input
2	SO (IO1)	I/O	Data Output (Data Input Output 1)
3	WP# (IO2)	I/O	Write Protect Input (Data Input Output 2)
4	VSS		Ground
5	SI (IO0)	I/O	Data Input (Data Input Output 0)
6	SCLK	I	Serial Clock Input
7	IO3	I/O	Data Input Output 3
8	VCC		Power Supply

Note:

1. CS# must be driven high if chip is not selected. Please don't leave CS# floating any time after power is on.

Figure 2 Connection Diagram for TFBGA24 5x5 ball array package



24-BALL TFBGA (5x5 ball array)

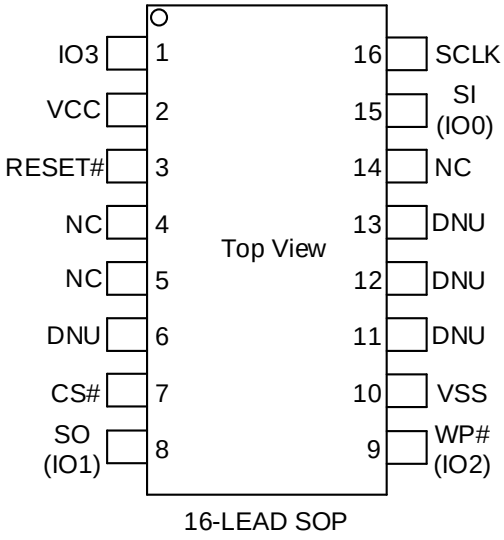
Table 2 Ball Description for TFBGA24 5x5 ball array package

Pin No.	Pin Name	I/O	Description
A4	RESET#	I	Reset Input
B2	SCLK	I	Serial Clock Input
B3	VSS		Ground
B4	VCC		Power Supply
C2	CS#	I	Chip Select Input
C4	WP# (IO2)	I/O	Write Protect Input (Data Input Output 2)
A5/C1/C3/C5/ D1/E2/E4/E5	DNU		Do Not Use (It may connect to internal signal inside)
D2	SO (IO1)	I/O	Data Output (Data Input Output 1)
D3	SI (IO0)	I/O	Data Input (Data Input Output 0)
D4	IO3	I/O	Data Input Output 3

Notes:

1. CS# must be driven high if chip is not selected. Please don't leave CS# floating any time after power is on.
2. The DNU ball must be floating. It may connect to internal signal inside.
3. The NC ball is not connected to any internal signal. It is OK to connect it to the system ground (GND) or leave it floating.
4. The RESET# pin is a dedicated hardware reset pin regardless of device settings or operation states. If the hardware reset function is not used, it is recommended to connect it to VCC in the system but leaving it floating is OK.

Figure 3 Connection Diagram for SOP16 package



16-LEAD SOP

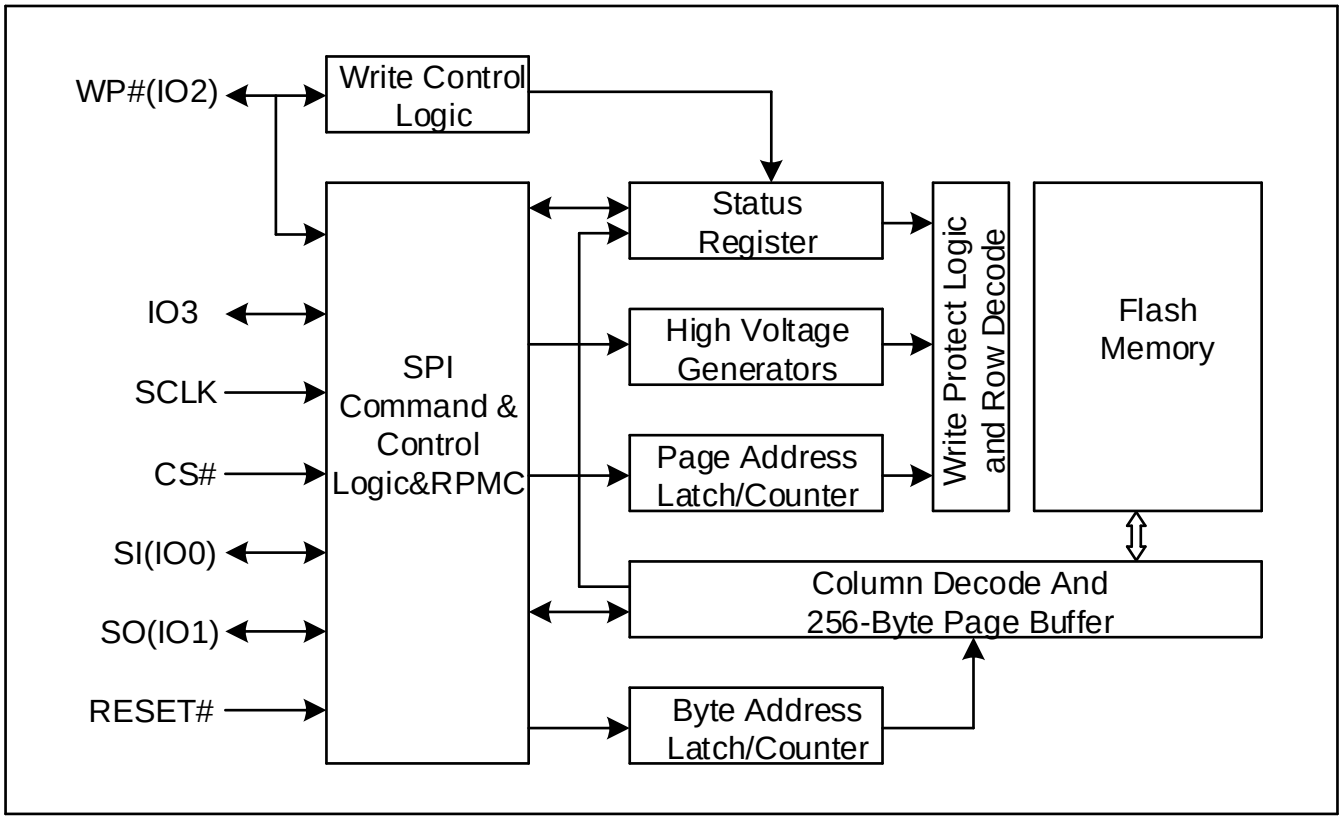
Table 3 Pin Description for SOP16 package

Pin No.	Pin Name	I/O	Description
1	IO3	I/O	Data Input Output 3
2	VCC		Power Supply
3	RESET#	I	Reset Input
7	CS#	I	Chip Select Input
8	SO (IO1)	I/O	Data Output (Data Input Output 1)
9	WP# (IO2)	I/O	Write Protect Input (Data Input Output 2)
10	VSS		Ground
6/11/12/13	DNU		Do Not Use (It may connect to internal signal inside)
15	SI (IO0)	I/O	Data Input (Data Input Output 0)
16	SCLK	I	Serial Clock Input

Notes:

1. CS# must be driven high if chip is not selected. Please don't leave CS# floating any time after power is on.
2. The DNU pin must be floating. It may connect to internal signal inside.
3. The NC pin is not connected to any internal signal. It is OK to connect it to the system ground (GND) or leave it floating.
4. The RESET# pin is a dedicated hardware reset pin regardless of device settings or operation states. If the hardware reset function is not used, it is recommended to connect it to VCC in the system but leaving it floating is OK.

BLOCK DIAGRAM



3 MEMORY ORGANIZATION

GD25LR256F

Each device has	Each block has	Each sector has	Each page has	
32M	64/32K	4K	256	Bytes
128K	256/128	16	-	pages
8K	16/8	-	-	sectors
512/1K	-	-	-	blocks

UNIFORM BLOCK SECTOR ARCHITECTURE

GD25LR256F 64K Bytes Block Sector Architecture

Block	Sector	Address range	
511	8191	1FFF000H	1FFFFFFH
	.....	.....	.....
	8176	1FF0000H	1FF0FFFH
510	8175	1FEF000H	1FEFFFFH
	.....	.....	.....
	8160	1FE0000H	1FE0FFFH
.....	.....	.....	.....
	.....	.....	.....
	.....	.....	.....
.....	.....	.....	.....
	.....	.....	.....
	.....	.....	.....
2	47	02F000H	02FFFFH
	.....	.....	.....
	32	020000H	020FFFH
1	31	01F000H	01FFFFH
	.....	.....	.....
	16	010000H	010FFFH
0	15	00F000H	00FFFFH
	.....	.....	.....
	0	000000H	000FFFH

4 DEVICE OPERATIONS

4.1 SPI Mode

Standard SPI

The GD25LR256F features a serial peripheral interface on 4 signals bus: Serial Clock (SCLK), Chip Select (CS#), Serial Data Input (SI) and Serial Data Output (SO). Both SPI bus mode 0 and 3 are supported. Input data is latched on the rising edge of SCLK and data shifts out on the falling edge of SCLK.

Dual SPI

The GD25LR256F supports Dual SPI operation when using the “Dual Output Fast Read”, “Dual Output Fast Read with 4-Byte address”, “Dual I/O Fast Read” and “Dual I/O Fast Read with 4-Byte address” commands (3Bh, 3Ch, BBh and BCh). These commands allow data to be transferred to or from the device at twice the rate of the standard SPI. When using the Dual SPI command, the SI and SO pins become bidirectional I/O pins: IO0 and IO1.

Quad SPI

The GD25LR256F supports Quad SPI operation when using the “Quad Output Fast Read”, “Quad I/O Fast Read”, “Quad Page Program” (6Bh/6Ch, EBh/ECh, 32h/34h) commands. These commands allow data to be transferred to or from the device at four times the rate of the standard SPI. When using the Quad SPI command the SI and SO pins become bidirectional I/O pins: IO0 and IO1, and the WP# pin become bidirectional I/O pins: IO2.

4.2 QPI Mode

The GD25LR256F supports Quad Peripheral Interface (QPI) operations only when the device is switched from Standard/Dual/Quad SPI mode to QPI mode using the “Enable the QPI (38h)” command. The QPI mode utilizes all four IO pins to input the command code. Standard/Dual/Quad SPI mode and QPI mode are exclusive. Only one mode can be active at any given times. “Enable the QPI (38h)” and “Disable the QPI (FFh)” commands are used to switch between these two modes. Upon power-up and Hardware Reset or after Software Reset using “Enable Reset (66h) and Reset (99h)” command, the default state of the device is Standard/Dual/Quad SPI mode.

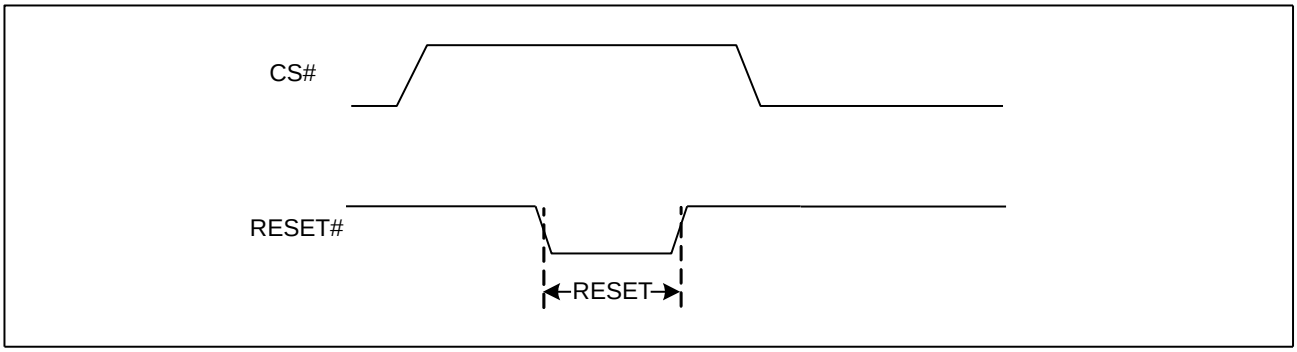
4.3 RESET Function

The RESET# pin allows the device to be reset by the control.

The RESET# pin goes low for a minimum period of tRLRH will reset the flash. After reset cycle, the flash is at the following states:

- Standby mode
- All the volatile bits will return to the default status as power on.

Figure 4 RESET Condition



Note: RESET function can only reset memory operations. RPMC operations cannot be reset by this function.

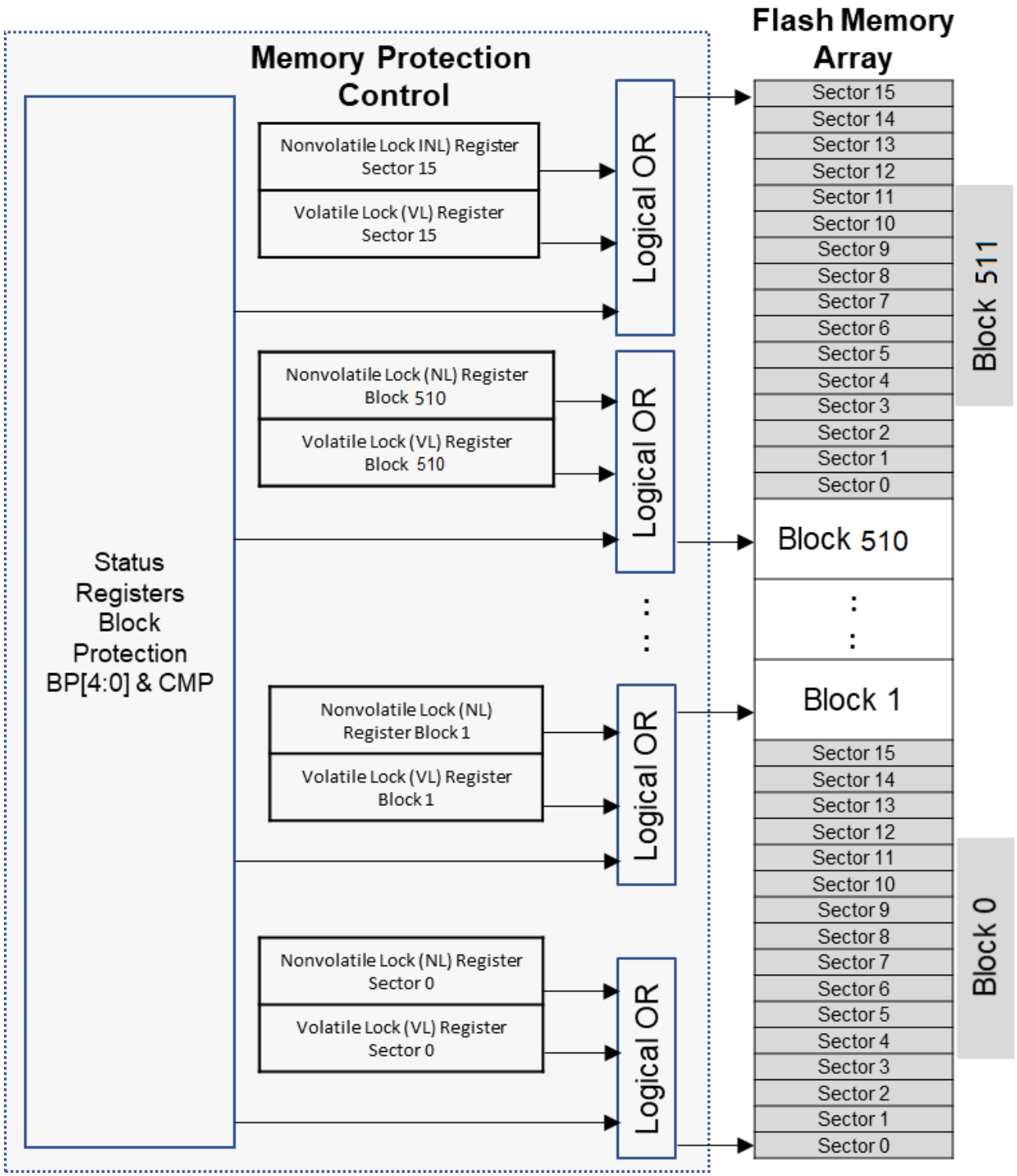
5 DATA PROTECTION

The GD25LR256F provides the following data protection methods:

- Write Enable (WREN) command: The WREN command sets the Write Enable Latch (WEL) bit to '1'. The WEL bit will reset to '0' after the following sequence or instructions:
  - Power-Up/ Software Reset (66h+99h)/Hardware Reset
  - Write Disable (WRDI)
  - Write Status Register (WRSR 1, 2 & 3)
  - Write Extended Address Register (WEAR)
  - Write Nonvolatile Configuration Register (WNVCR)
  - Write Volatile Configuration Register (WVCR)
  - Page Program (PP)
  - Sector Erase (SE) / Block Erase (BE) / Chip Erase (CE) - Erase Security Registers / Program Security Registers
  - Advanced Block Protection related instructions: Set Nonvolatile Lock (NL) Register, Clear All Nonvolatile Lock (NL) Registers
- Software Protection Mode:
  -The Block Protect (BP4, BP3, BP2, BP1, and BP0 along with the CMP) bits define the section of the memory array that can be read but cannot be changed.
  - Nonvolatile Lock (NL) Registers are additional memory non-volatile lock registers that can protect or unprotect a memory with greater granularity at the individual sectors/block level.
  - Volatile Lock (VL) Registers like NL Registers serve similar lock bit functionality at individual sector/block level except they are volatile bits.
- Hardware Protection Mode when SRP0 is '1': WP# goes low to protect the Status Register bits (i.e., BP0~BP4, CMP bits) and Nonvolatile Lock (NL) Registers against writes.
- Deep Power-Down Mode: In Deep Power-Down Mode, all commands are ignored except the Release from Deep Power-Down Mode command and reset command (66h+99h).

The GD25LR256F device supports several memory protection methods: Block Protection via Block Protect/CMP bits, Individual Volatile Block Lock Protection via VL Register bits, Individual Nonvolatile Block Lock Protection via NL Register Bits. All these protection schemes function in a logical OR method to protect or unprotect targeted sector/block as shown on Figure 5.

Figure 5 Memory Protection Control Overview



Notes:

1. The first and last blocks will have NL/VL Registers protections at the 4KB sector level. Each 4KB sector in these blocks can be individually locked by NL/VL Registers setting.
2. Each of the middle 64KB blocks has NL/VL Registers protections at the 64KB block level. Each 64KB block can be individually locked by NL/VL Registers setting.

Status Register Block Protection (BP4, BP3, BP2, BP1, BP0, CMP)

Table 4. GD25LR256F Protected area size (CMP=0)

Status Register Content					Memory Content			
BP4	BP3	BP2	BP1	BP0	Blocks	Addresses	Density	Portion
X	0	0	0	0	NONE	NONE	NONE	NONE
0	0	0	0	1	511	01FF0000h-01FFFFFFh	64KB	Upper 1/512
0	0	0	1	0	510 to 511	01FE0000h-01FFFFFFh	128KB	Upper 1/256
0	0	0	1	1	508 to 511	01FC0000h-01FFFFFFh	256KB	Upper 1/128
0	0	1	0	0	504 to 511	01F80000h-01FFFFFFh	512KB	Upper 1/64
0	0	1	0	1	496 to 511	01F00000h-01FFFFFFh	1MB	Upper 1/32
0	0	1	1	0	480 to 511	01E00000h-01FFFFFFh	2MB	Upper 1/16
0	0	1	1	1	448 to 511	01C00000h-01FFFFFFh	4MB	Upper 1/8
0	1	0	0	0	384 to 511	01800000h-01FFFFFFh	8MB	Upper 1/4
0	1	0	0	1	256 to 511	01000000h-01FFFFFFh	16MB	Upper 1/2
1	0	0	0	1	0	00000000h-0000FFFFh	64KB	Lower 1/512
1	0	0	1	0	0 to 1	00000000h-0001FFFFh	128KB	Lower 1/256
1	0	0	1	1	0 to 3	00000000h-0003FFFFh	256KB	Lower 1/128
1	0	1	0	0	0 to 7	00000000h-0007FFFFh	512KB	Lower 1/64
1	0	1	0	1	0 to 15	00000000h-000FFFFFh	1MB	Lower 1/32
1	0	1	1	0	0 to 31	00000000h-001FFFFFh	2MB	Lower 1/16
1	0	1	1	1	0 to 63	00000000h-003FFFFFh	4MB	Lower 1/8
1	1	0	0	0	0 to 127	00000000h-007FFFFFh	8MB	Lower 1/4
1	1	0	0	1	0 to 255	00000000h-00FFFFFFh	16MB	Lower 1/2
X	1	1	0	X	ALL	00000000h-01FFFFFFh	32MB	ALL
X	1	X	1	X	ALL	00000000h-01FFFFFFh	32MB	ALL

Table 5. GD25LR256F Protected area size (CMP=1)

Status Register Content					Memory Content			
BP4	BP3	BP2	BP1	BP0	Blocks	Addresses	Density	Portion
X	0	0	0	0	ALL	00000000h-01FFFFFFh	ALL	ALL
0	0	0	0	1	0 to 510	00000000h – 01FEFFFFh	32,704KB	Lower 511/512
0	0	0	1	0	0 to 509	00000000h – 01FDFFFFh	32,640KB	Lower 255/256
0	0	0	1	1	0 to 507	00000000h – 01FBFFFFh	32,512KB	Lower 127/128
0	0	1	0	0	0 to 503	00000000h – 01F7FFFFh	32,256KB	Lower 63/64
0	0	1	0	1	0 to 495	00000000h – 01EFFFFFh	31MB	Lower 31/32
0	0	1	1	0	0 to 479	00000000h – 01DFFFFFh	30MB	Lower 15/16
0	0	1	1	1	0 t0 447	00000000h – 01BFFFFFh	28MB	Lower 7/8
0	1	0	0	0	0 to 383	00000000h – 017FFFFFh	24MB	Lower 3/4
0	1	0	0	1	0 to 255	00000000h – 00FFFFFFh	16MB	Lower 1/2
1	0	0	0	1	1 to 511	00010000h – 01FFFFFFh	32,704KB	Upper 511/512
1	0	0	1	0	2 to 511	00020000h – 01FFFFFFh	32,640KB	Upper 255/256

1	0	0	1	1	4 to 511	00040000h – 01FFFFFFh	32,512KB	Upper 127/128
1	0	1	0	0	8 to 511	00080000h – 01FFFFFFh	32,256KB	Upper 63/64
1	0	1	0	1	16 to 511	00100000h – 01FFFFFFh	31MB	Upper 31/32
1	0	1	1	0	32 to 511	00200000h – 01FFFFFFh	30MB	Upper 15/16
1	0	1	1	1	64 to 511	00400000h – 01FFFFFFh	28MB	Upper 7/8
1	1	0	0	0	128 to 511	00800000h – 01FFFFFFh	24MB	Upper 3/4
1	1	0	0	1	256 to 511	01000000h – 01FFFFFFh	16MB	Upper 1/2
X	1	1	0	X	NONE	NONE	NONE	NONE
X	1	X	1	X	NONE	NONE	NONE	NONE

Volatile Lock (VL) Registers

The GD25LR256F has a total of 542 Volatile Lock Registers. Each VL Register has an 8-bit (byte) VL Register bits. The VL Register is read independently by Read VL Register (E0h) using either a sector or block address. Each VL Register is written independently by Write VL Register (E1h) instruction using either a sector or block address. All VL Registers are cleared collectively by Global VL Registers Unlock (98h) instruction and set collectively by Global VL Registers Lock (7Eh) instruction.

The bottom and top 64KB Blocks have individual volatile protection lock registers on each 4KB sectors (total 32). The middle 64KB Blocks have their own individual volatile block lock registers (total 510). The VL register mapping assignments to the memory sectors/blocks are illustrated on Figure 6. The default value of the VL Registers from power up or reset is based on the VL Default value (NVCR Address <02> Bit 2). VL Register value of '00h' indicates the corresponding sectors or blocks are unprotected. A VL Register value of 'FFh' indicates the corresponding sectors or blocks are protected.

No.	Name	Description	Note
542 VL Registers[Sector/Block Address] = 00h or FFh(1)	VL Registers	Each VL Register protects or unprotect a corresponding sector or block: 00h = Unprotected Sector/Block FFh = Protected Sector/Block Others = Not Supported(2)	Volatile Writable

Notes:

1. VL Registers mapping across the full memory is illustrated on Figure 6. NL and VL Registers Assignment on the Memory. Default value of the VL Registers from power up or reset is based on VL Default value set on NVCR Address <02> Bit 2.
2. Only valid data (00h or FFh) are valid and accepted during Write VL Register. Other data combinations are not valid data input; the Write VL Register command will be ignored; and the WEL bit will not be cleared.

Nonvolatile Lock (NL) Registers

The GD25LR256F has a total of 542 Nonvolatile Lock Registers that are non-volatile. Each NL Register has an 8-bit (byte) NL Register bits. The NL Register is read independently using either a sector or block address using Read NL Register (E2h) instruction. Each NL Register is also set independently by Set NL Register (E3h) instruction using either a sector or block address. All NL Registers are cleared collectively by Clear All NL Registers (E4h) instruction.

The bottom and top 64KB Blocks have individual non-volatile protection lock registers on each 4KB sectors (total 32). The middle 64KB Blocks have their own individual non-volatile block lock registers (total 510). The NL Register mapping

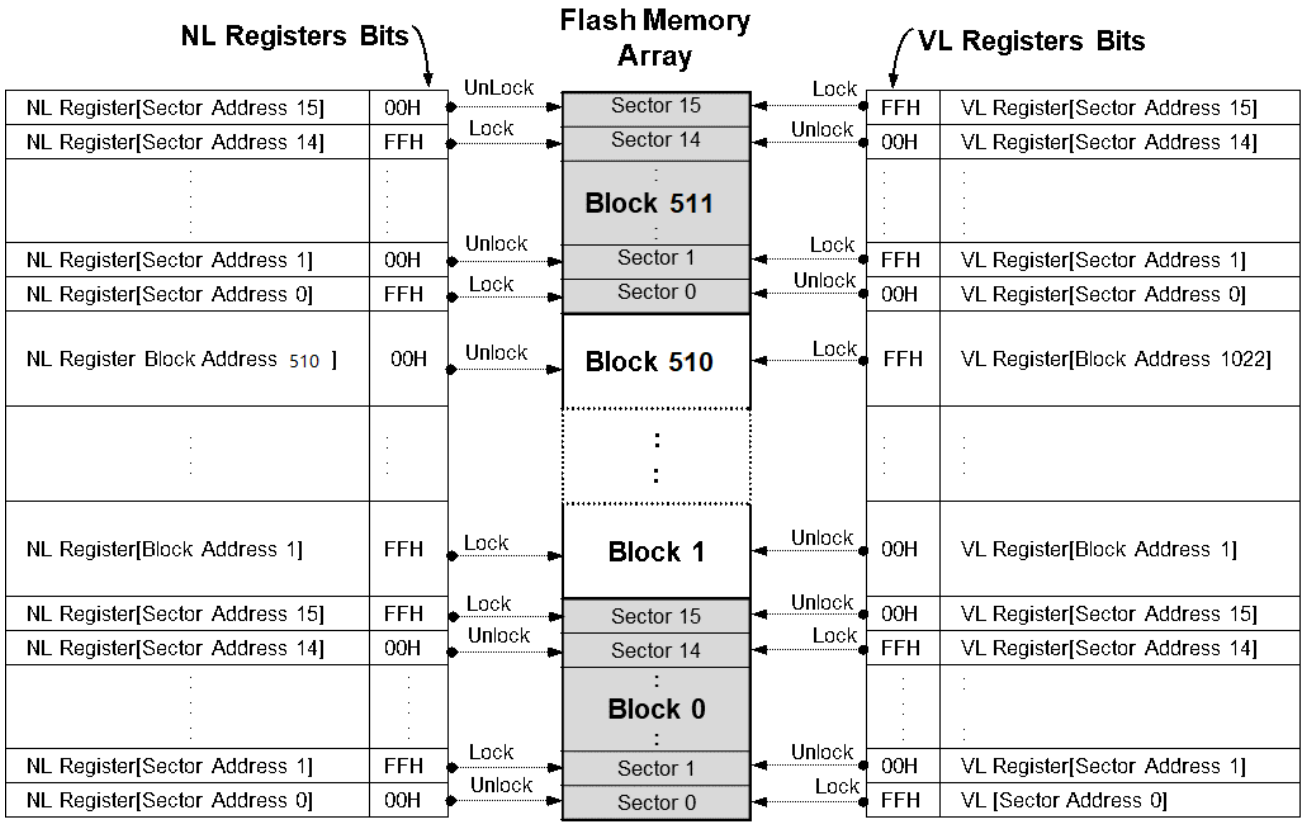
assignments to the memory sectors/blocks are illustrated on Figure 6. The factory default value of the NL Registers is '00h' indicating the corresponding sectors or blocks are unprotected. When NL Register is set to 'FFh', the corresponding sector or block is protected against program or erase.

No.	Name	Description	Note
542 NL Registers[Sector/Block Address] = 00h or FFh(1)	NL Registers	Each NL Register protects or unprotect a corresponding sector or block: 00h = Unprotected Sector/Block FFh = Protected Sector/Block Others = Not Supported	Non-Volatile Writable

Note:

1. NL Registers mapping across the full memory is illustrated on Figure 6 (NL and VL Registers Assignment on the Memory).

Figure 6. NL Registers and VL Registers Assignment on the Memory



Notes:

1. The first and last blocks will have NL/VL Registers protections at the 4KB sector level. Each 4KB sector in these blocks can be individually locked by NL/VL Registers setting.
2. Each of the middle 64KB blocks has NL/VL Registers protections at the 64KB block level. Each 64KB block can be individually locked by NL/VL Registers setting.

6 REGISTERS

6.1 Status Register

Table 6. Status Register-SR No.1

No.	Bit Name	Description	Note
S7	SRP0	Status Register Protection Bit	Non-volatile writable
S6	BP4	Block Protect Bit	Non-volatile writable
S5	BP3	Block Protect Bit	Non-volatile writable
S4	BP2	Block Protect Bit	Non-volatile writable
S3	BP1	Block Protect Bit	Non-volatile writable
S2	BP0	Block Protect Bit	Non-volatile writable
S1	WEL	Write Enable Latch	Volatile, read only
S0	WIP	Erase/Write In Progress	Volatile, read only

Table 7. Status Register-SR No.2

No.	Bit Name	Description	Note
S15	SUS1	Erase Suspend Bit	Volatile, read only
S14	CMP	Complement Protect	Non-volatile writable
S13	LB3	Security Register Lock Bit	Non-volatile writable (OTP)
S12	LB2	Security Register Lock Bit	Non-volatile writable (OTP)
S11	LB1	Security Register Lock Bit	Non-volatile writable (OTP)
S10	SUS2	Program Suspend Bit	Volatile, read only
S9	QE	Quad Enable Bit	QE = 1 permanently
S8	SRP1	Status Register Protection Bit	Non-volatile writable

Table 8. Status Register-SR No.3

No.	Bit Name	Description	Note
S23	Reserved	Reserved	Reserved
S22	Reserved	Reserved	Reserved
S21	Reserved	Reserved	Reserved
S20	ADP	Power Up Address Mode Bit	Non-volatile writable
S19	ADS	Current Address Mode Bit	Volatile, read only
S18	Reserved	Reserved	Reserved
S17	DC1	Dummy Configuration Bit	Non-volatile writable
S16	DC0	Dummy Configuration Bit	Non-volatile writable

The status and control bits of the Status Register are as follows:

WIP bit

The Write in Progress (WIP) bit indicates whether the memory is busy in program/erase/write status register or configuration register progress. When WIP bit sets to 1, means the device is busy in program/erase/write status register or configuration register progress, when WIP bit sets 0, means the device is not in program/erase/write status register or configuration register progress.

WEL bit

The Write Enable Latch (WEL) bit indicates the status of the internal Write Enable Latch. When set to 1 the internal Write Enable Latch is set, when set to 0 the internal Write Enable Latch is reset and no Write, Program or Erase command is accepted.

BP4, BP3, BP2, BP1, BP0 bits

The Block Protect (BP4, BP3, BP2, BP1, and BP0) bits are non-volatile. They define the size of the area to be software protected against Program and Erase commands. These bits are written with the Write Status Register (WRSR) command. When the Block Protect (BP4, BP3, BP2, BP1, and BP0) bits are set to 1, the relevant memory area becomes protected against Page Program (PP), Sector Erase (SE) and Block Erase (BE) commands. The Block Protect (BP4, BP3, BP2, BP1, and BP0) bits can be written provided that the Hardware Protected mode has not been set. The Chip Erase (CE) command is executed only if none sector or block is protected.

SRP0, SRP1 bits

The Status Register Protect (SRP1 and SRP0) bits are non-volatile Read/Write bits in the status register. The SRP bits control the method of write protection: software protection, hardware protection, power supply lock-down or one-time programmable protection.

SRP1	SRP0	#WP	Status Register/NL Register	Description
0	0	X	Software Protected	The Status Register and NL Registers can be written to after a Write Enable command, WEL=1. (Default)
0	1	0	Hardware Protected	WP#=0, the Status Register and NL Registers are locked and cannot be written to.
0	1	1	Hardware Unprotected	WP#=1, the Status Register and NL Registers are unlocked and can be written to after a Write Enable command, WEL=1.
1	X	X	Power Supply Lock-Down(1)	Status Register and NL Registers are protected and cannot be written to again until the next Power-Down, Power-Up cycle ,Software Reset(66h+99h),Hardware Reset.
1	X	X	One Time Program(2)	Status Register and NL Registers are permanently protected and cannot be written to. **(Enabled by adding prefix command AAh, 55h)**

Notes:

1. When SRP1 =1, a power-down, power-up cycle, Software reset (66H+99H), Hardware Reset will change SRP1 =0 state.
2. Please contact GigaDevice for details regarding the special instruction sequence.

ADS bit

The Address Status (ADS) bit is a read only bit that indicates the current address mode the device is operating in. The device is in 3-Byte address mode when ADS=0 (default), and in 4-Byte address mode when ADS=1.

QE bit

The Quad Enable (QE) bit is a non-volatile bit in the Status Register that allows Quad operation. The default value of QE bit is 1 and it cannot be changed, so that the IO2 and IO3 pins are enabled all the time.

SUS1, SUS2 bits

The SUS1 and SUS2 bits are read only bits in the status register (S15 and S10) that are set to 1 after executing an Program/Erase Suspend (75h) command (The Erase Suspend will set the SUS1 bit to 1, and the Program Suspend will set the SUS2 bit to 1). The SUS1 and SUS2 bits are cleared to 0 by Erase/Program Resume (7Ah) command, software reset (66h+99h) command as well as a power-down, power-up cycle.

LB3, LB2, LB1 bits

The LB3, LB2 and LB1 bits are non-volatile One Time Program (OTP) bits in Status Register (S13, S12 and S11) that provide the write protect control and status to the Security Registers. The default state of LB3, LB2 and LB1 bits are 0, the security registers are unlocked. The LB3, LB2 and LB1 bits can be set to 1 individually using the Write Register instruction. The LB3, LB2 and LB1 bits are One Time Programmable, once they are set to 1, the Security Registers will become read-only permanently.

DC1, DC0 bits

The Dummy Configuration (DC) bits are non-volatile, which select the number of dummy cycles between the end of address and the start of read data output. Dummy cycles provide additional latency that is needed to complete the initial read access of the flash array before data can be returned to the host system. Some read commands require additional dummy cycles as the SCLK frequency increases.

The following dummy cycle tables provide different dummy cycle settings that are configured.

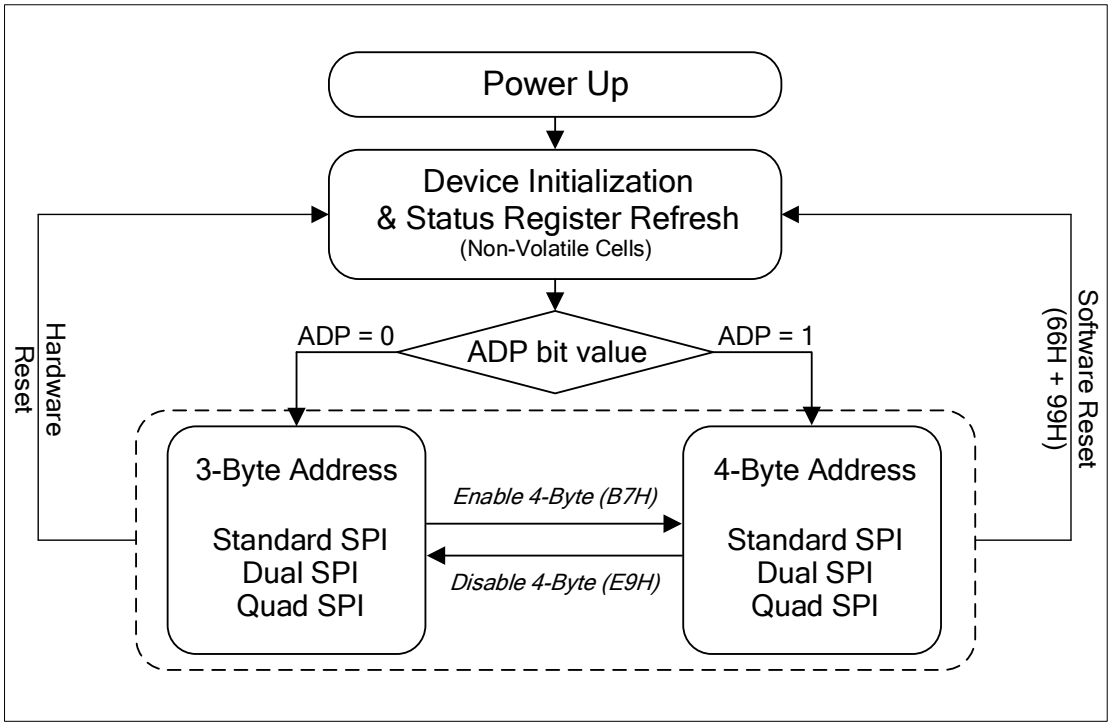
Command	DC1, DC0	Dummy Cycles	Freq.(MHz)
0Bh, 0Ch 3Bh, 3Ch 6Bh, 6Ch	00(default)	8	104
	01	8	104
	10	8	104
	11	8	104
BBh, BCh	00(default)	4	80
	01	8	104
	10	4	80
	11	8	104
EBh, ECh	00(default)	6	80
	01	6	80
	10	8	104
	11	10	104

CMP bit

The CMP bit is a non-volatile Read/Write bit in the Status Register (S14). It is used in conjunction with the BP4-BP0 bits to provide more flexibility for the array protection. Please see the Status registers. Memory Protection table for details. The default setting is CMP=0.

ADP bit

The Address Power-up (ADP) bit is a non-volatile writable bit that determines the initial address mode when the device is powered on or reset. This bit is only used during the power on or device reset initialization period. When ADP=0 (factory default), the device will power up into 3-Byte address mode, the Extended Address Register must be used to access memory regions beyond 128Mb. When ADP=1, the device will power up into 4-Byte address mode directly.



Reserved bit

It is recommended to set the value of the reserved bit as “0”.

6.2 Extended Address Register

Table 9 Extended Address Register

No.	Name	Description	Note
EA7	Reserved	Reserved	Reserved
EA6	Reserved	Reserved	Reserved
EA5	Reserved	Reserved	Reserved
EA4	Reserved	Reserved	Reserved
EA3	Reserved	Reserved	Reserved
EA2	Reserved	Reserved	Reserved
EA1	Reserved	Reserved	Reserved
EA0	A24	Address bit	Volatile writable

The extended address register is only used when the address mode is 3-Byte mode, as to set the higher address. The default value of the address bit is “0”.

For the read operation, the whole array can be continually read out with one command. Data output starts from the selected 128Mb, and it can cross the boundary. When the last Byte of the segment is reached, the next Byte (in a continuous reading) is the first Byte of the next segment. However, the EAR (Extended Address Register) value does not change. The random access reading can only be operated in the selected segment.

The Chip erase command will erase the whole chip and is not limited by EAR selected segment. However, the sector erase, block erase, program operation are limited in selected segment and will not cross the boundary.

A24 bits

The Extended Address Bits are used only when the device is operating in the 3-Byte Address Mode (ADS=0), which is volatile writable by C5h command.

If the device powers up with ADP bit set to 1, or an “Enter 4-Byte Address Mode (B7h)” instruction is issued, the device will require 4-Byte address input for all address related instructions, and the Extended Address Bit setting will be ignored.

A24	Address Range
0	0000 0000h-00FF FFFFh
1	0100 0000h-01FF FFFFh

Reserved bit

It is recommended to set the value of the reserved bit as “0”.

6.3 Flag Status Register

Table 10 Flag Status Register

No.	Name	Description	Note
FS7	RY/BY#	Ready/Busy# Bit	Volatile, read only
FS6	Reserved	Reserved	Reserved
FS5	Reserved	Reserved	Reserved
FS4	Reserved	Reserved	Reserved
FS3	Reserved	Reserved	Reserved
FS2	Reserved	Reserved	Reserved
FS1	PE	Program Error Bit	Volatile, read only
FS0	EE	Erase Error bit	Volatile, read only

The status and control bits of the Flag Status Register are as follows:

RY/BY# bit

The RY/BY# bit is a read only bit that indicates Program or Erase Status bit. Indicates whether one of the following command cycles is in progress: WRITE STATUS REGISTER, WRITE NONVOLATILE CONFIGURATION REGISTER, PROGRAM, or ERASE.

PE bit

The Program Error (PE) bit is a read only bit that indicates a program failure. It will also be set when the user attempts to program a protected array sector or access the locked OTP space. PE is cleared to "0" after program operation resumes or by Clear Flag Status Register command (30h).

EE bit

The Erase Error (EE) bit is a read only bit that indicates an erase failure. It will also be set when the user attempts to erase a protected array sector or access the locked OTP space. EE is cleared to "0" after erase operation resumes or by Clear Flag Status Register command (30h).

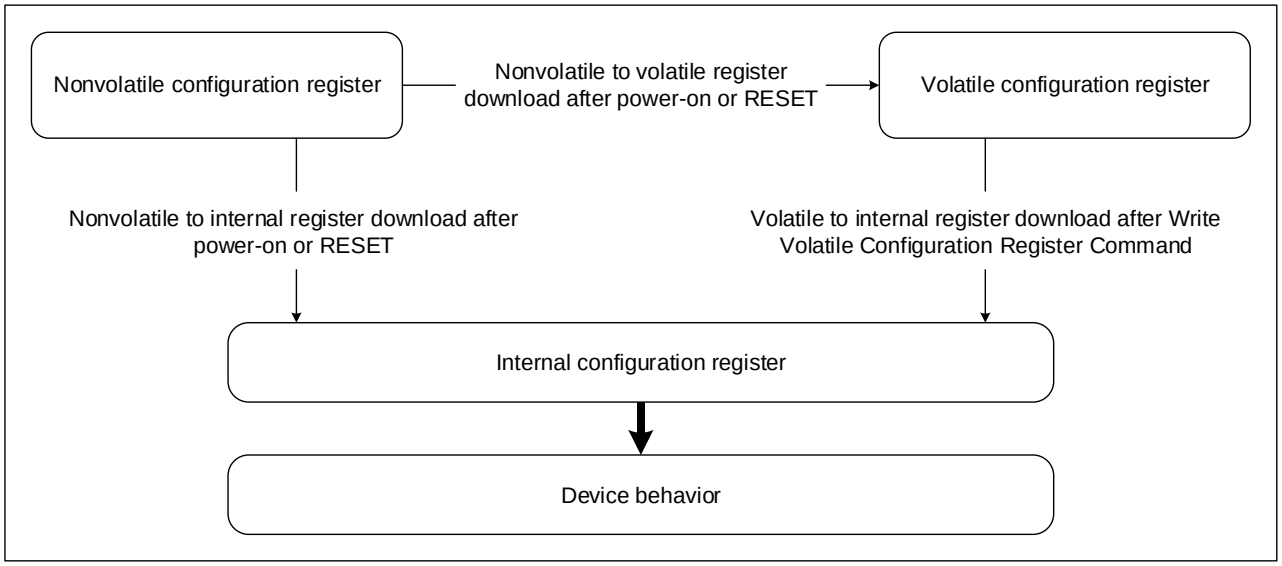
Reserved bit

It is recommended to set the value of the reserved bit as “0”.

7 INTERNAL CONFIGURATION REGISTER

The memory configuration is set by an internal configuration register that is not directly accessible to users. The user can change the default configuration at power up by using the WRITE NONVOLATILE CONFIGURATION REGISTER. Information from the nonvolatile configuration register overwrites the internal configuration register during power on or after a reset.

The user can change the configuration during device operation using the WRITE VOLATILE CONFIGURATION REGISTER command. Information from the volatile configuration registers overwrite the internal configuration register immediately after the WRITE command completes.



7.1 Nonvolatile Configuration Register

Nonvolatile Configuration Register bits set the device configuration after power-up or reset. All bits are erased (FFh) unless stated otherwise. This register is read from and written to using the READ NONVOLATILE CONFIGURATION REGISTER and the WRITE NONVOLATILE CONFIGURATION REGISTER commands, respectively. The commands use the main array address scheme, but only the LSB is used to access different register settings, thereby providing up to 256 Bytes of registers (See the table below for the details). A WRITE command to a reserved address will set the device to the default status of the corresponding Byte.

Table 11 Nonvolatile Configuration Register

Addr	Settings	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Description
<0>	Reserved									
<1>	Driver Strength configuration	x	x	x	x	x	x	0	0	18 Ohm
		x	x	x	x	x	x	0	1	25 Ohm (Default)
		x	x	x	x	x	x	1	0	35 Ohm
		x	x	x	x	x	x	1	1	50 Ohm
		Others								Reserved
<2>	VL default value	x	x	x	x	x	1	x	x	all VL=1 after POR or Reset
		x	x	x	x	x	0	x	x	all VL=0 after POR or Reset(Default)
		Others								Reserved
<3>	Reserved									
<4>	Reserved									
<5>	Reserved									
<6>	Reserved									
<7>	Reserved									
<8>	Reserved									
<9>	Reserved									
<A>	Reserved									
<B>	Reserved									

7.2 Volatile Configuration Register

Volatile Configuration Register bits temporarily set the device configuration after power-up or reset. All bits are erased (FFh) unless stated otherwise. This register is read from and written to using the READ VOLATILE CONFIGURATION REGISTER and the WRITE VOLATILE CONFIGURATION REGISTER commands, respectively. The commands use the main array address scheme; however, only the LSB is used to access different register settings to provide up to 256 Bytes of registers (See the table below for the details). A WRITE command to a reserved address will set the device to the default status of the corresponding Byte.

Table 12 Volatile Configuration Register

Addr	Settings	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Description
<0>	Reserved									
<1>	Driver Strength configuration	x	x	x	x	x	x	0	0	18 Ohm
		x	x	x	x	x	x	0	1	25 Ohm (Default)
		x	x	x	x	x	x	1	0	35 Ohm
		x	x	x	x	x	x	1	1	50 Ohm
		Others								Reserved
<2>	Reserved									
<3>	Reserved									
<4>	Reserved									
<5>	Reserved									
<6>	Reserved									
<7>	Reserved									
<8>	Reserved									
<9>	Reserved									
<A>	Reserved									
<B>	Reserved									

8 COMMAND DESCRIPTIONS

All commands, addresses and data are shifted in and out of the device, beginning with the most significant bit on the first rising edge of SCLK after CS# is driven low. Then, the one-Byte command code must be shifted in to the device, with most significant bit first on SI, and each bit is latched on the rising edges of SCLK.

Every command sequence starts with a one-Byte command code. Depending on the command, this might be followed by address Bytes, or by data Bytes, or by both or none. CS# must be driven high after the last bit of the command sequence has been completed. For the command of Read, Fast Read, Read Status Register or Release from Deep Power-Down, and Read Device ID, the shifted-in command sequence is followed by a data-out sequence. All read instruction can be completed after any bit of the data-out sequence is being shifted out, and then CS# must be driven high to return to deselected status.

For the command of Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register, Write Enable, Write Disable or Deep Power-Down command, CS# must be driven high exactly at a Byte boundary, otherwise the command is rejected, and is not executed. That is CS# must be driven high when the number of clock pulses after CS# being driven low is an exact multiple of eight. For Page Program, if at any time the input Byte is not a full Byte, nothing will happen and WEL will not be reset.

Table 13. Commands (SPI, 3- or 4-Byte Addr. Mode)

Command Name	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	Byte 8	Byte 9
Write Enable	06h								
Write Disable	04h								
Read Status Register-1	05h	(S7-S0)	(cont.)						
Read Status Register-2	35h	(S15-S8)	(cont.)						
Read Status Register-3	15h	(S23-S16)	(cont.)						
Read Flag Status Register	70h	FS7~FS0	(cont.)						
Write Status Register-1&2	01h	S7-S0	S15-S8						
Write Status Register-3	11h	S23-S16							
Read Extended Addr. Register	C8h	(EA7-EA0)							
Write Extended Addr. Register	C5h	EA7-EA0							
Volatile SR write Enable	50h								
Clear SR Flags	30h								
Set Burst with Wrap	77h	dummy(1)	dummy(1)	dummy(1)	W7-W0(1)				

Chip Erase	60h/C7h								
Enter 4-Byte Address Mode	B7h								
Exit 4-Byte Address Mode	E9h								
Read Manufacturer/ Device ID	90h	00H	00H	00H	(MID7-MID0)	(DID7-DID0)	(cont.)		
Read Identification	9Fh	(M7-M0)	(JDID15-JDID8)	(JDID7-JDID0)	(cont.)				
Enable Reset	66h								
Reset	99h								
Program/Erase Suspend	75h								
Program/Erase Resume	7Ah								
Deep Power-Down	B9h								
Release From Deep Power-Down	ABh								
Release From Deep Power-Down and Read Device ID	ABh	dummy	dummy	dummy	(DID7-DID0)	(cont.)			
Enable QPI	38h								
Read Serial Flash Discoverable Parameter	5Ah	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	(cont.)		
Read Data with 4-Byte Address	13h	A31-A24	A23-A16	A15-A8	A7-A0	(D7-D0)	(cont.)		
Fast Read with 4-Byte Address	0Ch	A31-A24	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	(cont.)	
Fast Read Dual Output with 4-Byte Address	3Ch	A31-A24	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)(2)	(cont.)	
Fast Read Quad Output with 4-Byte Address	6Ch	A31-A24	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)(3)	(cont.)	
Fast Read Dual I/O with 4-Byte Address	BCh	A31-A24(4)	A23-A16(4)	A15-A8(4)	A7-A0(4)	M7-M0(5)	(D7-D0)(2)	(cont.)	
Fast Read Quad I/O with 4-Byte Address	ECh	A31-A24(6)	A23-A16(6)	A15-A8(6)	A7-A0(6)	M7-M0(7)	dummy	dummy	(D7-D0)(3)
Page Program with 4-Byte Address	12h	A31-A24	A23-A16	A15-A8	A7-A0	D7-D0	Next Byte		

Quad Page Program with 4-Byte Address	34h	A31-A24	A23-A16	A15-A8	A7-A0	D7-D0	Next Byte		
Sector Erase with 4-Byte Address	21h	A31-A24	A23-A16	A15-A8	A7-A0				
Block Erase (32K) with 4-Byte Address	5Ch	A31-A24	A23-A16	A15-A8	A7-A0				
Block Erase (64K) with 4-Byte Address	DCh	A31-A24	A23-A16	A15-A8	A7-A0				
Read VL Register	E0h	A31-A24	A23-A16	A15-A8	A7-A0	(D7-D0)	(cont.)		
Write VL Register	E1h	A31-A24	A23-A16	A15-A8	A7-A0	D7-D0			
Read NL Register	E2h	A31-A24	A23-A16	A15-A8	A7-A0	(D7-D0)	(cont.)		
NL bit Program	E3h	A31-A24	A23-A16	A15-A8	A7-A0				
All NL bit Erase	E4h								
Global Block Lock	7Eh								
Global Block Unlock	98h								

Table 14. Commands (SPI, 3-Byte Addr. Mode)

Command Name	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	Byte 8	Byte 9
Read Data	03h	A23-A16	A15-A8	A7-A0	(D7-D0)	(cont.)			
Fast Read	0Bh	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	(cont.)		
Dual Output Fast Read	3Bh	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)(2)	(cont.)		
Quad Output Fast Read	6Bh	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)(3)	(cont.)		
Dual I/O Fast Read	BBh	A23-A16(9)	A15-A8(9)	A7-A0(9)	M7-M0(5)	(D7-D0)(2)	(cont.)		
Quad I/O Fast Read	EBh	A23-A16(10)	A15-A8(10)	A7-A0(10)	M7-M0(7)	dummy	dummy	(D7-D0)(3)	(cont.)
Page Program	02h	A23-A16	A15-A8	A7-A0	D7-D0	Next Byte			
Quad Page Program	32h	A23-A16	A15-A8	A7-A0	D7-D0	Next Byte			
Sector Erase	20h	A23-A16	A15-A8	A7-A0					
Block Erase (32K)	52h	A23-A16	A15-A8	A7-A0					
Block Erase (64K)	D8h	A23-A16	A15-A8	A7-A0					
Read Unique ID	4Bh	00H	00H	00H	dummy	(UID7-UID0)	(cont.)		
Erase Security Registers(11)	44h	A23-A16	A15-A8	A7-A0					

Program Security Registers(11)	42h	A23-A16	A15-A8	A7-A0	D7-D0	Next Byte			
Read Security Registers(11)	48h	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	(cont.)		
Write Nonvolatile Configuration Register	B1h	A23-A16	A15-A8	A7-A0	(D7-D0)				
Write Volatile Configuration Register	81h	A23-A16	A15-A8	A7-A0	(D7-D0)				
Read Nonvolatile Configuration Register	B5h	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)			
Read Volatile Configuration Register	85h	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)			

Table 15. Commands (SPI, 4-Byte Addr. Mode)

Command Name	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	Byte 8	Byte 9
Read Data	03h	A31-A24	A23-A16	A15-A8	A7-A0	(D7-D0)	(cont.)		
Fast Read	0Bh	A31-A24	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	(cont.)	
Dual Output Fast Read	3Bh	A31-A24	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)(2)	(cont.)	
Quad Output Fast Read	6Bh	A31-A24	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)(3)	(cont.)	
Dual I/O Fast Read	BBh	A31-A24(4)	A23-A16(4)	A15-A8(4)	A7-A0(4)	M7-M0(5)	(D7-D0)(2)	(cont.)	
Quad I/O Fast Read	EBh	A31-A24(6)	A23-A16(6)	A15-A8(6)	A7-A0(6)	M7-M0(7)	dummy	dummy	(D7-D0) (3)
Page Program	02h	A31-A24	A23-A16	A15-A8	A7-A0	D7-D0	Next Byte		
Quad Page Program	32h	A31-A24(6)	A23-A16(6)	A15-A8(6)	A7-A0(6)	D7-D0	Next Byte		
Sector Erase	20h	A31-A24	A23-A16	A15-A8	A7-A0				
Block Erase (32K)	52h	A31-A24	A23-A16	A15-A8	A7-A0				
Block Erase (64K)	D8h	A31-A24	A23-A16	A15-A8	A7-A0				
Read Unique ID	4Bh	00H	00H	00H	00H	dummy	(UID7-UID0)	(cont.)	
Erase Security Registers(11)	44h	A31-A24	A23-A16	A15-A8	A7-A0				
Program Security Registers(11)	42h	A31-A24	A23-A16	A15-A8	A7-A0	D7-D0	Next Byte		
Read Security Registers(11)	48h	A31-A24	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	(cont.)	
Write Nonvolatile Configuration Register	B1h	A31-A24	A23-A16	A15-A8	A7-A0	(D7-D0)			
Write Volatile Configuration Register	81h	A31-A24	A23-A16	A15-A8	A7-A0	(D7-D0)			

Read Nonvolatile Configuration Register	B5h	A31-A24	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)		
Read Volatile Configuration Register	85h	A31-A24	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)		

Table 16. Commands (QPI, 3- or 4-Byte Addr. Mode)

Command Name	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	Byte 8	Byte 9
Clock Number	(0,1)	(2,3)	(4,5)	(6,7)	(8,9)	(10,11)	(12,13)	(14,15)	(16,17)
Write Enable	06h								
Write Disable	04h								
Read Status Register-1	05h	(S7~S0)	(cont.)						
Read Status Register-2	35h	(S15-S8)	(cont.)						
Read Status Register-3	15h	(S23~S16)	(cont.)						
Read Flag Status Register	70h	FS7~FS0	(cont.)						
Write Status Register-1&2	01h	S7-S0	S15-S8						
Write Status Register-3	11h	S23-S16							
Read Extended Addr. Register	C8h	(EA7-EA0)							
Write Extended Addr. Register	C5h	EA7-EA0							
Volatile SR Write Enable	50h								
Clear SR Flags	30h								
Chip Erase	60h/C7h								
Enter 4-Byte Address Mode	B7h								
Exit 4-Byte Address Mode	E9h								
Manufacturer/Device ID	90h	dummy	dummy	00H	(M7-M0)	(ID7-ID0)	(cont.)		
Read Identification	9Fh	(M7-M0)	(JDID15-JDID8)	(JDID7-JDID0)	(cont.)				
Enable Reset	66h								
Reset	99h								
Program/Erase Suspend	75h								
Program/Erase Resume	7Ah								
Deep Power-Down	B9h								
Release From Deep Power-Down	ABh								

Release From Deep Power-Down, And Read Device ID	ABh	dummy	dummy	dummy	(ID7-ID0)	(cont.)			
Read Serial Flash Discoverable Parameter	5Ah	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	(cont.)		
Fast Read Quad Output with 4-Byte Address	ECh	A31-A24	A23-A16	A15-A8	A7-A0	M7-M0	dummy	(D7-D0)	
Page Program with 4-Byte Address	12h	A31-A24	A23-A16	A15-A8	A7-A0	D7-D0	Next Byte		
Sector Erase with 4-Byte Address	21h	A31-A24	A23-A16	A15-A8	A7-A0				
Block Erase (32K) with 4-Byte Address	5Ch	A31-A24	A23-A16	A15-A8	A7-A0				
Block Erase (64K) with 4-Byte Address	DCh	A31-A24	A23-A16	A15-A8	A7-A0				
Set Read Parameters	C0h	P7-P0							
Disable QPI	FFh								
Read VL Register	E0h	A31-A24	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	(cont.)	
Write VL Register	E1h	A31-A24	A23-A16	A15-A8	A7-A0	D7-D0			
Read NL Register	E2h	A31-A24	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	(cont.)	
NL bit Program	E3h	A31-A24	A23-A16	A15-A8	A7-A0				
All NL bit Erase	E4h								
Global Block Lock	7Eh								
Global Block Unlock	98h								

Table 17. Commands (QPI, 3-Byte Addr. Mode)

Command Name	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	Byte 8	Byte 9
Clock Number	(0,1)	(2,3)	(4,5)	(6,7)	(8,9)	(10,11)	(12,13)	(14,15)	(16,17)
Fast Read	0Bh	A23-A16	A15-A8	A7-A0	dummy	dummy	(D7-D0)		
Quad I/O Fast Read	EBh	A23-A16	A15-A8	A7-A0	M7-M0	dummy	(D7-D0)		
Page Program	02h	A23-A16	A15-A8	A7-A0	D7-D0	Next Byte			
Sector Erase	20h	A23-A16	A15-A8	A7-A0					
Block Erase (32K)	52h	A23-A16	A15-A8	A7-A0					
Block Erase (64K)	D8h	A23-A16	A15-A8	A7-A0					
Burst Read with Wrap	0Ch	A23-A16	A15-A8	A7-A0	dummy	dummy	(D7-D0)		
Write Nonvolatile Configuration Register	B1h	A23-A16	A15-A8	A7-A0	(D7-D0)				
Write Volatile Configuration Register	81h	A23-A16	A15-A8	A7-A0	(D7-D0)				
Read Nonvolatile Configuration Register	B5h	A23-A16	A15-A8	A7-A0	dummy	dummy	dummy	dummy	(D7-D0)

Read Volatile Configuration Register	85h	A23-A16	A15-A8	A7-A0	dummy	dummy	dummy	dummy	(D7-D0)

Table 18. Commands (QPI, 4-Byte Addr. Mode)

Command Name	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	Byte 8	Byte 9	Byte 10
Clock Number	(0,1)	(2,3)	(4,5)	(6,7)	(8,9)	(10,11)	(12,13)	(14,15)	(16,17)	(18,19)
Fast Read	0Bh	A31-A24	A23-A16	A15-A8	A7-A0	dummy	dummy	(D7-D0)		
Quad I/O Fast Read	EBh	A31-A24	A23-A16	A15-A8	A7-A0	M7-M0	dummy	(D7-D0)		
Page Program	02h	A31-A24	A23-A16	A15-A8	A7-A0	D7-D0	Next Byte			
Sector Erase	20h	A31-A24	A23-A16	A15-A8	A7-A0					
Block Erase (32K)	52h	A31-A24	A23-A16	A15-A8	A7-A0					
Block Erase (64K)	D8h	A31-A24	A23-A16	A15-A8	A7-A0					
Burst Read with Wrap	0Ch	A31-A24	A23-A16	A15-A8	A7-A0	dummy	dummy	(D7-D0)		
Write Nonvolatile Configuration Register	B1h	A31-A24	A23-A16	A15-A8	A7-A0	(D7-D0)				
Write Volatile Configuration Register	81h	A31-A24	A23-A16	A15-A8	A7-A0	(D7-D0)				
Read Nonvolatile Configuration Register	B5h	A31-A24	A23-A16	A15-A8	A7-A0	dummy	dummy	dummy	dummy	(D7-D0)
Read Volatile Configuration Register	85h	A31-A24	A23-A16	A15-A8	A7-A0	dummy	dummy	dummy	dummy	(D7-D0)

Notes:

1. Dummy bits and Wrap Bits

IO0 = (x, x, x, x, x, x, W4, x)

IO1 = (x, x, x, x, x, x, W5, x)

IO2 = (x, x, x, x, x, x, W6, x)

IO3 = (x, x, x, x, x, x, x, x)

2. Dual Output data

IO0 = (D6, D4, D2, D0)

IO1 = (D7, D5, D3, D1)

3. Quad Output Data

IO0 = (D4, D0, …)

IO1 = (D5, D1, …)

IO2 = (D6, D2, …)

IO3 = (D7, D3, …)

4. Dual Input 4-Byte Address

IO0 = A30, A28, A26, A24, A22, A20, A18, A16, A14, A12, A10, A8 A6, A4, A2, A0

IO1 = A31, A29, A27, A25, A23, A21, A19, A17, A15, A13, A11, A9 A7, A5, A3, A1

5. Dual Input Mode bit

IO0 = M6, M4, M2, M0

IO1 = M7, M5, M3, M1

6. Quad Input 4-Byte Address

IO0 = A28, A24, A20, A16, A12, A8, A4, A0

IO1 = A29, A25, A21, A17, A13, A9, A5, A1

IO2 = A30, A26, A22, A18, A14, A10, A6, A2

IO3 = A31, A27, A23, A19, A15, A11, A7, A3

7. Quad Input Mode bit

IO0 = M4, M0

IO1 = M5, M1

IO2 = M6, M2

IO3 = M7, M3

8. Quad Output Data

IO0 = D4, D0, …

IO1 = D5, D1, …

IO2 = D6, D2, …

IO3 = D7, D3, …

9. Dual Input Address

IO0 = A22, A20, A18, A16, A14, A12, A10, A8 A6, A4, A2, A0

IO1 = A23, A21, A19, A17, A15, A13, A11, A9 A7, A5, A3, A1

10. Quad Input Address

IO0 = A20, A16, A12, A8, A4, A0

IO1 = A21, A17, A13, A9, A5, A1

IO2 = A22, A18, A14, A10, A6, A2

IO3 = A23, A19, A15, A11, A7, A3

11. Security Registers Address

Security Register1: A23-A16=00H, A15-A12=1H, A11--A0= Byte Address;

Security Register2: A23-A16=00H, A15-A12=2H, A11- A0= Byte Address;

Security Register3: A23-A16=00H, A15-A12=3H, A11- A0= Byte Address;

12. QPI Command, Address, Data input/output format:

CLK #0 1 2 3 4 5 6 7 8 9 10 11

IO0= C4, C0, A20, A16, A12, A8, A4, A0, D4, D0, D4, D0,

IO1= C5, C1, A21, A17, A13, A9, A5, A1, D5, D1, D5, D1

IO2= C6, C2, A22, A18, A14, A10, A6, A2, D6, D2, D6, D2

IO3= C7, C3, A23, A19, A15, A11, A7, A3, D7, D3, D7, D3

Table of ID Definitions

GD25LR256F

Operation Code	MID7-MID0	ID15-ID8	ID7-ID0
9Fh	C8	60	19
90h	C8		18
ABh			18

8.1 Enable 4-Byte Mode (B7h)

The Enable 4-Byte Mode command enables accessing the address length of 32-bit for the memory area of the higher density (larger than 128Mb). After sending the Enable 4-Byte Mode command, the ADS bit (S8) will be set to 1 to indicate the 4-Byte address mode has been enabled. Once the 4-Byte address mode is enabled, the address length becomes 32-bit.

Figure 7 Enable 4-Byte Mode Sequence Diagram (SPI)

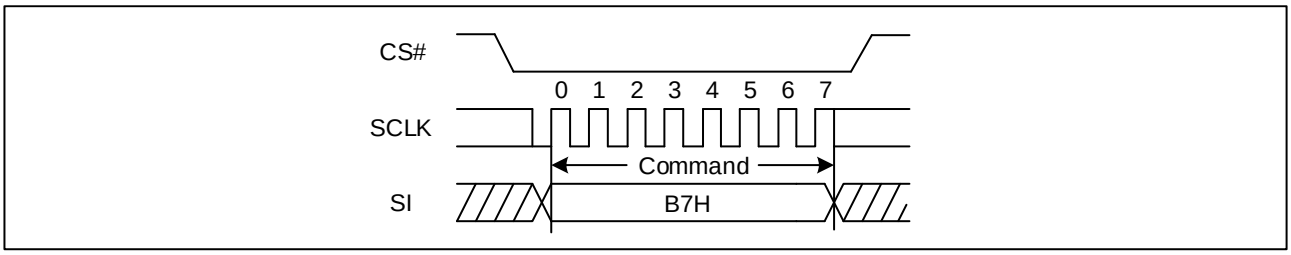
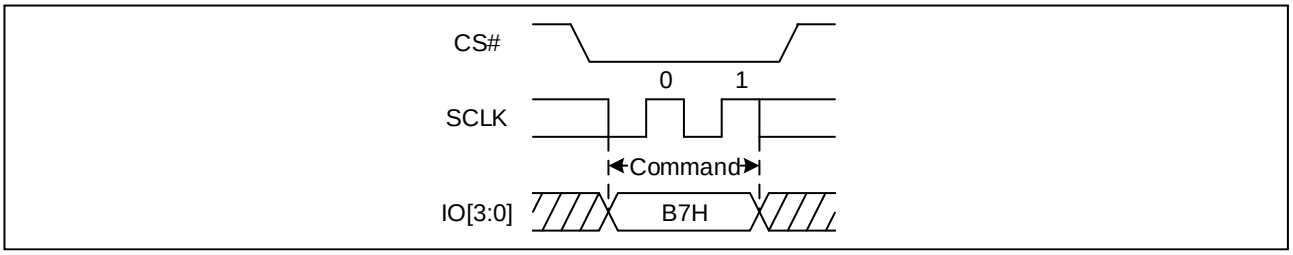


Figure 8 Enable 4-Byte Mode Sequence Diagram (QPI)



8.2 Disable 4-Byte Mode (E9h)

The Disable 4-Byte Mode command is executed to exit the 4-Byte address mode and enter the 3-Byte address mode. After sending the Disable 4-Byte Mode command, the ADS bit (S8) will be clear to be 0 to indicate the 4-Byte address mode has been disabled, and then the address length will return to 24-bit.

Figure 9 Disable 4-Byte Mode Sequence Diagram (SPI)

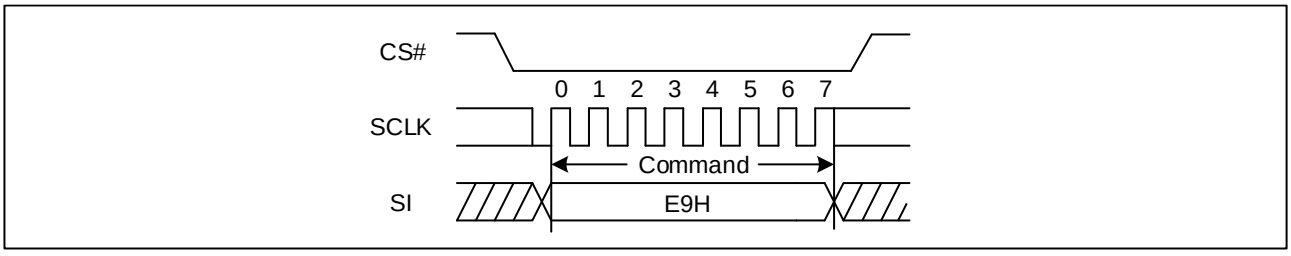
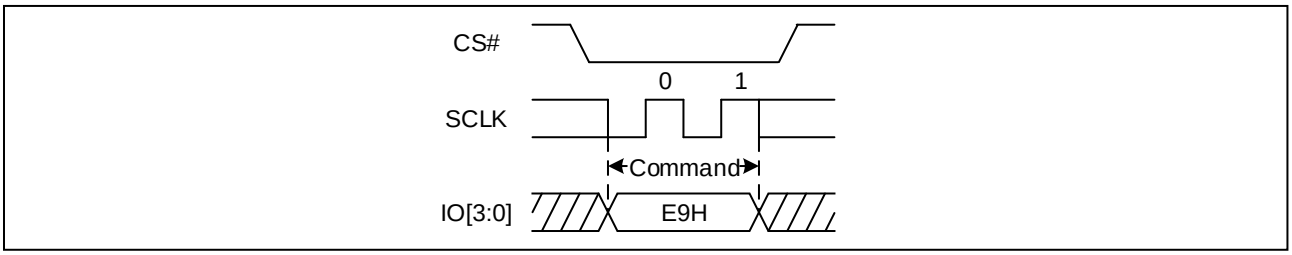


Figure 10 Disable 4-Byte Mode Sequence Diagram (QPI)



8.3 Clear Flag Status Register (30h)

The Clear Status Register Flags command resets bit FS0 (Erase Error bit) and FS1 (Program Error bit) in status register. It is not necessary to set the WEL bit before the Clear Status Register command is executed. The Clear Flag Status Register command will not be accepted when the device remains busy with WIP set to 1. The WEL bit will be unchanged after this command is executed.

Figure 11. Clear Status Register Flags Diagram (SPI)

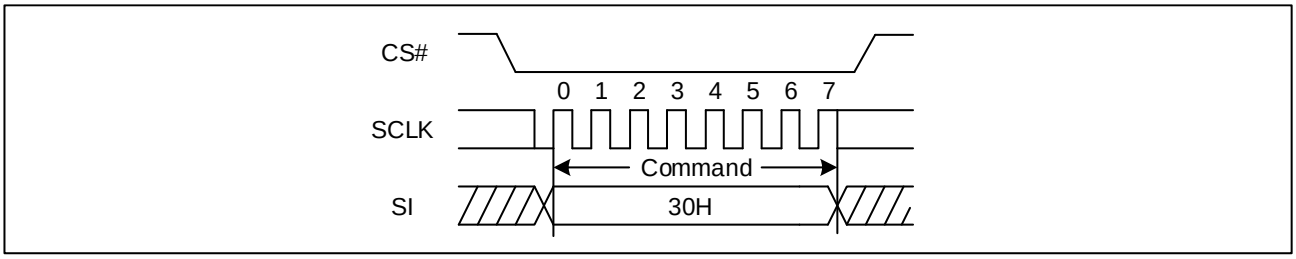
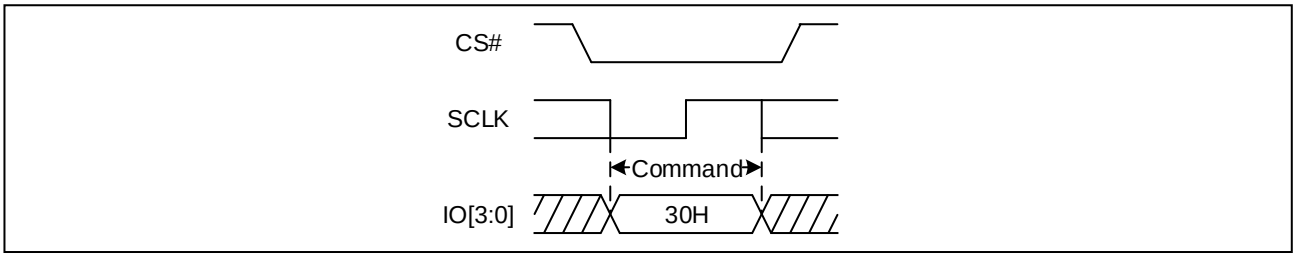


Figure 12. Clear Status Register Flags Diagram (QPI)



8.4 Write Enable (WREN) (06h)

The Write Enable (WREN) command is for setting the Write Enable Latch (WEL) bit. The Write Enable Latch (WEL) bit must be set prior to every Page Program (PP), Sector Erase (SE), Block Erase (BE), Chip Erase (CE), Write Status Register (WRSR), Write Extended Address Register (WEAR), Write Nonvolatile/Volatile configure register and Erase/Program Security Registers command. The Write Enable (WREN) command sequence: CS# goes low → sending the Write Enable command → CS# goes high.

Figure 13 Write Enable Sequence Diagram (SPI)

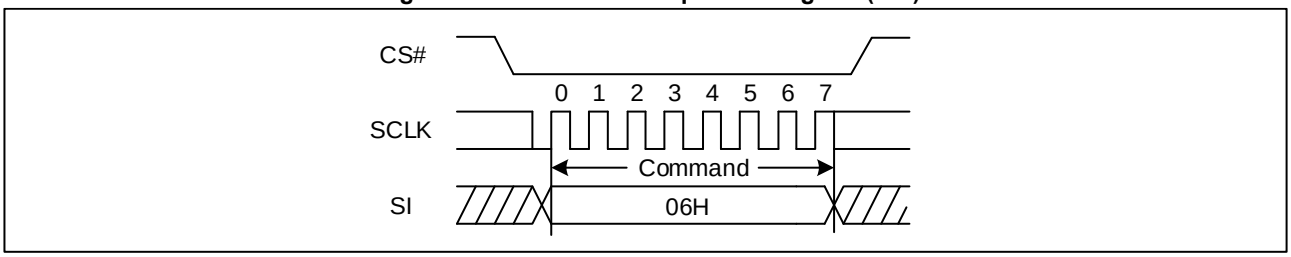
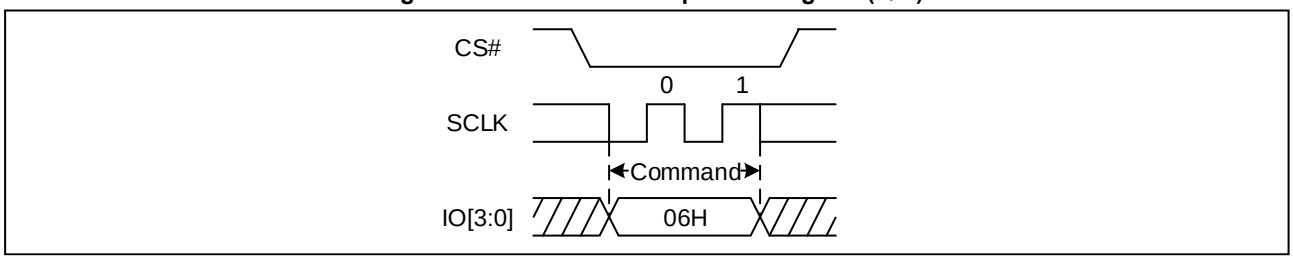


Figure 14 Write Enable Sequence Diagram (QPI)



8.5 Write Disable (WRDI) (04h)

The Write Disable command is for resetting the Write Enable Latch (WEL) bit. The Write Disable command sequence: CS# goes low →Sending the Write Disable command →CS# goes high. The WEL bit is reset by following condition: Power-up and upon completion of the Write Status Register, Write Extended Address Register (WEAR), Write Nonvolatile/Volatile configure register, Page Program, Sector Erase, Block Erase, Chip Erase, Erase/Program Security Registers and Reset commands.

Figure 15 Write Disable Sequence Diagram (SPI)

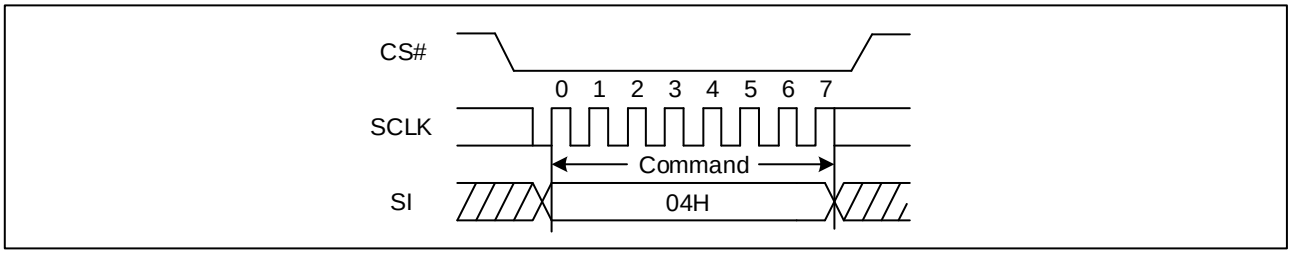
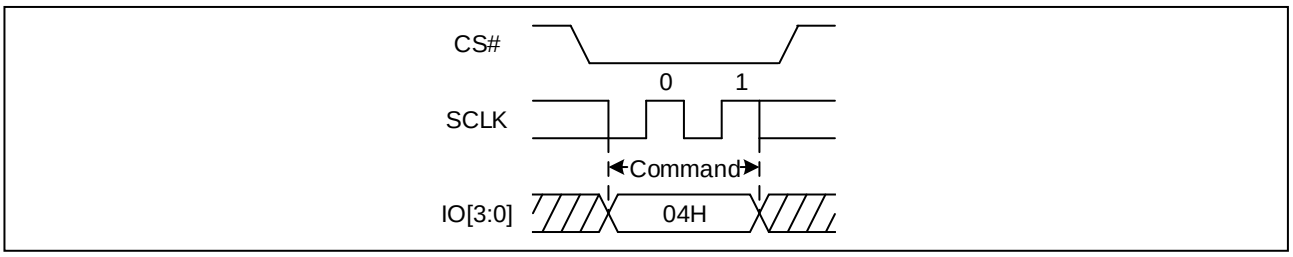


Figure 16 Write Disable Sequence Diagram (QPI)



8.6 Write Enable for Volatile Status Register (50h)

The non-volatile Status Register bits can also be written to as volatile bits. This gives more flexibility to change the system configuration and memory protection schemes quickly without waiting for the typical non-volatile bit write cycles or affecting the endurance of the Status Register non-volatile bits. The Write Enable for Volatile Status Register command must be issued prior to a Write Status Register command, and any other commands cannot be inserted between them. Otherwise, Write Enable for Volatile Status Register will be cleared. The Write Enable for Volatile Status Register command will not set the Write Enable Latch bit, it is only valid for the Write Status Register command to change the volatile Status Register bit values.

Figure 17 Write Enable for Volatile Status Register Sequence Diagram (SPI)

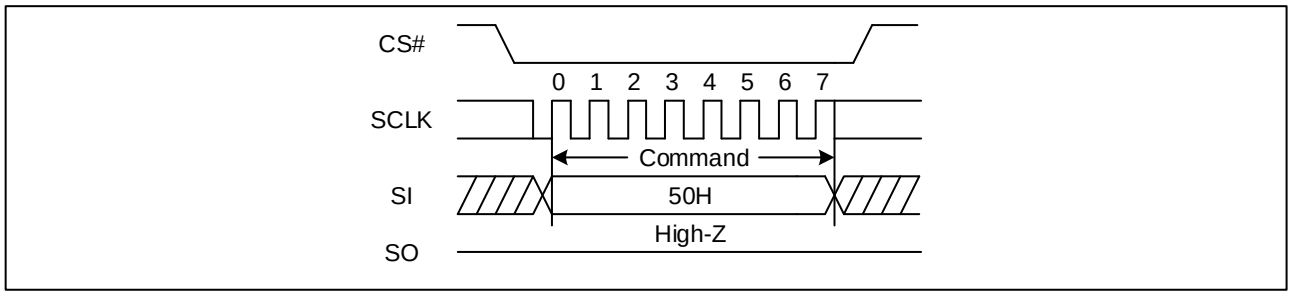
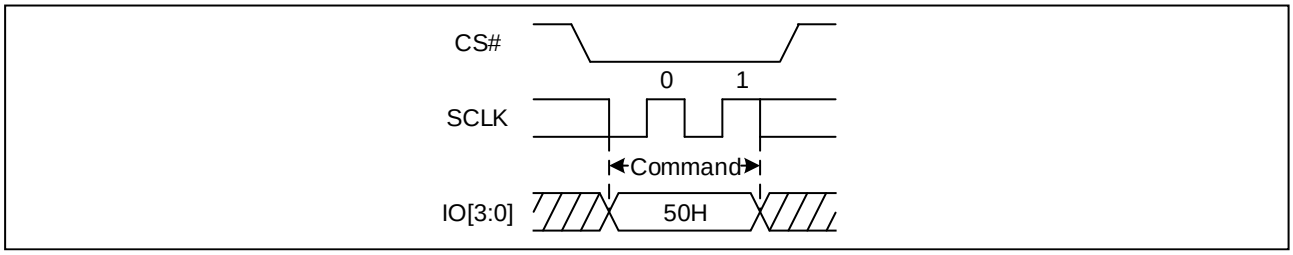


Figure 18 Write Enable for Volatile Status Register Sequence Diagram (QPI)



8.7 Write Status Register (WRSR) (01h/11h)

The Write Status Register (WRSR) command allows new values to be written to the Status Register. Before it can be accepted, a Write Enable (WREN) command must previously have been executed. After the Write Enable (WREN) command has been decoded and executed, the device sets the Write Enable Latch (WEL).

The Write Status Register (WRSR) command has no effect on S19, S15, S10, S9, S1 and S0 of the Status Register. CS# must be driven high after the eighth or sixteen bit of the data byte has been latched in. Otherwise, the Write Status Register (WRSR) command is not executed. If CS# is driven high after eighth bit of the data byte, the alterable bits in Status Register-2 (S15~S8) will be cleared to 0. As soon as CS# is driven high, the self-timed Write Status Register cycle (whose duration is tW) is initiated. While the Write Status Register cycle is in progress, the Status Register may still be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Write Status Register cycle, and is 0 when it is completed. When the cycle is completed, the Write Enable Latch (WEL) is reset.

The Write Status Register (WRSR) command allows the user to change the values of the Block Protect (BP4, BP3, BP2, BP1, and BP0) bits, to define the size of the area that is to be treated as read-only.

01h command is used to write Status Register-1&2. 11h command is used to write Status Register-3.

Figure 19. Write Status Register-1&2 Sequence Diagram (SPI)

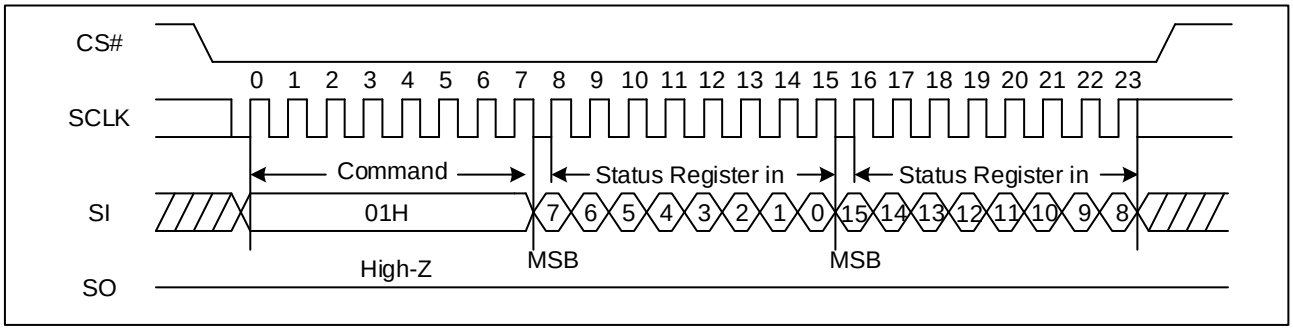


Figure 20. Write Status Register-1&2 Sequence Diagram (QPI)

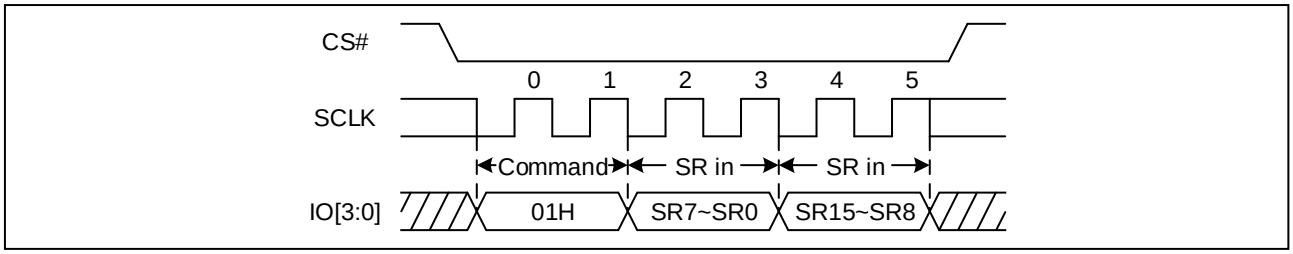


Figure 21. Write Status Register-3 Sequence Diagram (SPI)

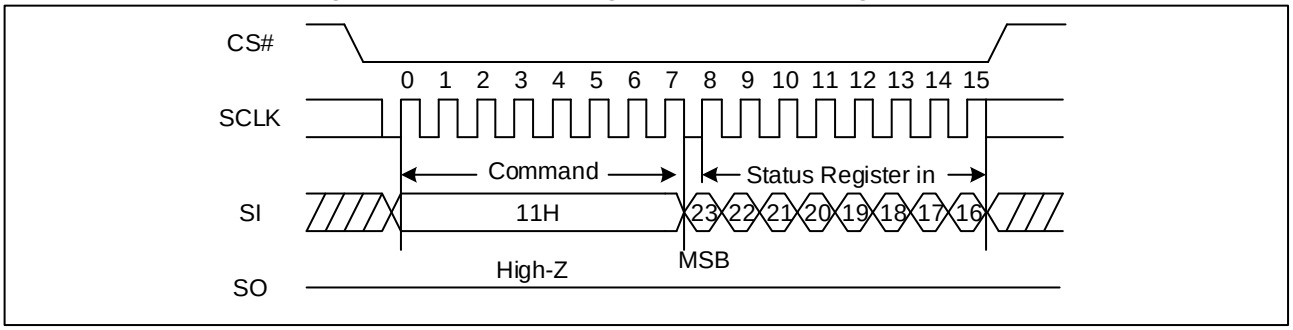
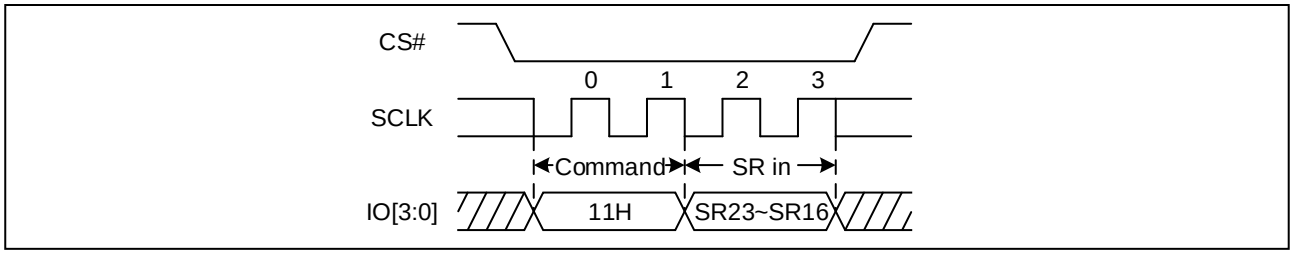


Figure 22. Write Status Register-3 Sequence Diagram (QPI)



8.8 Write Extended Address Register (C5h)

The Extended Address Register is a volatile register that stores the 4th Byte address (A31-A24) when the device is operating in the 3-Byte Address Mode (ADS=0). To write the Extended Address Register bits, a Write Enable (06h) instruction must previously have been executed for the device to accept the Write Extended Address Register instruction (Status Register bit WEL must equal 1). Once write enabled, the instruction is entered by driving CS# low, sending the instruction code “C5h”, and then writing the Extended Address Register data Byte.

Upon power up or the execution of a Software/Hardware Reset, the Extended Address Register bit values will be cleared to 0.

The Extended Address Bit is only effective when the device is in the 3-Byte Address Mode. When the device operates in the 4-Byte Address Mode (ADS=1), any command with address input of A31-A24 will replace the Extended Address Register values. It is recommended to check and update the Extended Address Register if necessary when the device is switched from 4-Byte to 3-Byte Address Mode.

Figure 23 Write Extended Address Register Sequence Diagram (SPI)

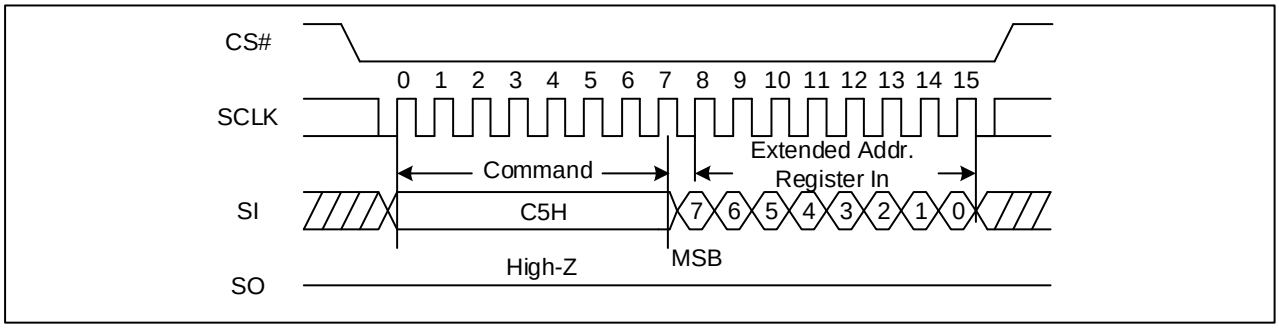
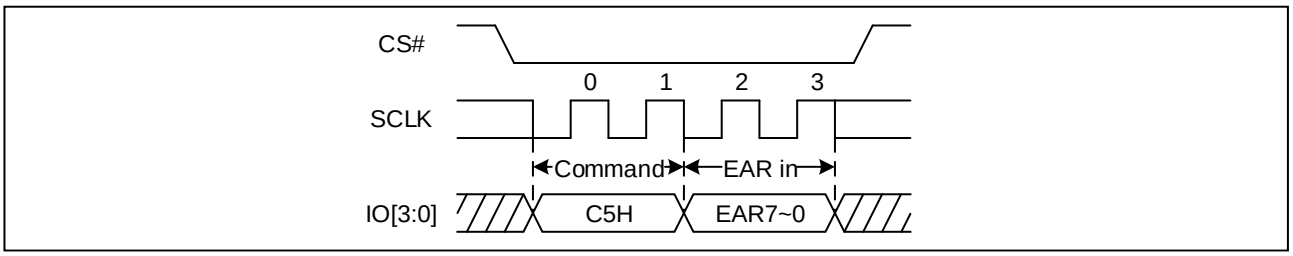


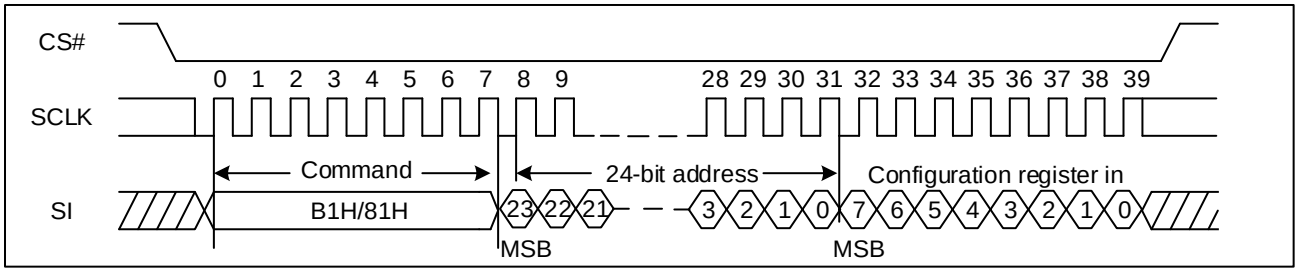
Figure 24 Write Extended Address Register Sequence Diagram (QPI)



8.9 Write Nonvolatile/Volatile Configuration Register (B1h/81h)

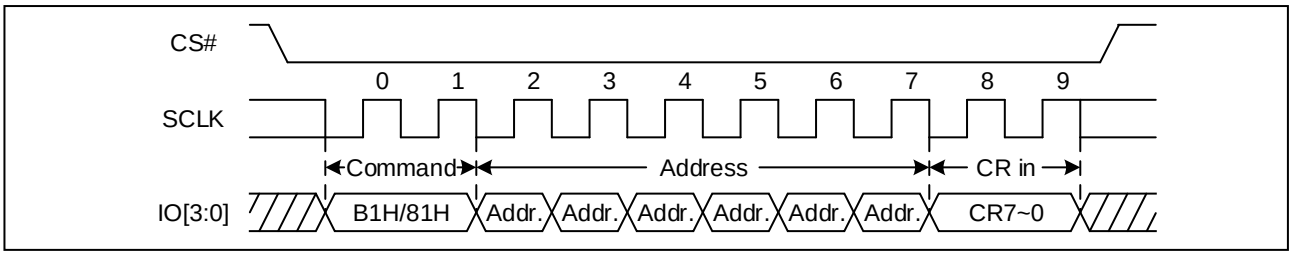
The Write Nonvolatile/Volatile Configuration Register command allows new values to be written to the Nonvolatile/Volatile Configuration Register. Before it can be accepted, a Write Enable (WREN) command must previously have been executed. After the Write Enable (WREN) command has been decoded and executed, the device sets the Write Enable Latch (WEL). CS# must be driven high after the data Byte has been latched in. If not, the Write Configuration Register command is not executed. As soon as CS# is driven high, the self-timed Write Configuration Register cycle (whose duration is tW for B1h) is initiated. The Write In Progress (WIP) bit is 1 during the self-timed Write Configuration Register cycle, and is 0 when it is completed. When the cycle is completed, the Write Enable Latch (WEL) is reset.

Figure 25 Write Nonvolatile/Volatile Configuration Register Sequence Diagram (SPI)



Note: The device default is in 24-bit address mode. For 4-Byte mode, the address length becomes 32-bit.

Figure 26 Write Nonvolatile/Volatile Configuration Register Sequence Diagram (QPI)



Note: The device default is in 24-bit address mode. For 4-Byte mode, the address length becomes 32-bit.

8.10 Read Status Register (05h/35h/15h)

The Read Status Register (RDSR) command is for reading the Status Register. The Status Register may be read at any time, even while a Program, Erase or Write Status Register cycle is in progress. When one of these cycles is in progress, it is recommended to check the Write in Progress (WIP) bit before sending a new command to the device. It is also possible to read the Status Register continuously. For command code of “05h” / “35h” / “15h”, the SO will output Status Register bits S7~S0 / S15-S8 / S23-S16.

Figure 27 Read Status Register Sequence Diagram (SPI)

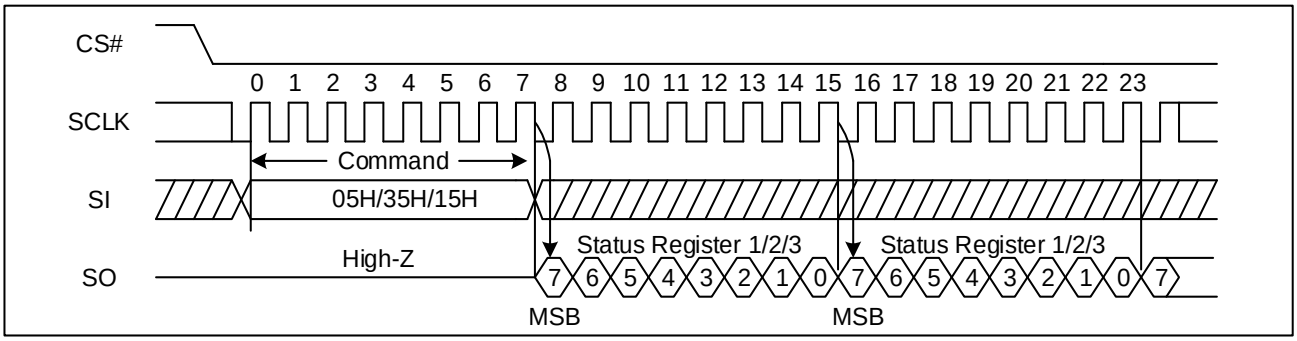
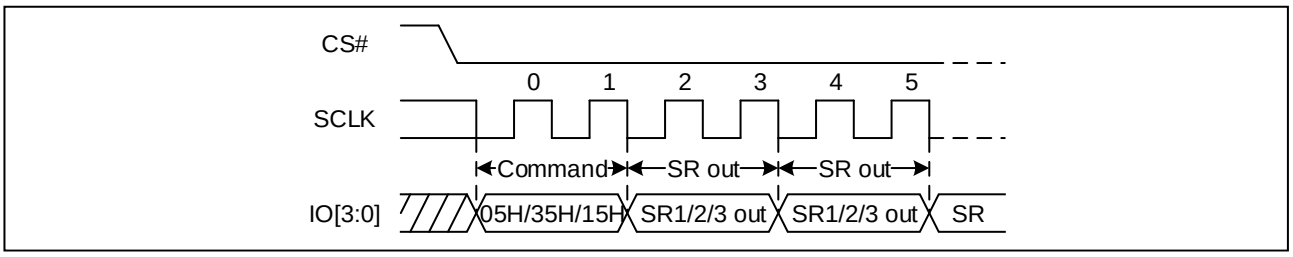


Figure 28 Read Status Register Sequence Diagram (QPI)



8.11 Read Flag Status Register (70h)

The Read Flag Status Register command is for reading the Flag Status Register. The Flag Status Register may be read at any time, even while a Program, Erase or Write Status Register cycle is in progress. When one of these cycles is in progress, it is also possible to read the Flag Status Register continuously.

Figure 29 Read Flag Status Register Sequence Diagram (SPI)

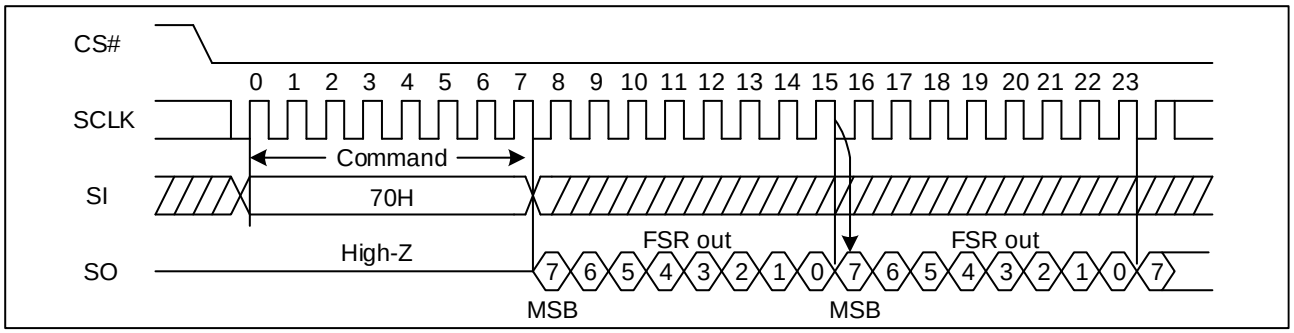
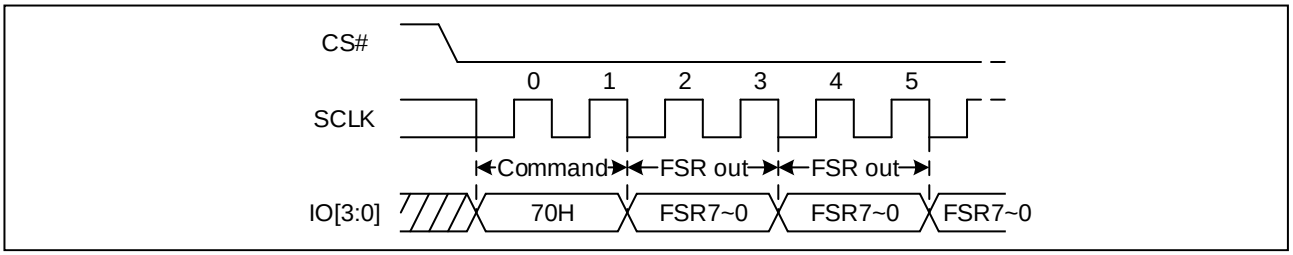


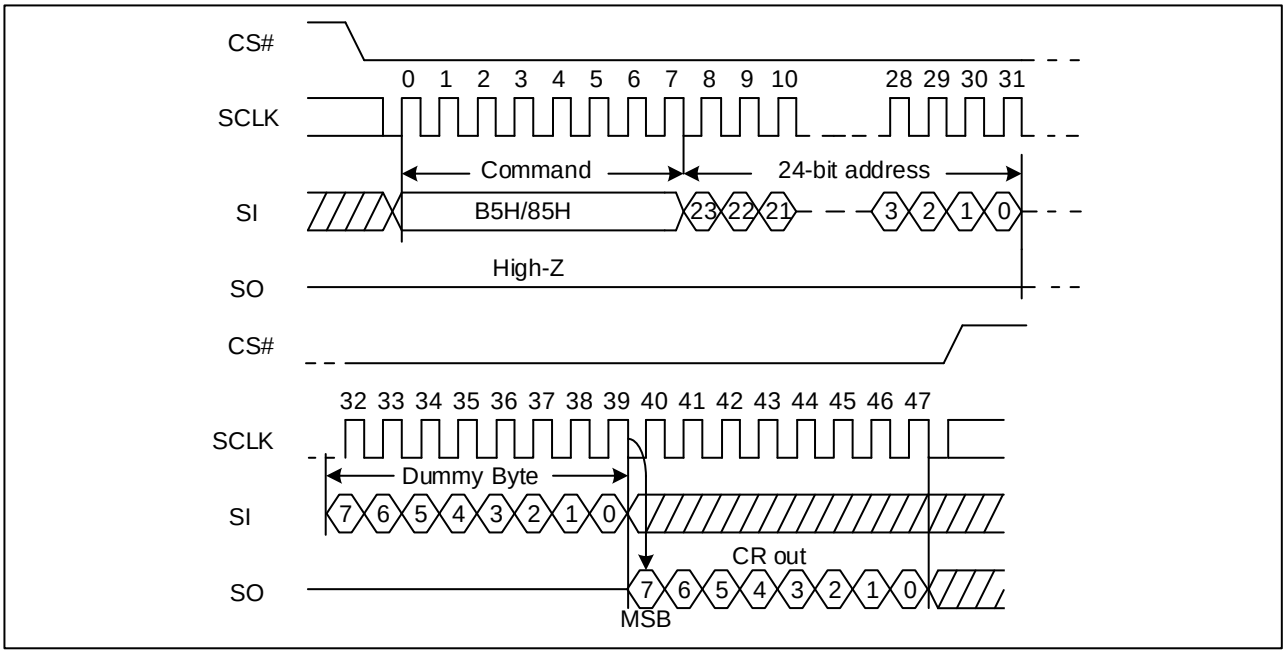
Figure 30 Read Flag Status Register Sequence Diagram (QPI)



8.12 Read Nonvolatile/Volatile Configuration Register (B5h/85h)

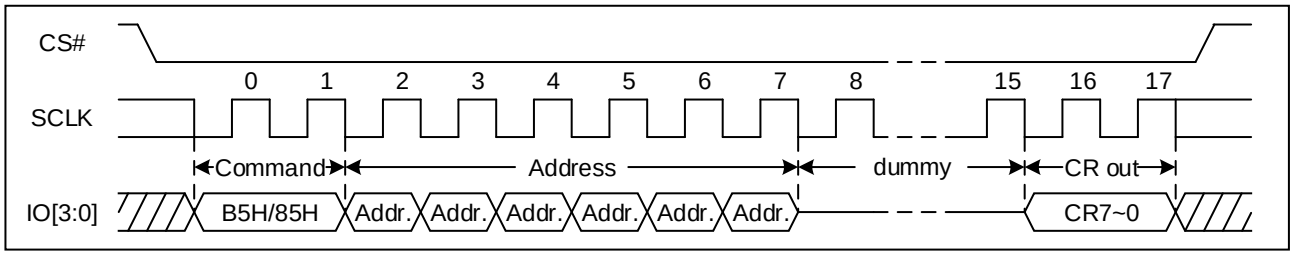
The Read Nonvolatile/Volatile Configuration Register command is for reading the Nonvolatile/Volatile Configuration Registers. It is followed by a 3-Byte address (A23-A0) or a 4-Byte address (A31-A0) and a dummy Byte, and each bit is latched-in on the rising edge of SCLK. Then the Configuration Register, at that address, is shifted out on SO, and each bit is shifted out, at a Max frequency f_C, on the falling edge of SCLK. Read Nonvolatile/Volatile Configuration Register command, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure 31 Read Configuration Registers Sequence Diagram (SPI)



Note: The device default is in 24-bit address mode. For 4-Byte mode, the address length becomes 32-bit.

Figure 32 Read Configuration Registers Sequence (QPI)



Note: The device default is in 24-bit address mode. For 4-Byte mode, the address length becomes 32-bit.

8.13 Read Extended Address Register (C8h)

The Read Extended Address Register instruction is entered by driving CS# low and shifting the instruction code "C8H" into the SI pin on the rising edge of SCLK. The Extended Address Register bits are then shifted out on the SO pin at the falling edge of SCLK with most significant bit (MSB) first.

When the device is in the 4-Byte Address Mode, the value of the address bits is ignored.

Figure 33 Read Extended Address Register Sequence Diagram (SPI)

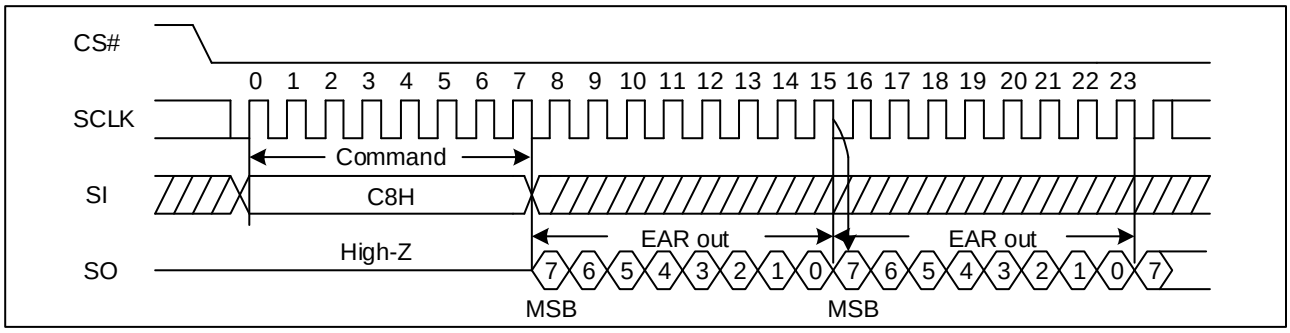
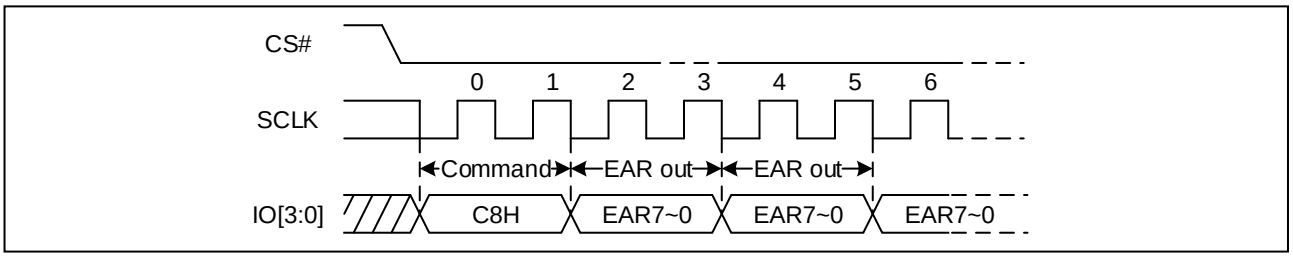


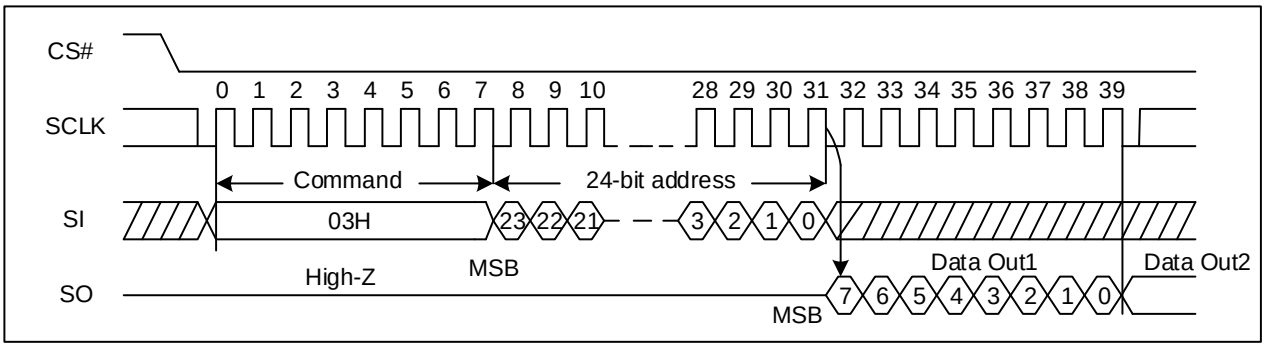
Figure 34 Read Extended Address Register Sequence Diagram (QPI)



8.14 Read Data Bytes (03h/13h)

The Read Data Bytes (READ) command is followed by a 3-Byte address (A23-A0) or a 4-Byte address (A31-A0), and each bit is latched-in on the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, and each bit is shifted out, at a Max frequency fR, on the falling edge of SCLK. The first Byte addressed can be at any location. The address is automatically incremented to the next higher address after each Byte of data is shifted out. The whole memory can, therefore, be read with a single Read Data Bytes (READ) command. Any Read Data Bytes (READ) command, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure 35 Read Data Bytes Sequence Diagram

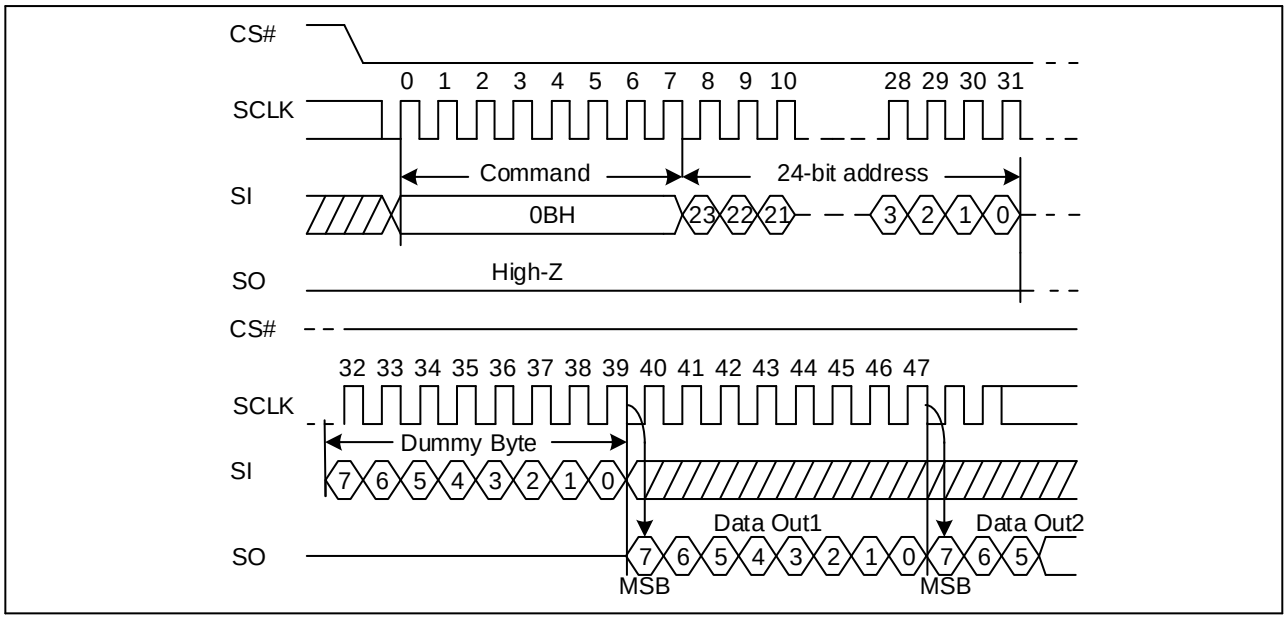


Note: The device default is in 24-bit address mode. For 4-Byte mode, the address length becomes 32-bit.

8.15 Read Data Bytes at Higher Speed (0Bh/0Ch)

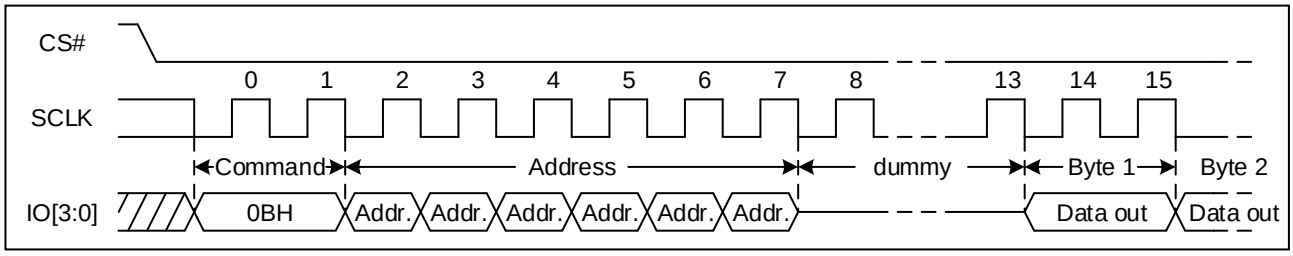
The Read Data Bytes at Higher Speed (Fast Read) command is for quickly reading data out. It is followed by a 3-Byte address (A23-A0) or a 4-Byte address (A31-A0) and dummy clocks, and each bit is latched-in on the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, and each bit is shifted out, at a Max frequency f_C, on the falling edge of SCLK. The first Byte addressed can be at any location. The address is automatically incremented to the next higher address after each Byte of data is shifted out.

Figure 36 Read Data Bytes at Higher Speed Sequence Diagram (SPI)



Note: The device default is in 24-bit address mode. For 4-Byte mode, the address length becomes 32-bit.

Figure 37 Read Data Bytes at Higher Speed Sequence Diagram (QPI)



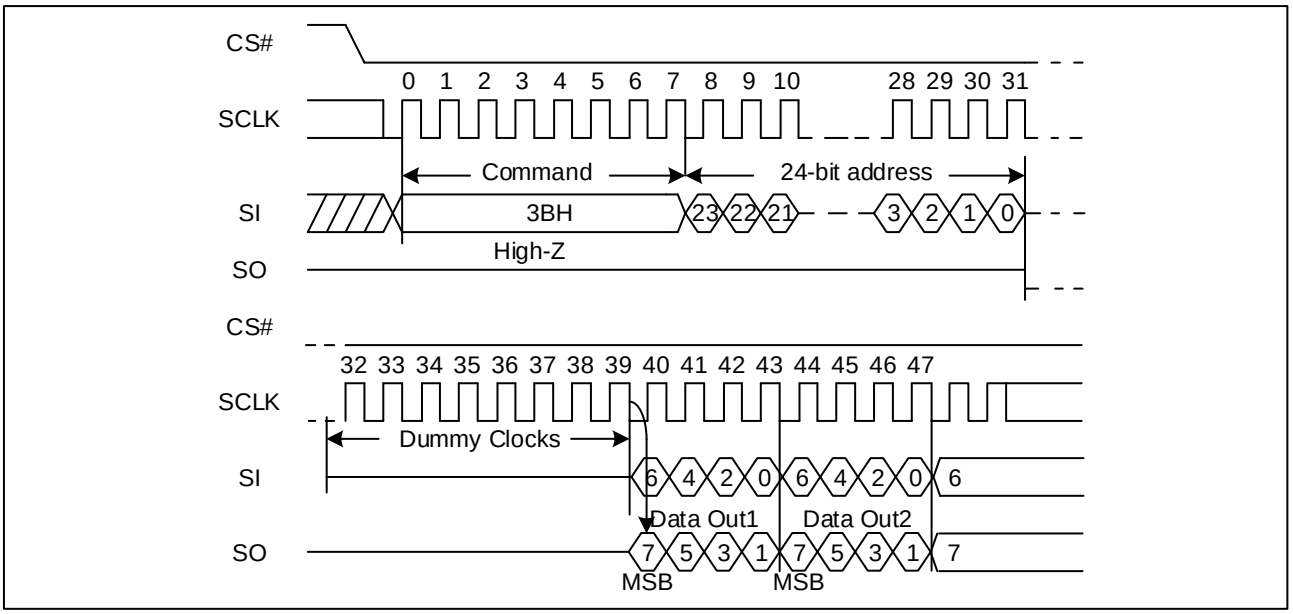
Note: The device default is in 24-bit address mode. For 4-Byte mode, the address length becomes 32-bit.

8.16 Dual Output Fast Read (3Bh/3Ch)

The Dual Output Fast Read command is followed by 3/4-Byte address and a dummy Byte, and each bit being latched in on the rising edge of SCLK, then the memory contents are shifted out 2-bit per clock cycle from SI and SO.

The first Byte addressed can be at any location. The address is automatically incremented to the next higher address after each Byte of data is shifted out.

Figure 38. Dual Output Fast Read Sequence Diagram

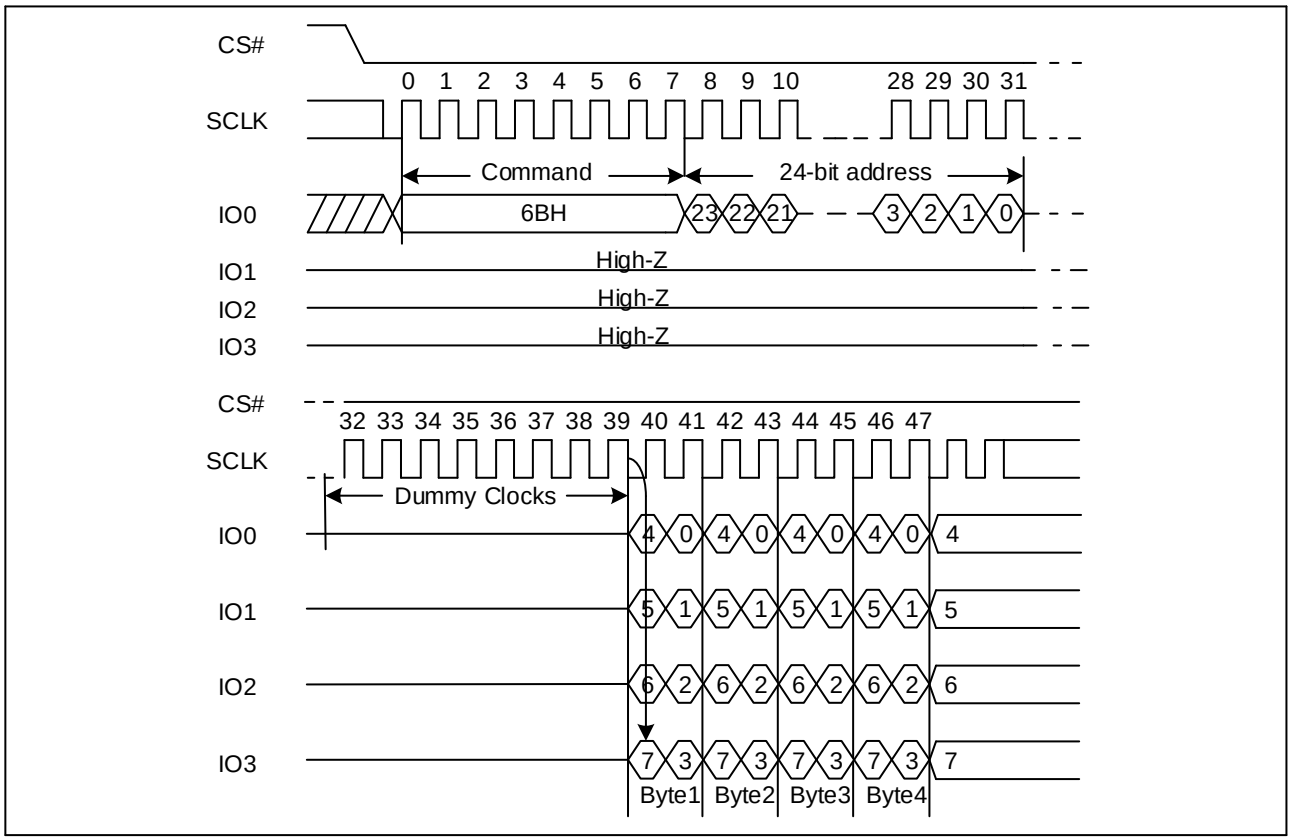


Note: The device default is in 24-bit address mode. For 4-Byte mode or 4-Byte command, the address length is 32-bit.

8.17 Quad Output Fast Read (6Bh/6Ch)

The Quad Output Fast Read command is followed by 3-Byte address (A23-A0) or a 4-Byte address (A31-A0) and dummy clocks, and each bit is latched in on the rising edge of SCLK, then the memory contents are shifted out 4-bit per clock cycle from IO3, IO2, IO1 and IO0. The first Byte addressed can be at any location. The address is automatically incremented to the next higher address after each Byte of data is shifted out.

Figure 39 Quad Output Fast Read Sequence Diagram (SPI)



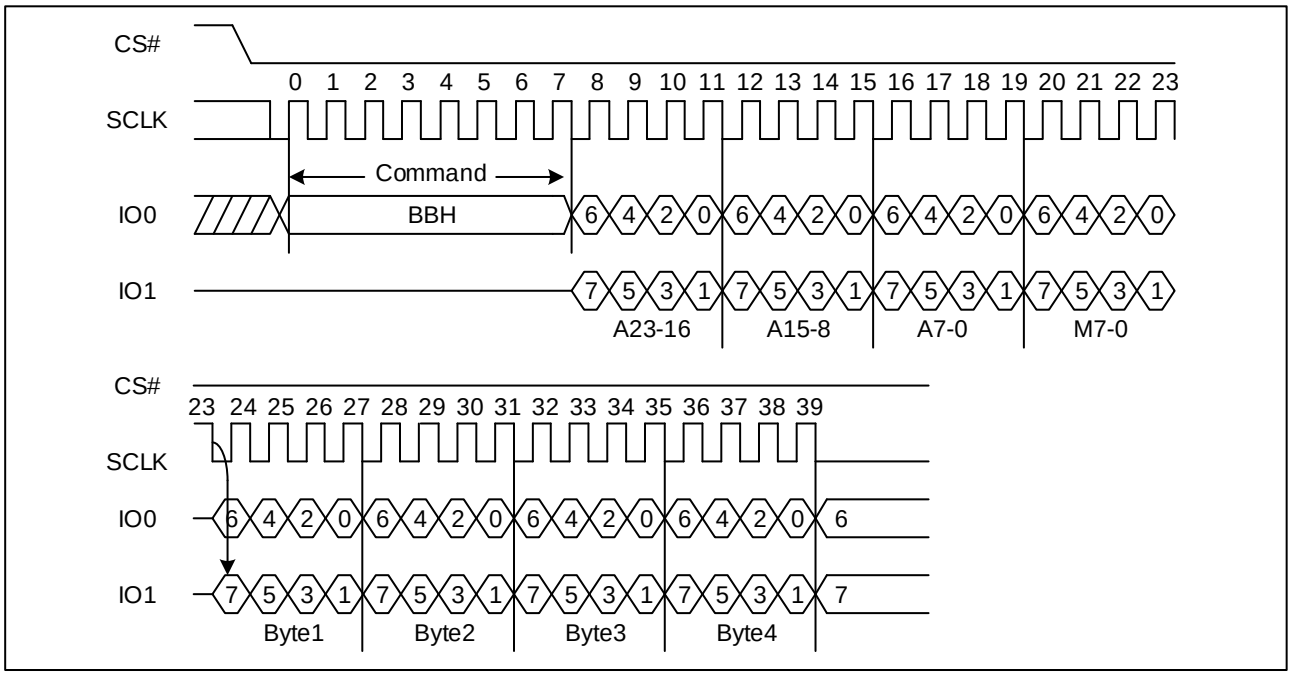
Note: The device default is in 24-bit address mode. For 4-Byte mode, the address length becomes 32-bit.

8.18 Dual I/O Fast Read (BBh/BCh)

The Dual I/O Fast Read command is similar to the Dual Output Fast Read command but with the capability to input the 3/4-Byte address and a “Continuous Read Mode” Byte 2-bit per clock by SI and SO, and each bit being latched in on the rising edge of SCLK, then the memory contents are shifted out 2-bit per clock cycle from SI and SO. The first Byte addressed can be at any location. The address is automatically incremented to the next higher address after each Byte of data is shifted out.

"Continuous Read Mode" bits must NOT be set as (M5-4) = (1, 0)

Figure 40 Dual I/O Fast Read Sequence Diagram ((M5-4) ≠ (1, 0))



Note:

1. The device default is in 24-bit address mode. For 4-Byte mode or 4-Byte command, the address length is 32-bit.
2. M5-4 must **not** be set as (1, 0).

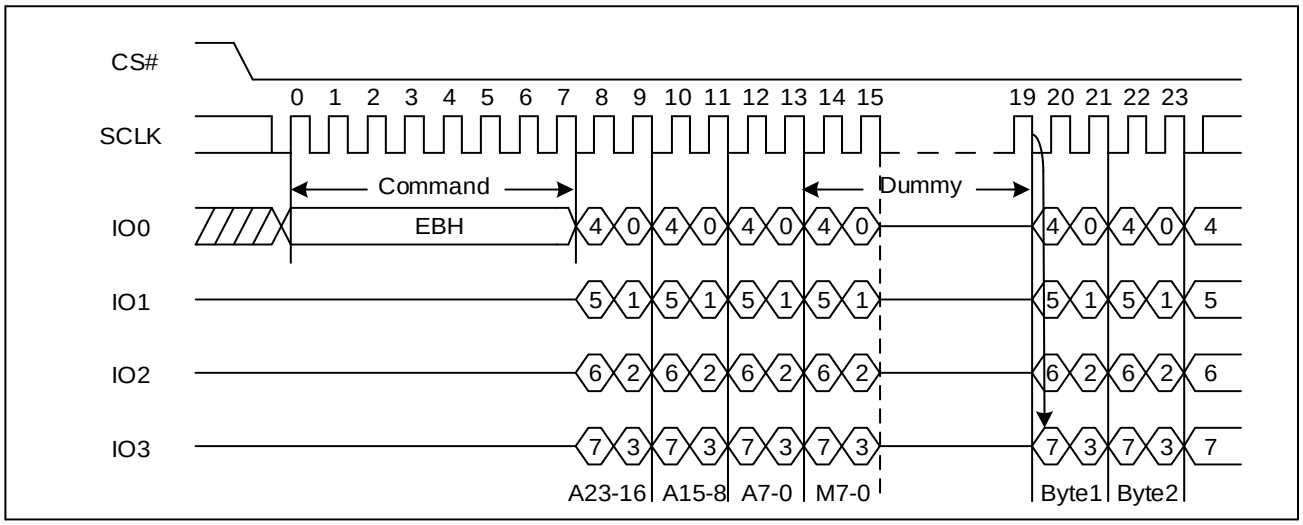
8.19 Quad I/O Fast Read (EBh/ECh)

The Quad I/O Fast Read command is similar to the Quad Output Fast Read command but with the capability to input the 3-Byte address (A23-A0) or a 4-Byte address (A31-A0) and a “Continuous Read Mode” Byte and dummy clocks. 4-bit per clock is transferred by IO0, IO1, IO2, IO3, and each bit is latched in on the rising edge of SCLK, then the memory contents are shifted out 4-bit per clock cycle from IO0, IO1, IO2, IO3. The first Byte addressed can be at any location. The address is automatically incremented to the next higher address after each Byte of data is shifted out.

The Quad I/O Fast Read command is also supported in QPI mode. In QPI mode, the number of dummy clocks is configured by the “Set Read Parameters (C0h)” command to accommodate a wide range application with different needs for either maximum Fast Read frequency or minimum data access latency. Depending on the Read Parameter Bits P5~P4 setting, the number of dummy clocks can be configured. To reach the maximum frequency, the device must be set in QPI mode with most dummy clocks. In QPI mode, the “Continuous Read Mode” bits M7-M0 are also considered as dummy clocks. “Continuous Read Mode” feature is not available in QPI mode for Quad I/O Fast Read command. “Wrap Around” feature is not available in QPI mode for Quad I/O Fast Read command. To perform a read operation with fixed data length wrap around in QPI mode, a dedicated “Burst Read with Wrap” (0Ch) command must be used.

"Continuous Read Mode" bits must NOT be set as (M5-4) = (1, 0)

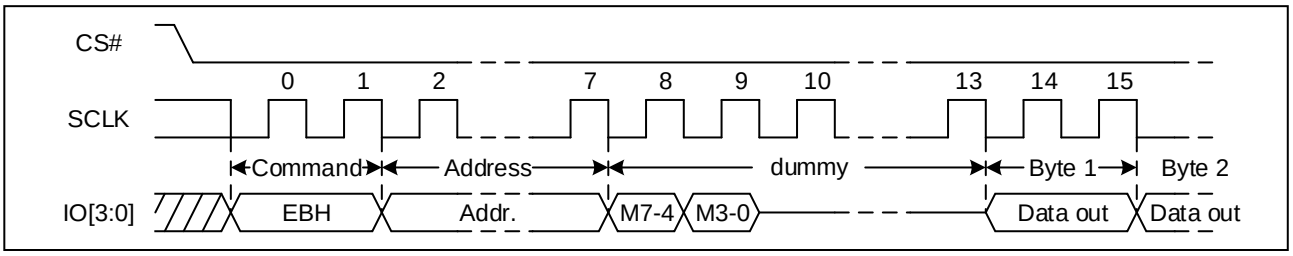
Figure 41 Quad I/O Fast Read Sequence Diagram (SPI, M5-4≠ (1, 0))



Note:

1. The device default is in 24-bit address mode. For 4-Byte mode, the address length becomes 32-bit.
2. M5-4 must **not** be set as (1, 0).

Figure 42 Quad I/O Fast Read Sequence Diagram (QPI, M5-4≠ (1, 0))



Note:

1. The device default is in 24-bit address mode. For 4-Byte mode, the address length becomes 32-bit.
2. M5-4 must **not** be set as (1, 0).

Quad I/O Fast Read with "8/16/32/64-Byte Wrap Around"

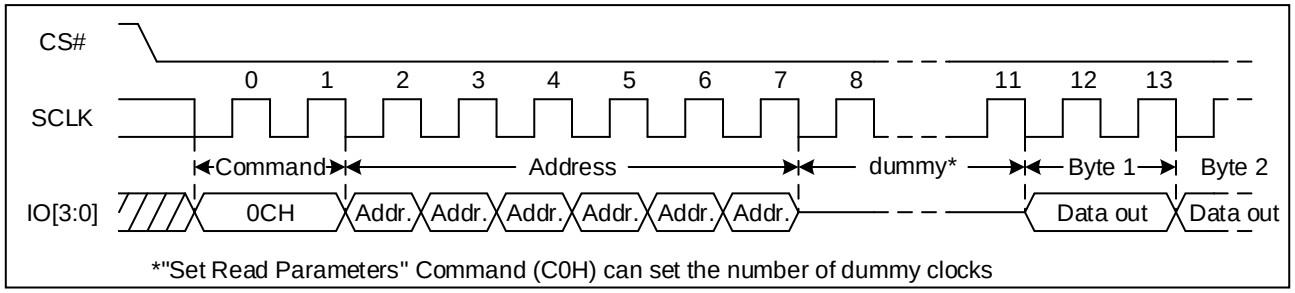
The Quad I/O Fast Read command can be used to access a specific portion within a page by issuing Wrap configuration register Byte prior to EBh/ECh. The data being accessed can be limited to either a 8/16/32/64-Byte section of a 256-Byte page. The output data starts at the initial address specified in the command, once it reaches the ending boundary of the 8/16/32/64-Byte section, the output will wrap around the beginning boundary automatically until CS# is pulled high to terminate the command.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-Byte) of data without issuing multiple read commands.

8.20 Burst Read with Wrap (0Ch)

The "Burst Read with Wrap (0Ch)" command provides an alternative way to perform the read operation with "Wrap Around" in QPI mode. This command is similar to the "Fast Read (0Bh)" command in QPI mode, except the addressing of the read operation will "Wrap Around" to the beginning boundary of the "Wrap Around" once the ending boundary is reached. The "Wrap Length" and the number of dummy clocks can be configured by the "Set Read Parameters (C0h)" command.

Figure 43. Burst Read with Wrap Sequence Diagram



Note: The device default is in 24-bit address mode. For 4-Byte mode, the address length becomes 32-bit.

8.21 Set Burst with Wrap (77h)

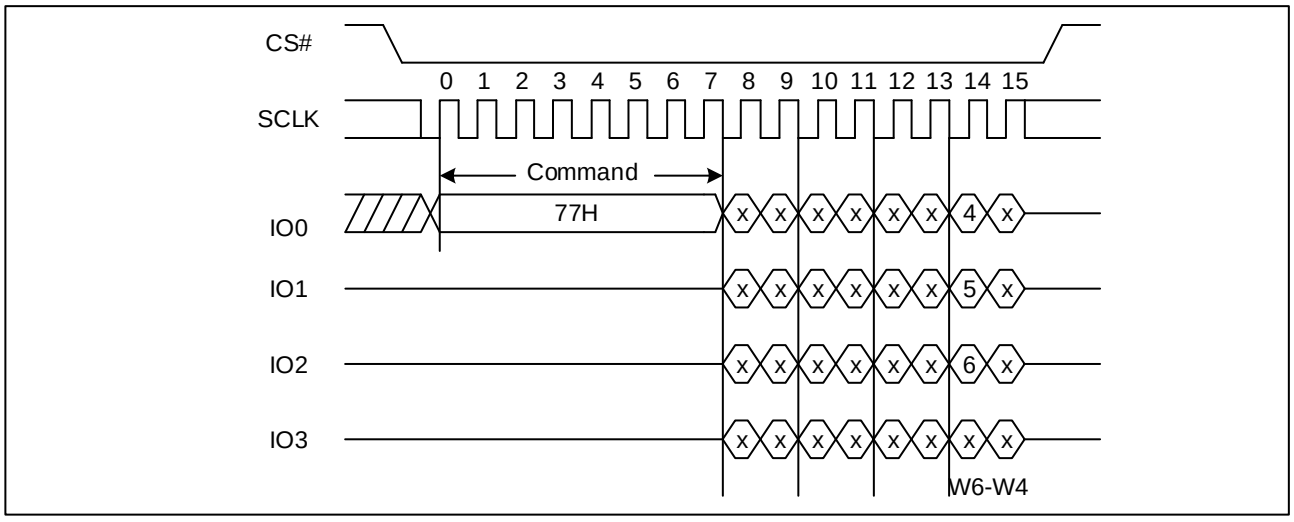
The Set Burst with Wrap command is used in conjunction with "Quad I/O Fast Read" command to access a fixed length of 8/16/32/64-byte section within a 256-byte page, in standard SPI mode.

The Set Burst with Wrap command sequence: CS# goes low → Send Set Burst with Wrap command → Send 24 dummy bits → Send 8 bits "Wrap bits" → CS# goes high.

W6,W5	W4=0		W4=1 (default)	
	Wrap Around	Wrap Length	Wrap Around	Wrap Length
0, 0	Yes	8-byte	No	N/A
0, 1	Yes	16-byte	No	N/A
1, 0	Yes	32-byte	No	N/A
1, 1	Yes	64-byte	No	N/A

If the W6-W4 bits are set by the Set Burst with Wrap command, all the following "Quad I/O Fast Read" command will use the W6-W4 setting to access the 8/16/32/64-byte section within any page. To exit the "Wrap Around" function and return to normal read operation, another Set Burst with Wrap command should be issued to set W4=1.

Figure 44. Set Burst with Wrap Sequence Diagram



8.22 Set Read Parameters (C0h)

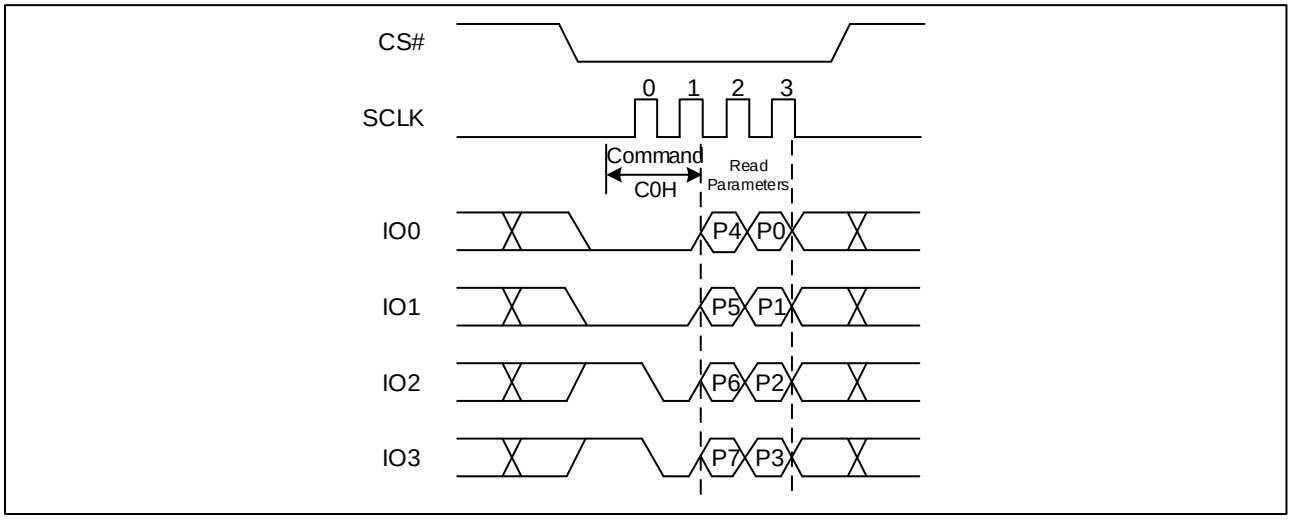
In QPI mode the "Set Read Parameters (C0h)" command can be used to configure the number of dummy clocks for "Fast Read (0Bh)", "Quad I/O Fast Read (EBh)" and "Burst Read with Wrap (0Ch)" command, and to configure the number of

bytes of “Wrap Length” for the “Burst Read with Wrap (0Ch)” command. The “Wrap Length” is set by W5-6 bit in the “Set Burst with Wrap (77h)” command. This wrap setting will remain unchanged when the device is switched from Standard SPI mode to QPI mode.

P5-P4	Dummy Clocks	Maximum Read Freq.	P1-P0	Wrap Length
0 0(Default)	4	80MHz	0 0(Default)	8-byte
0 1	6	104MHz	0 1	16-byte
1 0	8	104MHz	1 0	32-byte
1 1	Reserved	Reserved	1 1	64-byte

Note: Default from power up or reset.

Figure 45. Set Read Parameters command Sequence Diagram



8.23 Page Program (PP) (02h/12h)

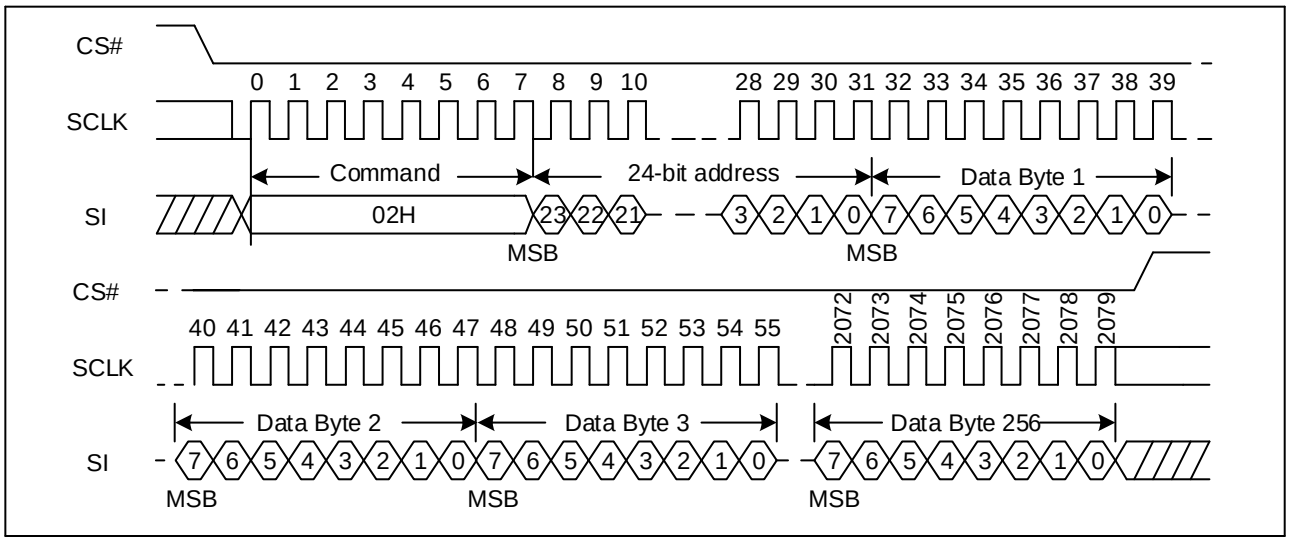
The Page Program (PP) command is for programming the memory. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Page Program command.

The Page Program (PP) command is entered by driving CS# Low, followed by the command code, three or four address Bytes and at least one data Byte on SI. If the 8 least significant address bits (A7-A0) are not all zero, all transmitted data that goes beyond the end of the current page are programmed from the start address of the same page (from the address whose 8 least significant bits (A7-A0) are all zero). CS# must be driven low for the entire duration of the sequence. The Page Program command sequence: CS# goes low → sending Page Program command → 3-Byte address or 4-Byte address on SI → at least 1 Byte data on SI → CS# goes high. If more than 256 Bytes are sent to the device, previously latched data are discarded and the last 256 data Bytes are guaranteed to be programmed correctly within the same page. If less than 256 data Bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other Bytes of the same page. CS# must be driven high after the eighth bit of the last data Byte has been latched in; otherwise the Page Program (PP) command is not executed.

As soon as CS# is driven high, the self-timed Page Program cycle (whose duration is t_{PP}) is initiated. While the Page Program cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Page Program cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

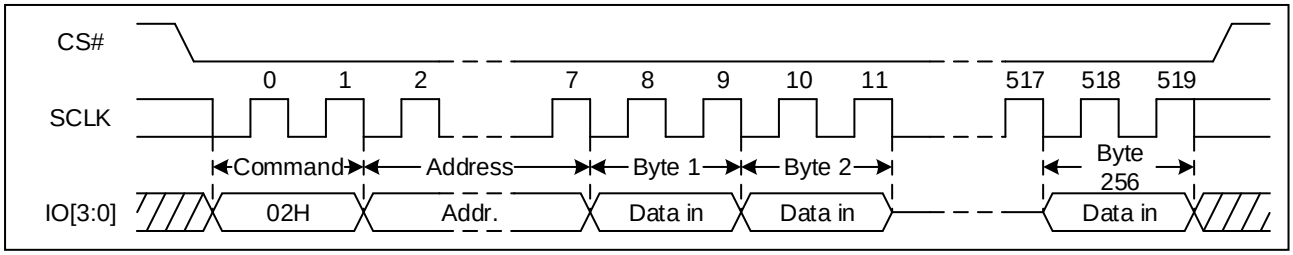
A Page Program (PP) command applied to a page which is protected by the Block Protect (BP4, BP3, BP2, BP1, and BP0) is not executed.

Figure 46 Page Program Sequence Diagram (SPI)



Note: The device default is in 24-bit address mode. For 4-Byte mode, the address length becomes 32-bit.

Figure 47 Page Program Sequence Diagram (QPI)



Note: The device default is in 24-bit address mode. For 4-Byte mode, the address length becomes 32-bit.

8.24 Quad Page Program (32h/34h)

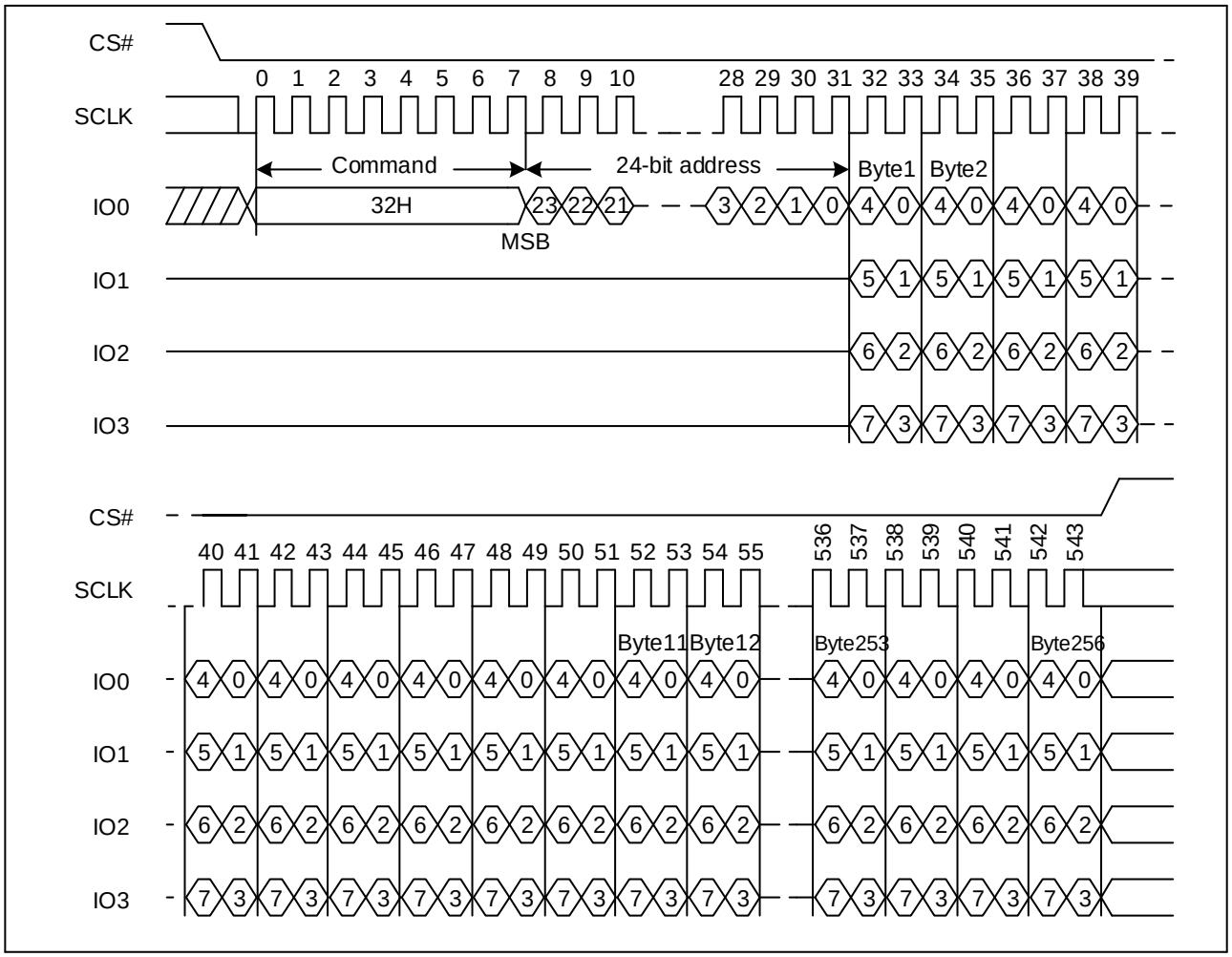
The Quad Page Program command is for programming the memory using four pins: IO0, IO1, IO2, and IO3. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Page Program command. The quad Page Program command is entered by driving CS# Low, followed by the command code (32h/34h), three or four address Bytes and at least one data Byte on IO pins.

If more than 256 Bytes are sent to the device, previously latched data are discarded and the last 256 data Bytes are guaranteed to be programmed correctly within the same page. If less than 256 data Bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other Bytes of the same page. CS# must be driven high after the eighth bit of the last data Byte has been latched in; otherwise the Quad Page Program (PP) command is not executed.

As soon as CS# is driven high, the self-timed Quad Page Program cycle (whose duration is t_{PP}) is initiated. While the Quad Page Program cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Quad Page Program cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

A Quad Page Program command applied to a page which is protected by the Block Protect (BP4, BP3, BP2, BP1, and BP0) is not executed.

Figure 48 Quad Page Program Sequence Diagram (SPI)

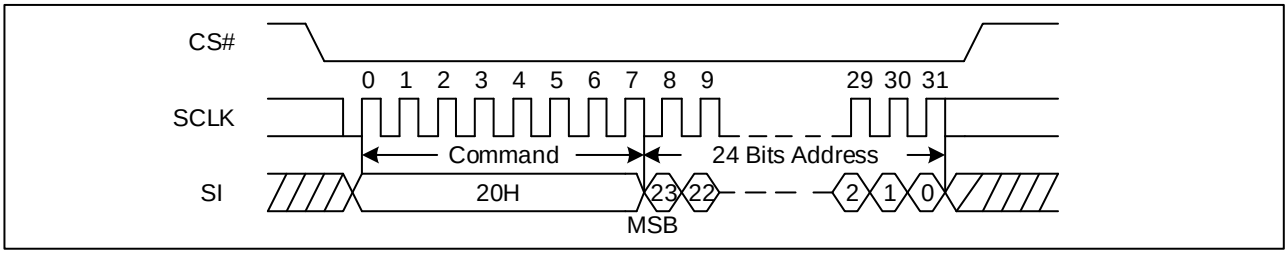


Note: The device default is in 24-bit address mode. For 4-Byte mode, the address length becomes 32-bit.

8.25 Sector Erase (SE) (20h/21h)

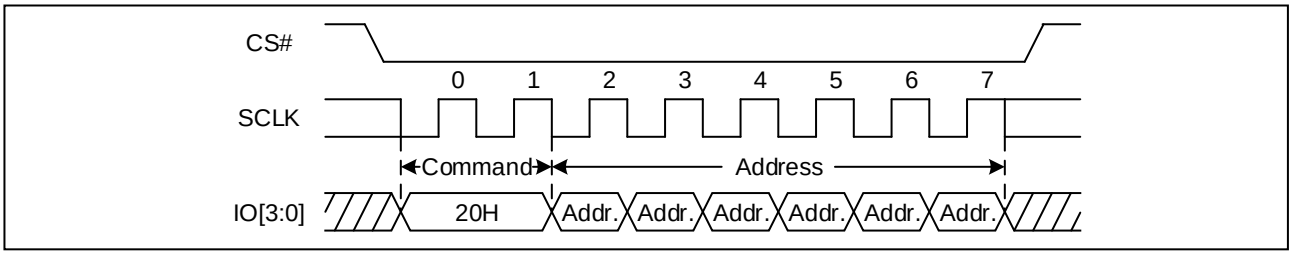
The Sector Erase (SE) command is erased the all data of the chosen sector. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit. The Sector Erase (SE) command is entered by driving CS# low, followed by the command code, and 3- Byte address or 4-Byte address on SI. Any address inside the sector is a valid address for the Sector Erase (SE) command. CS# must be driven low for the entire duration of the sequence. The Sector Erase command sequence: CS# goes low → sending Sector Erase command → 3-Byte address or 4-Byte address on SI → CS# goes high. CS# must be driven high after the eighth bit of the last address Byte has been latched in; otherwise the Sector Erase (SE) command is not executed. As soon as CS# is driven high, the self-timed Sector Erase cycle (whose duration is t_{SE}) is initiated. While the Sector Erase cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Sector Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. A Sector Erase (SE) command applied to a sector which is protected by the Block Protect (BP4, BP3, BP2, BP1, and BP0) bits is not executed.

Figure 49 Sector Erase Sequence Diagram (SPI)



Note: The device default is in 24-bit address mode. For 4-Byte mode, the address length becomes 32-bit.

Figure 50 Sector Erase Sequence Diagram (QPI)

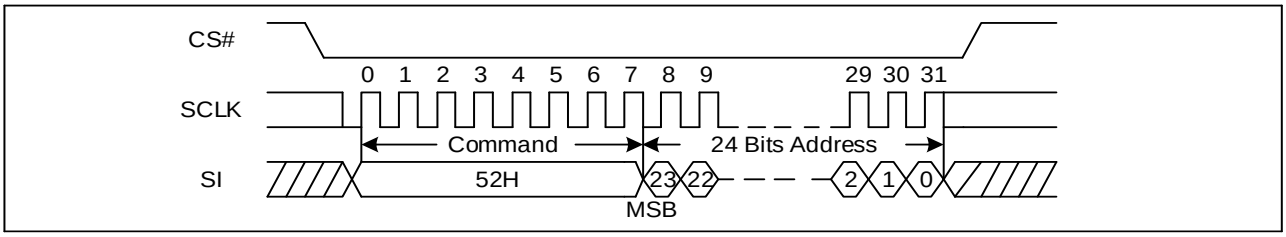


Note: The device default is in 24-bit address mode. For 4-Byte mode, the address length becomes 32-bit.

8.26 32KB Block Erase (BE32) (52h/5Ch)

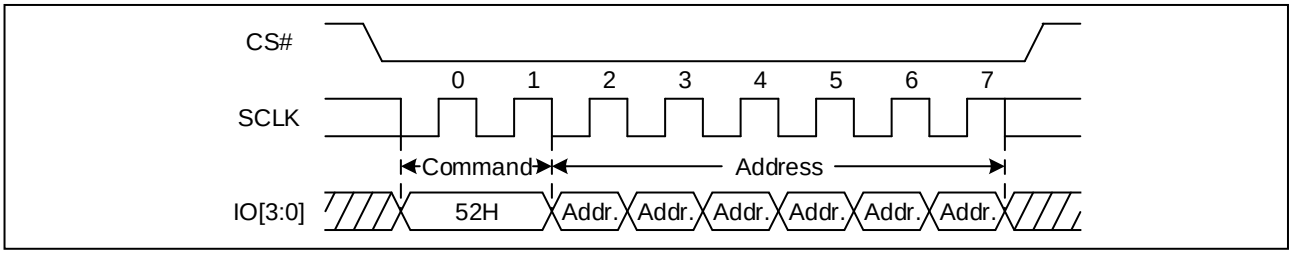
The 32KB Block Erase command is erased the all data of the chosen block. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit. The 32KB Block Erase (BE) command is entered by driving CS# low, followed by the command code, and 3-Byte address or 4-Byte address on SI. Any address inside the block is a valid address for the 32KB Block Erase command. CS# must be driven low for the entire duration of the sequence. The 32KB Block Erase command sequence: CS# goes low → sending 32KB Block Erase command → 3-Byte address or 4-Byte address on SI → CS# goes high. CS# must be driven high after the eighth bit of the last address Byte has been latched in; otherwise the 32KB Block Erase command is not executed. As soon as CS# is driven high, the self-timed Block Erase cycle (whose duration is t_{BE1}) is initiated. While the Block Erase cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Block Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. A 32KB Block Erase command applied to a block which is protected by the Block Protect (BP4, BP3, BP2, BP1, and BP0) bits is not executed.

Figure 51 32KB Block Erase Sequence Diagram (SPI)



Note: The device default is in 24-bit address mode. For 4-Byte mode, the address length becomes 32-bit.

Figure 52 32KB Block Erase Sequence Diagram (QPI)



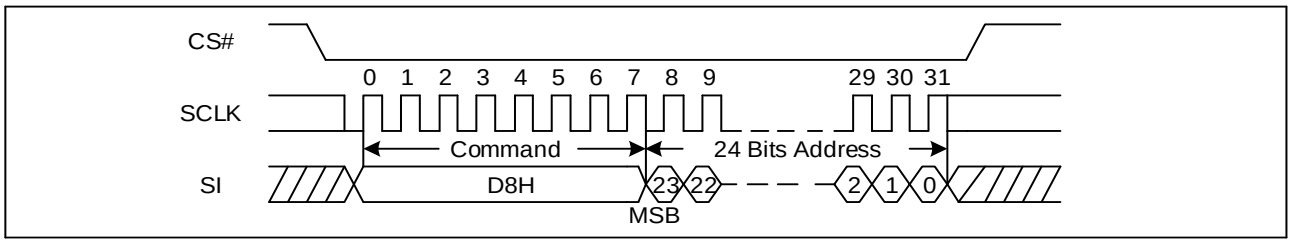
Note: The device default is in 24-bit address mode. For 4-Byte mode, the address length becomes 32-bit.

8.27 64KB Block Erase (BE64) (D8h/DCh)

The 64KB Block Erase command is erased the all data of the chosen block. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit. The 64KB Block Erase command is entered by driving CS# low, followed by the command code, and 3-Byte address or 4-Byte address on SI. Any address inside the block is a valid address for the 64KB Block Erase command. CS# must be driven low for the entire duration of the sequence.

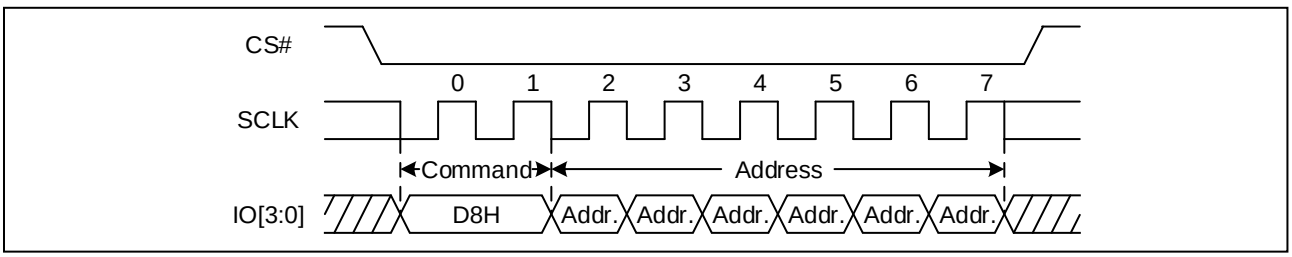
The 64KB Block Erase command sequence: CS# goes low → sending 64KB Block Erase command → 3-Byte address or 4-Byte address on SI → CS# goes high. CS# must be driven high after the eighth bit of the last address Byte has been latched in; otherwise the 64KB Block Erase command is not executed. As soon as CS# is driven high, the self-timed Block Erase cycle (whose duration is t_{BE2}) is initiated. While the Block Erase cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Block Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. A 64KB Block Erase command applied to a block which is protected by the Block Protect (BP4, BP3, BP2, BP1, and BP0) bits is not executed.

Figure 53 64KB Block Erase Sequence Diagram (SPI)



Note: The device default is in 24-bit address mode. For 4-Byte mode, the address length becomes 32-bit.

Figure 54 64KB Block Erase Sequence Diagram (QPI)



Note: The device default is in 24-bit address mode. For 4-Byte mode, the address length becomes 32-bit.

8.28 Chip Erase (CE) (60h/C7h)

The Chip Erase (CE) command is erased the all data of the chip. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit .The Chip Erase (CE) command is entered by driving CS# Low, followed by the command code on Serial Data Input (SI). CS# must be driven Low for the entire duration of the sequence.

The Chip Erase command sequence: CS# goes low → sending Chip Erase command → CS# goes high. CS# must be driven high after the eighth bit of the command code has been latched in; otherwise the Chip Erase command is not executed. As soon as CS# is driven high, the self-timed Chip Erase cycle (whose duration is t_{CE}) is initiated. While the Chip Erase cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Chip Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. The Chip Erase (CE) command is executed, if no block is protected. The Chip Erase (CE) command is ignored if one or more sectors are protected.

Figure 55 Chip Erase Sequence Diagram (SPI)

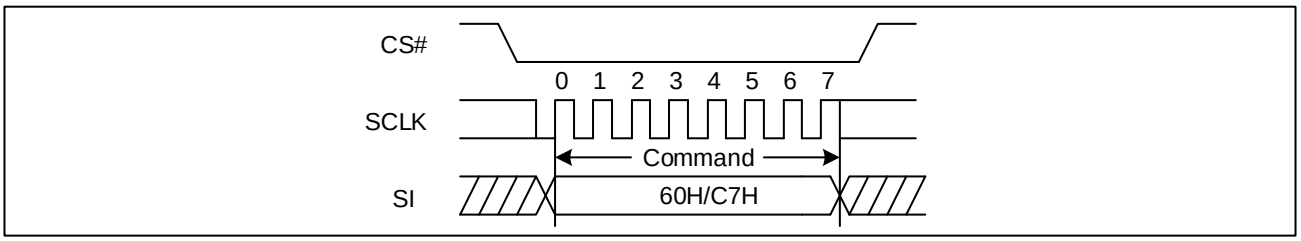
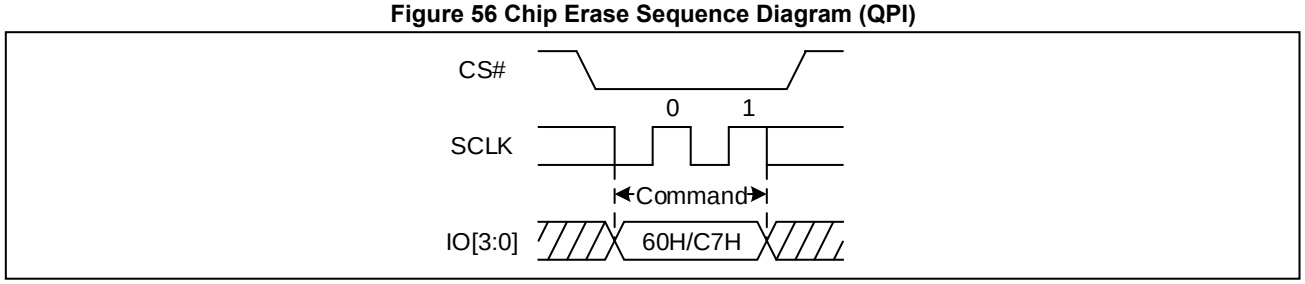


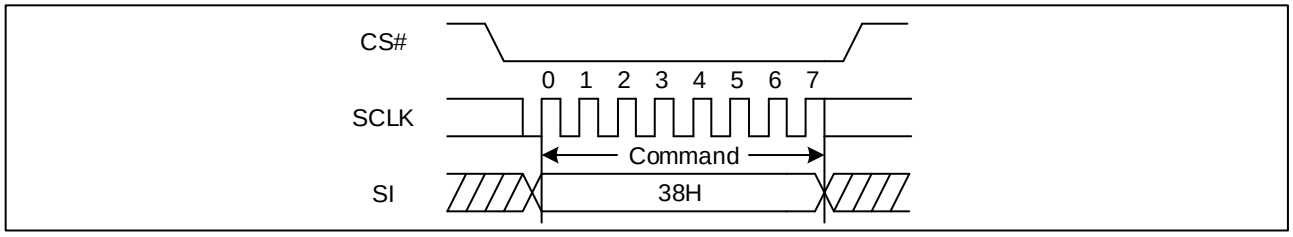
Figure 56 Chip Erase Sequence Diagram (QPI)



8.29 Enable QPI (38h)

The device support both Standard/Quad SPI and QPI mode. The “Enable QPI (38H)” command can switch the device from SPI mode to QPI mode. In order to switch the device to QPI mode, “Enable QPI (38H)” command must be issued. When the device is switched from SPI mode to QPI mode, the existing Write Enable Latch and Program/Erase Suspend status, and the Wrap Length setting will remain unchanged.

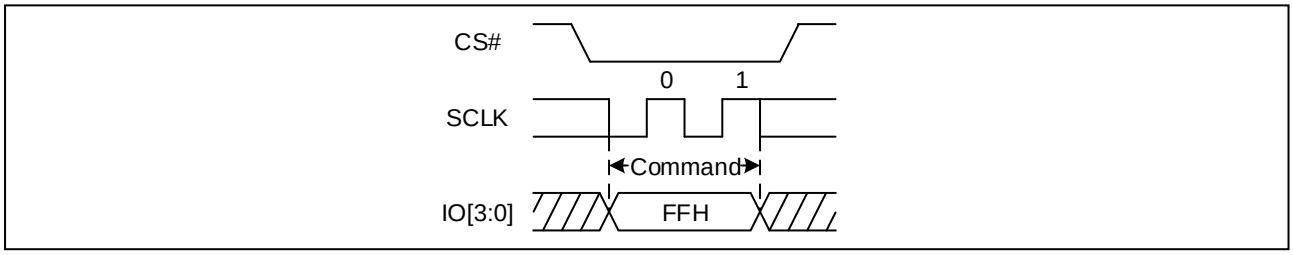
Figure 57 Enable QPI mode command Sequence Diagram



8.30 Disable QPI (FFh)

To exit the QPI mode and return to Standard/Quad SPI mode, the “Disable QPI (FFh)” command must be issued. When the device is switched from QPI mode to SPI mode, the existing Write Enable Latch and Program/Erase Suspend status, and the Wrap Length setting will remain unchanged.

Figure 58 Disable QPI mode command Sequence Diagram



8.31 Deep Power-Down (DP) (B9h)

Executing the Deep Power-Down (DP) command is the only way to put the device in the lowest consumption mode (the Deep Power-Down Mode). It can also be used as an extra software protection mechanism, while the device is not in active use, since in this mode, the device ignores all Write, Program and Erase commands. Driving CS# high deselects the device, and puts the device in the Standby Mode (if there is no internal cycle currently in progress). But this mode is not the Deep Power-Down Mode. The Deep Power-Down Mode can only be entered by executing the Deep Power-Down (DP) command. Once the device has entered the Deep Power-Down Mode, all commands are ignored except the Release from Deep Power-Down (ABh) or Enable Reset (66h) and Reset (99h) commands. These commands can release the device from this mode. The Release from Deep Power-Down command releases the device from deep power down mode.

The Deep Power-Down Mode automatically stops at Power-Down, and the device is in the Standby Mode after Power-Up. The Deep Power-Down command sequence: CS# goes low → sending Deep Power-Down command → CS# goes high. CS# must be driven high after the eighth bit of the command code has been latched in; otherwise the Deep Power-Down (DP) command is not executed. As soon as CS# is driven high, it requires a delay of t_{DP} before the supply current is reduced to I_{CC2} and the Deep Power-Down Mode is entered. Any Deep Power-Down (DP) command, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure 59 Deep Power-Down Sequence Diagram (SPI)

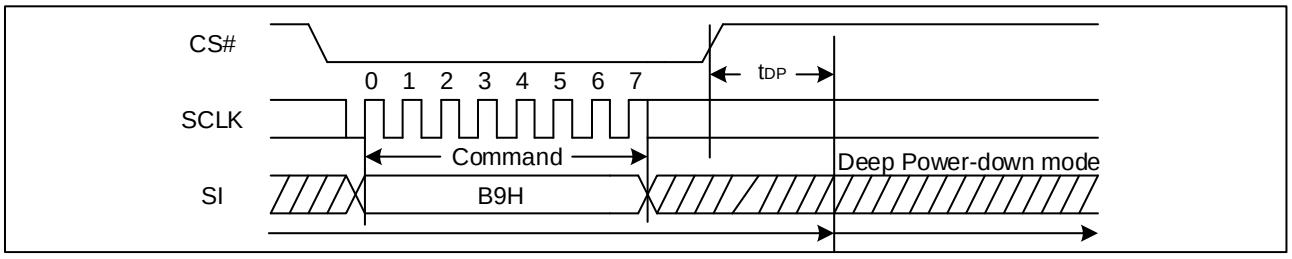
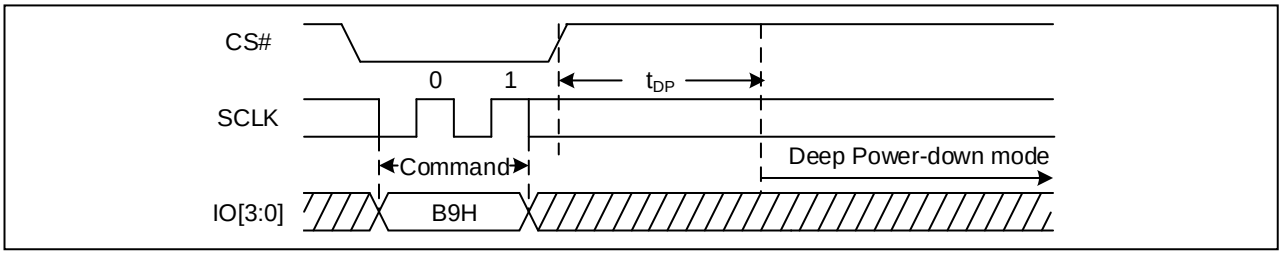


Figure 60 Deep Power-Down Sequence Diagram (QPI)



8.32 Release from Deep Power-Down (ABh)

To release the device from the Power-Down state, the command is issued by driving the CS# pin low, shifting the instruction code “ABh” and driving CS# high. Release from Power-Down will take the time duration of t_{RES1} (See AC Characteristics) before the device will resume normal operation and other command are accepted. The CS# pin must

remain high during the t_{RES1} time duration.

When used to release the device from the Power-Down state, the command is the same as previously described, After this time duration the device will resume normal operation and other command will be accepted. If the Release from Power-Down command is issued while an Erase, Program or Write cycle is in process (when WIP equal 1) the command is ignored and will not have any effects on the current cycle.

Figure 61 Release Power-Down Sequence Diagram (SPI)

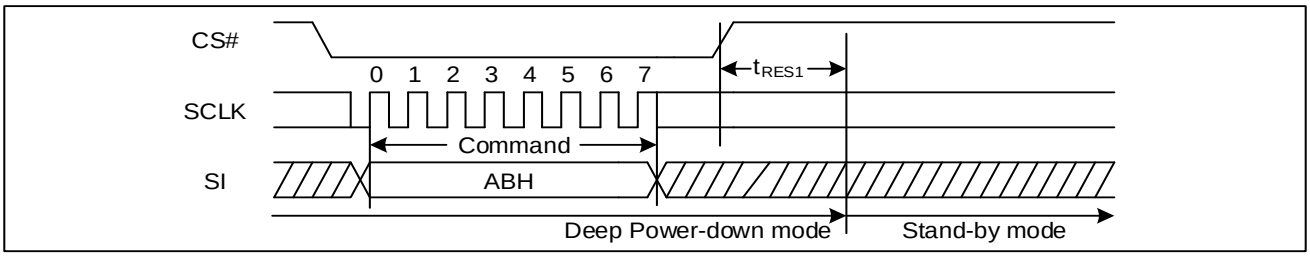


Figure 62 Release Power-Down Sequence Diagram (QPI)

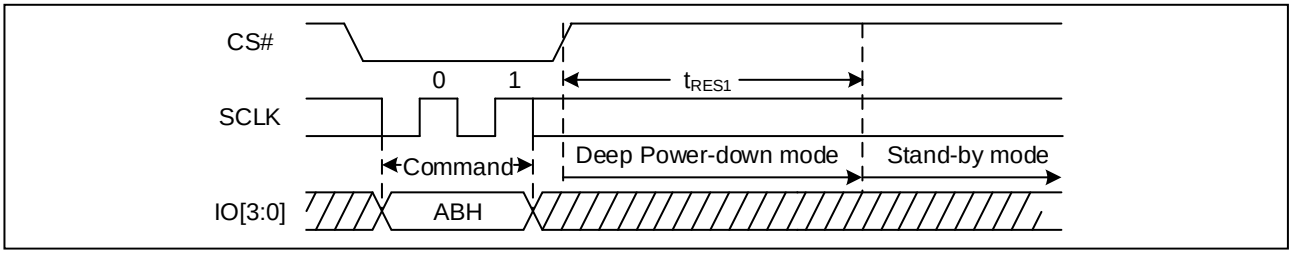


Figure 63. Release Power-Down/Read Device ID Sequence Diagram (SPI)

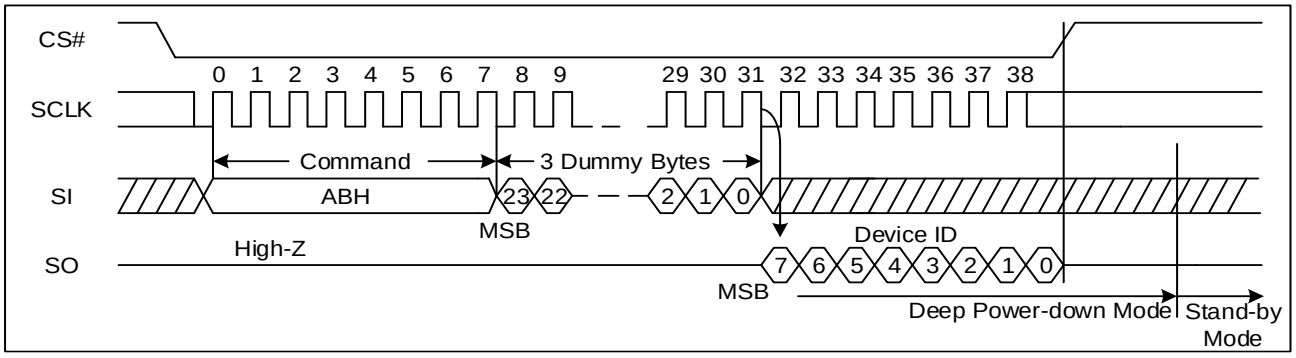
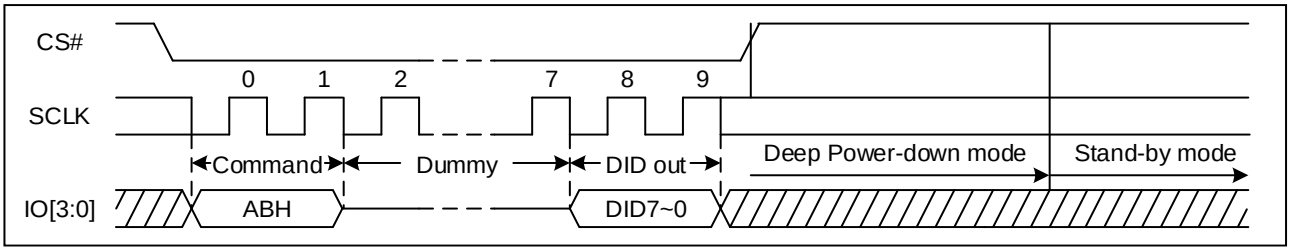


Figure 64. Release Power-Down/Read Device ID Sequence Diagram (QPI)

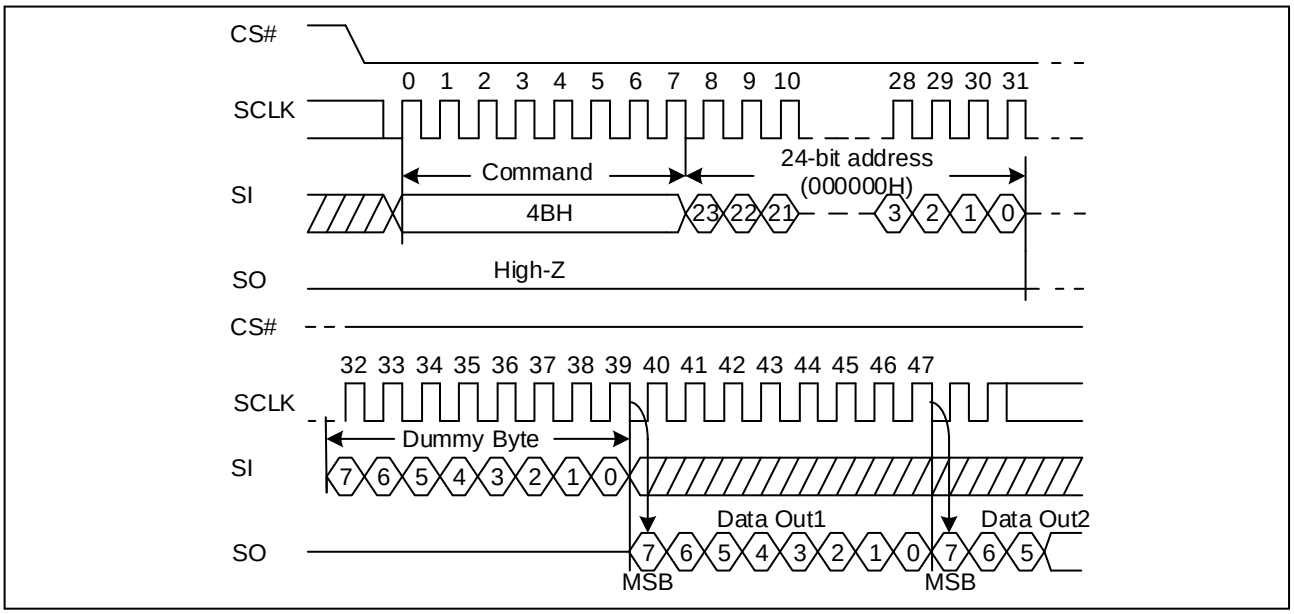


8.33 Read Unique ID (4Bh)

The Read Unique ID command accesses a factory-set read-only 128bit number that is unique to each device. The Unique ID can be used in conjunction with user software methods to help prevent copying or cloning of a system.

The Read Unique ID command sequence: CS# goes low → sending Read Unique ID command → 3-Byte (000000h) or 4-Byte (00000000h) Address →1 Byte Dummy →128bit Unique ID Out →CS# goes high.

Figure 65 Read Unique ID Sequence Diagram (SPI)



Note: The device default is in 24-bit address mode. For 4-Byte mode, the address length becomes 32-bit.

8.34 Read Manufacture ID/ Device ID (REMS) (90h)

The Read Manufacturer/Device ID command is an alternative to the Release from Power-Down / Device ID command that provides both the JEDEC assigned Manufacturer ID and the specific Device ID.

The command is initiated by driving the CS# pin low and shifting the command code “90h” followed by a 24-bit address (A23-A0) of 000000h. After which, the Manufacturer ID and the Device ID are shifted out on the falling edge of SCLK with most significant bit (MSB) first.

Figure 66. Read Manufacture ID/ Device ID Sequence Diagram (SPI)

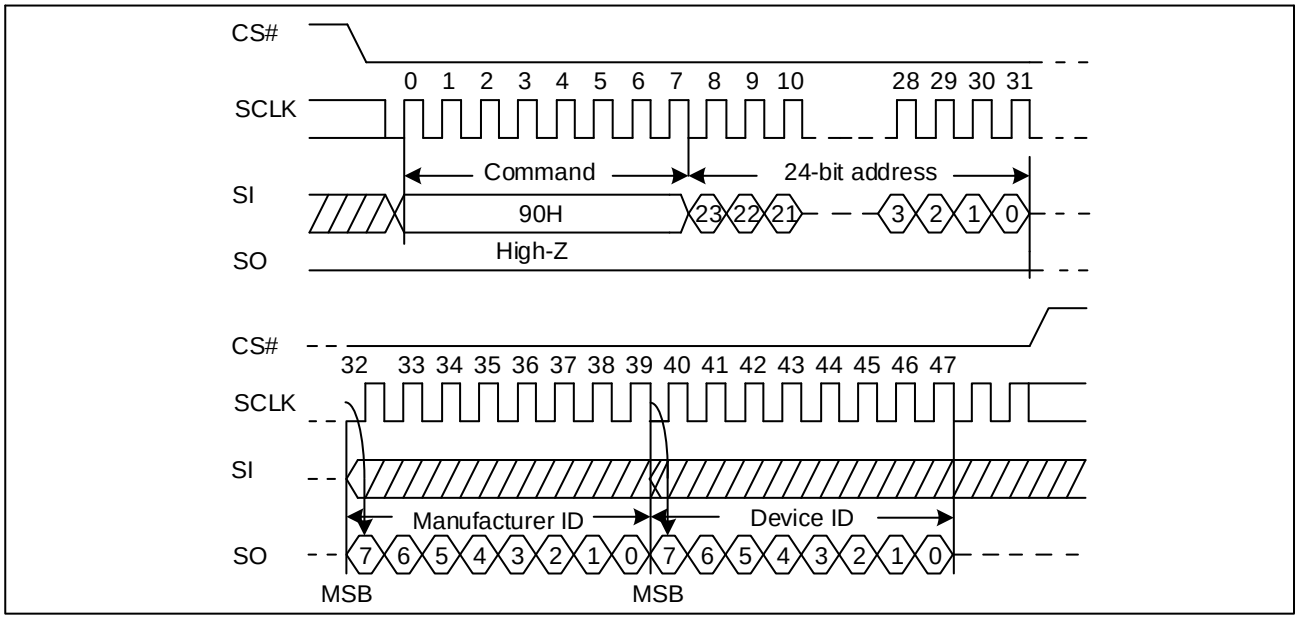
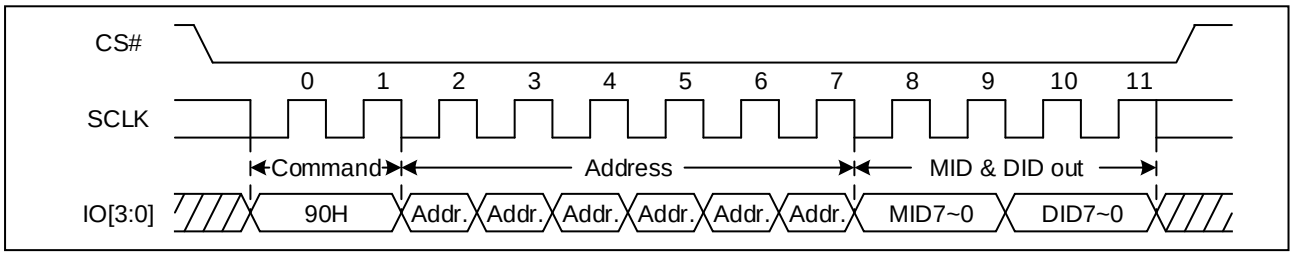


Figure 67. Read Manufacture ID/ Device ID Sequence Diagram (QPI)



8.35 Read Identification (RDID) (9Fh)

The Read Identification (RDID) command allows the 8-bit manufacturer identification to be read, followed by three Bytes of device identification. The device identification indicates the memory type in the first Byte, and the memory capacity of the device in the second Byte. The Read Identification (RDID) command while an Erase or Program cycle is in progress, is not decoded, and has no effect on the cycle that is in progress. The Read Identification (RDID) command should not be issued while the device is in Deep Power-Down Mode.

The device is first selected by driving CS# low. Then, the 8-bit command code for the command is shifted in. This is followed by the 24-bit device identification, stored in the memory. Each bit is shifted out on the falling edge of Serial Clock. The Read Identification (RDID) command is terminated by driving CS# high at any time during data output. When CS# is driven high, the device is in the Standby Mode. Once in the Standby Mode, the device waits to be selected, so that it can receive, decode and execute commands.

Figure 68 Read Identification ID Sequence Diagram (SPI)

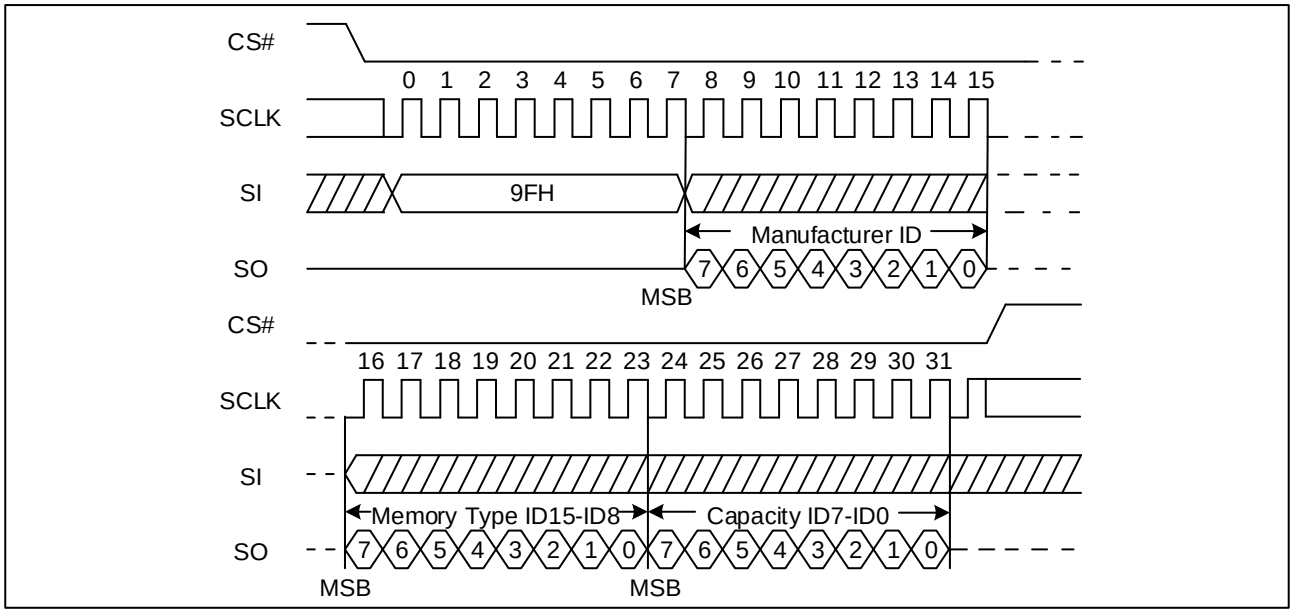
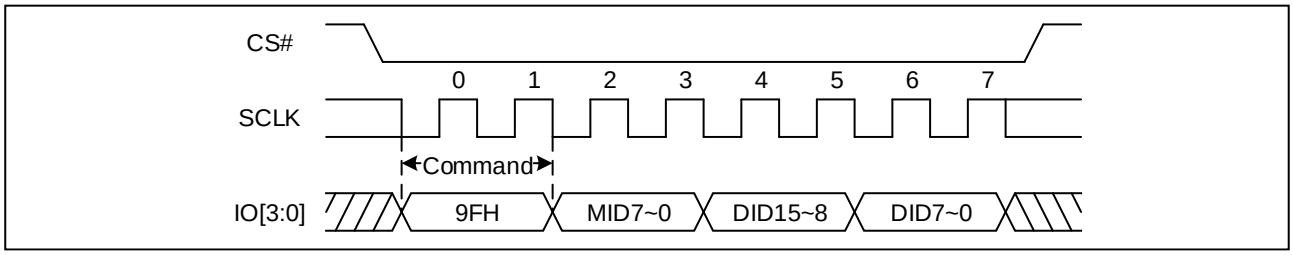


Figure 69 Read Identification ID Sequence Diagram (QPI)



8.36 Program/Erase Suspend (PES) (75h)

The Program/Erase Suspend command “75h”, allows the system to interrupt a page program or sector/block erase operation and then read data from any other sector or block. The Write Status Register command (01h,11h,B1h,AAh,55h) and Erase/Program Security Registers command (44h, 42h) and Erase commands (20h/21h, 52h/5Ch, D8h/DCh, 60h/C7h) and Page Program command (02h/12h,32h/34h) are not allowed during Program suspend. The Write Status Register command (01h, 11h, B1h,AAh,55h) and Erase Security Registers command (44h) and Erase commands (20h/21h, 52h/5Ch, D8h/DCh, 60h/C7h) and 50h, E1h, E3h, E4h, 7Eh, 98h are not allowed during Erase suspend. Program/Erase Suspend is valid only during the page program or sector/block erase operation. A maximum of time of “tsus” (See AC Characteristics) is required to suspend the program/erase operation.

The Program/Erase Suspend command will be accepted by the device only if the SUS1/SUS2 bit in the Status Register equal to 0 and WIP bit equal to 1 while a Page Program or a Sector or Block Erase operation is on-going. If the SUS1/SUS2 bit equal to 1 or WIP bit equal to 0, the Suspend command will be ignored by the device. The WIP bit will be cleared from 1 to 0 within “tsus” and the SUS1/SUS2 bit will be set from 0 to 1 immediately after Program/Erase Suspend. A power-off during the suspend period will reset the device and release the suspend state

Figure 70 Program/Erase Suspend Sequence Diagram (SPI)

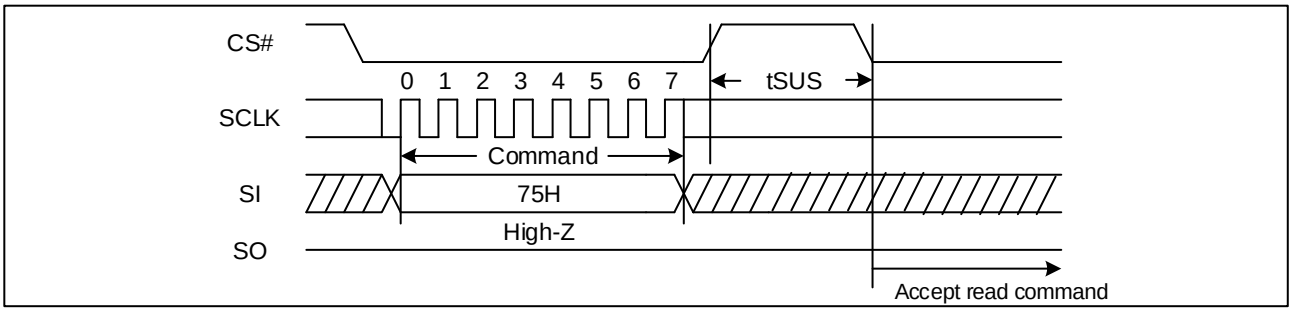
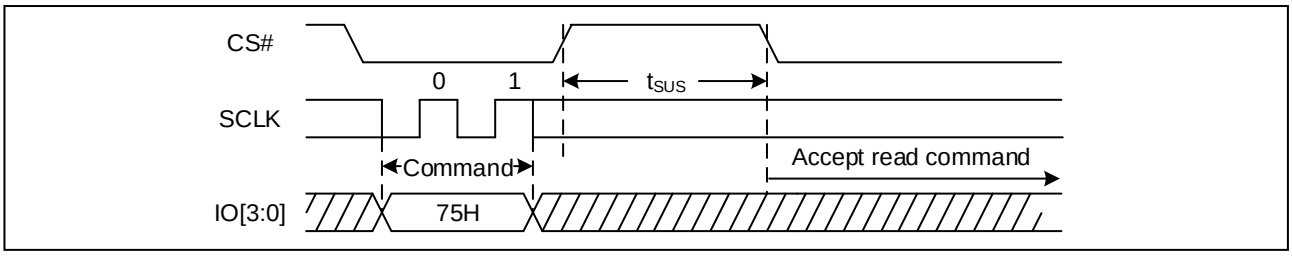


Figure 71 Program/Erase Suspend Sequence Diagram (QPI)



8.37 Program/Erase Resume (PER) (7Ah)

The Program/Erase Resume command must be written to resume the program or sector/block erase operation after a Program/Erase Suspend command. The Program/Erase Resume command will be accepted by the device only if the SUS2/SUS1 bit equal to 1 and the WIP bit equal to 0. After issued the SUS2/SUS1 bit in the status register will be cleared from 1 to 0 immediately, the WIP bit will be set from 0 to 1 within 200ns and the Sector or Block will complete the erase operation or the page will complete the program operation. The Program/Erase Resume command will be ignored unless a Program/Erase Suspend is active.

Figure 72 Program/Erase Resume Sequence Diagram

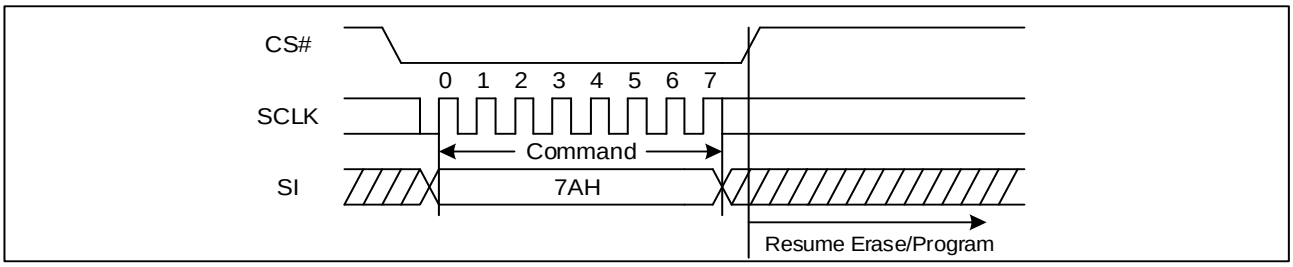
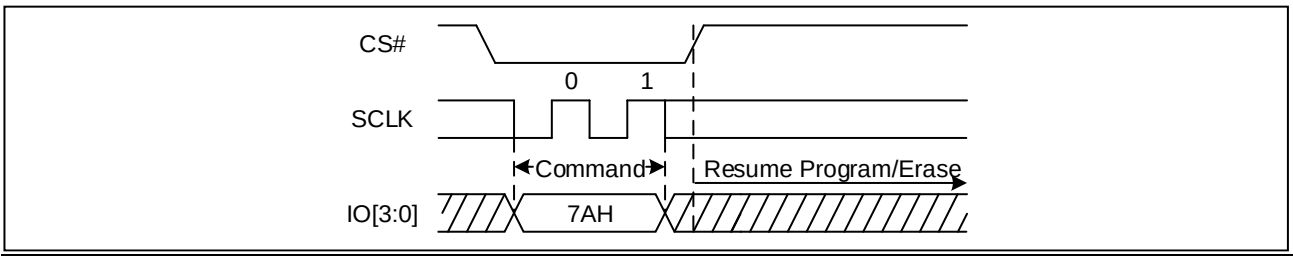


Figure 73 Program/Erase Resume Sequence Diagram (QPI)



8.38 Erase Security Registers (44h)

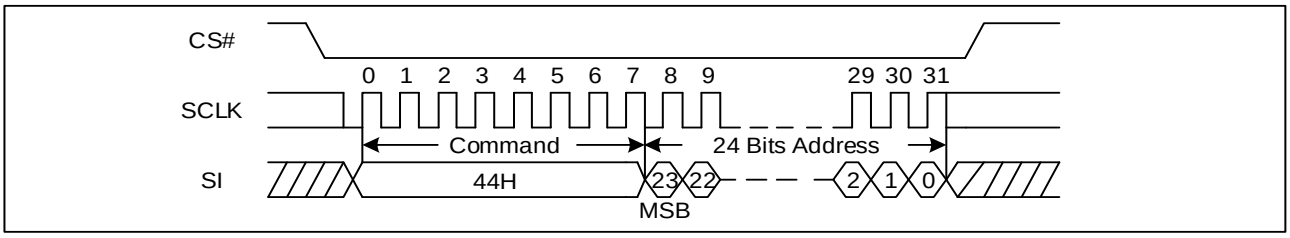
The GD25LR256F provides 4K-Byte Security Registers which can be erased and programmed individually. These registers may be used by the system manufacturers to store security and other important information separately from the main memory array.

The Erase Security Registers command is similar to Sector/Block Erase command. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit.

The Erase Security Registers command sequence: CS# goes low → sending Erase Security Registers command → CS# goes high. CS# must be driven high after the eighth bit of the last address Byte has been latched in; otherwise the Erase Security Registers command is not executed. As soon as CS# is driven high, the self-timed Erase Security Registers cycle (whose duration is t_{SE}) is initiated. While the Erase Security Registers cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Erase Security Registers cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. The Security Registers Lock Bit in the Status Register can be used to OTP protect the security registers. Once the bit is set to 1, the Security Registers will be permanently locked; the Erase Security Registers command will be ignored.

Address	A23-16	A15-12	A11-0
Security Register #1	00H	0 0 0 1	Don't care
Security Register #2	00H	0 0 1 0	Don't care
Security Register #3	00H	0 0 1 1	Don't care

Figure 74 Erase Security Registers command Sequence Diagram (SPI)



Note: The device default is in 24-bit address mode. For 4-Byte mode, the address length becomes 32-bit.

8.39 Program Security Registers (42h)

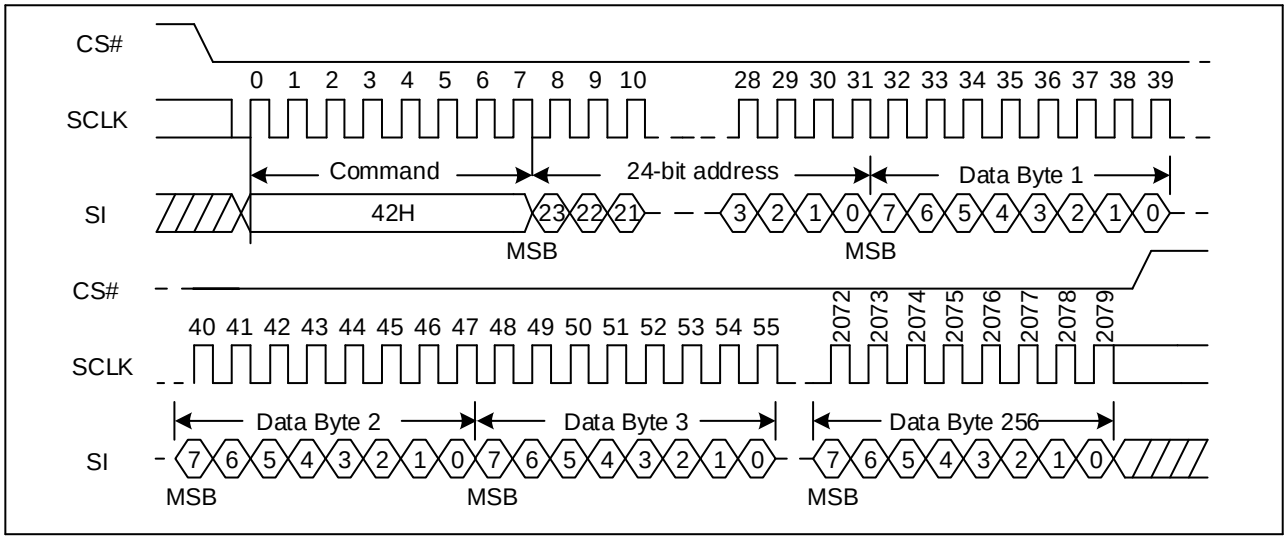
The Program Security Registers command is similar to the Page Program command. Each security register contains 16 pages content. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Program Security Registers command. The Program Security Registers command is entered by driving CS# Low, followed by the command code (42h), three address Bytes and at least one data Byte on SI. As soon as CS# is driven high, the self-timed Program Security Registers cycle (whose duration is tPP) is initiated. While the Program Security Registers cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Program Security Registers cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

If the Security Registers Lock Bit is set to 1, the Security Registers will be permanently locked. Program Security Registers command will be ignored.

Address	A23-16	A15-12	A11-8	A7-0
Security Register #1	00H	0 0 0 1	Page Address	Byte Address
Security Register #2	00H	0 0 1 0	Page Address	Byte Address

Security Register #3	00H	0 0 1 1	Page Address	Byte Address

Figure 75 Program Security Registers command Sequence Diagram (SPI)



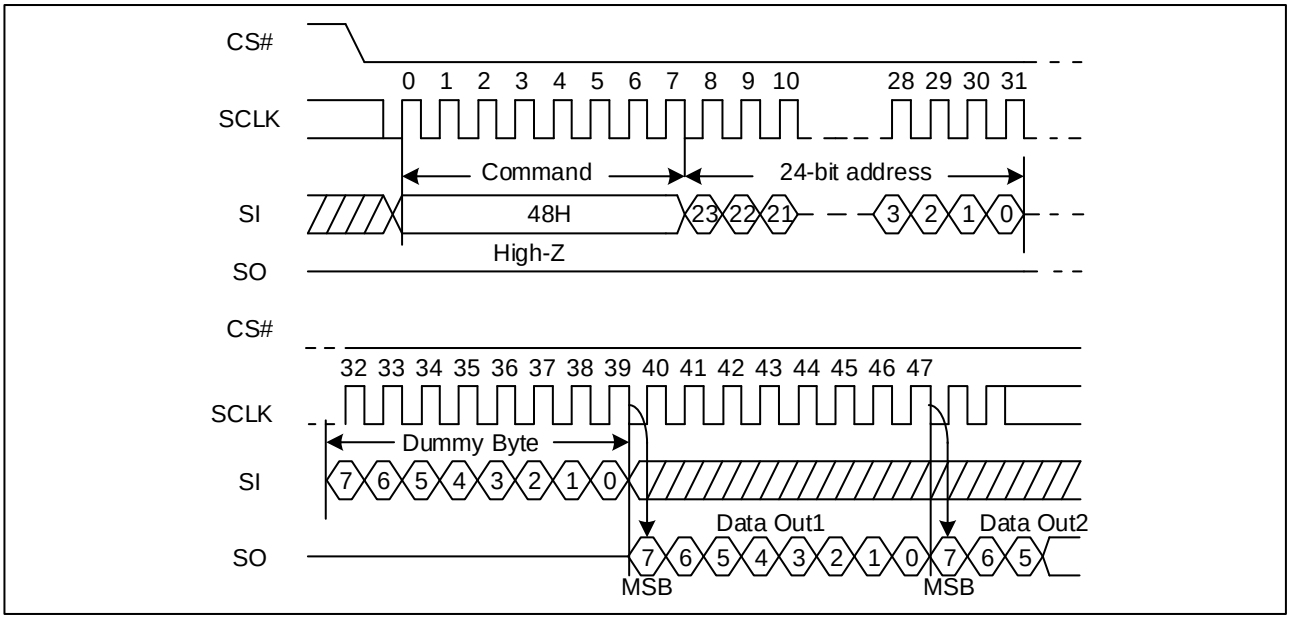
Note: The device default is in 24-bit address mode. For 4-Byte mode, the address length becomes 32-bit.

8.40 Read Security Registers (48h)

The Read Security Registers command is similar to Fast Read command. The command is followed by a 3-Byte or 4-Byte address (A23-A0 or A31-A0) and a dummy Byte, and each bit is latched-in on the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, and each bit is shifted out, at a Max frequency f_C, on the falling edge of SCLK. The first Byte addressed can be at any location. The address is automatically incremented to the next higher address after each Byte of data is shifted out. Once the A11-A0 address reaches the last Byte of the register (Byte FFFH), it will reset to 000H, the command is completed by driving CS# high.

Address	A23-16	A15-12	A11-8	A7-0
Security Register #1	00H	0 0 0 1	Page Address	Byte Address
Security Register #2	00H	0 0 1 0	Page Address	Byte Address
Security Register #3	00H	0 0 1 1	Page Address	Byte Address

Figure 76 Read Security Registers command Sequence Diagram (SPI)



Note: The device default is in 24-bit address mode. For 4-Byte mode, the address length becomes 32-bit.

8.41 Global Block/Sector Lock (7Eh) or Unlock (98h)

All Block/Sector Lock bits can be set to 1 by the Global Block/Sector Lock command, or can set to 0 by the Global Block/Sector Unlock command.

The Global Block/Sector Lock command (7Eh) sequence: CS# goes low →SI: Sending Global Block/Sector Lock command→ CS# goes high.

The Global Block/Sector Unlock command (98h) sequence: CS# goes low →SI: Sending Global Block/Sector Unlock command→ CS# goes high.

Figure 77 Global Block/Sector Lock Sequence Diagram (SPI)

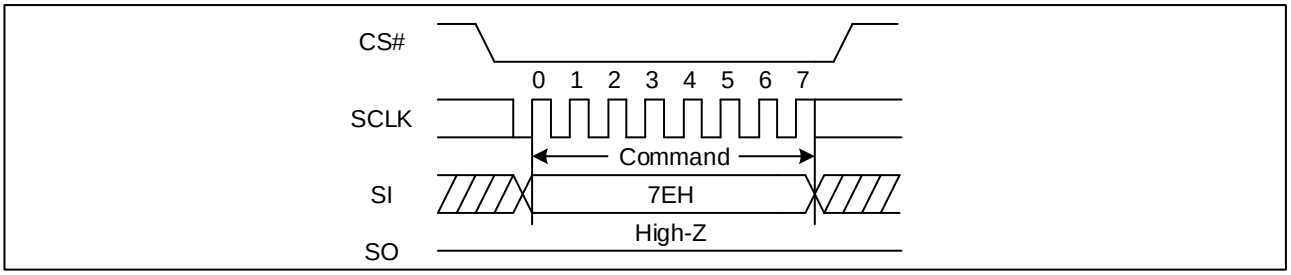


Figure 78 Global Block/Sector Lock Sequence Diagram (QPI)

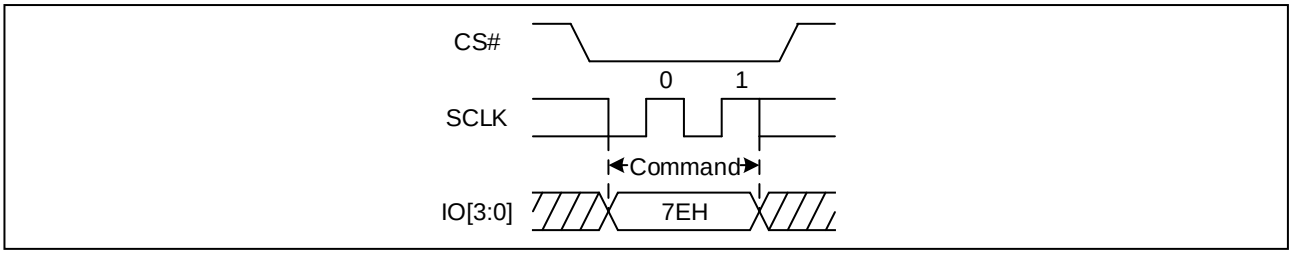


Figure 79 Global Block/Sector Unlock Sequence Diagram (SPI)

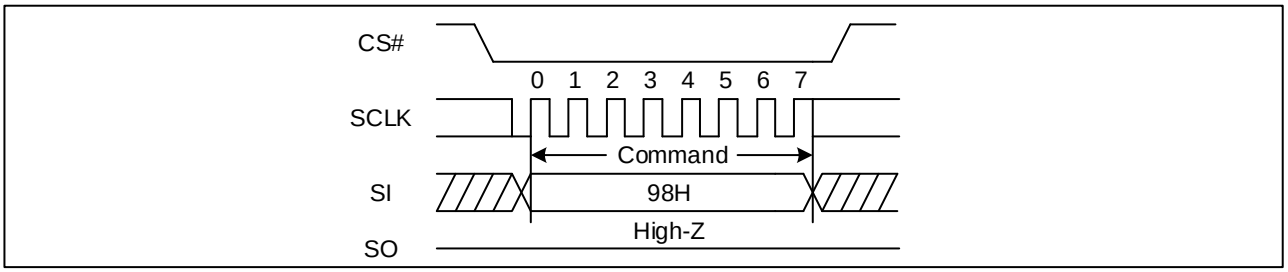
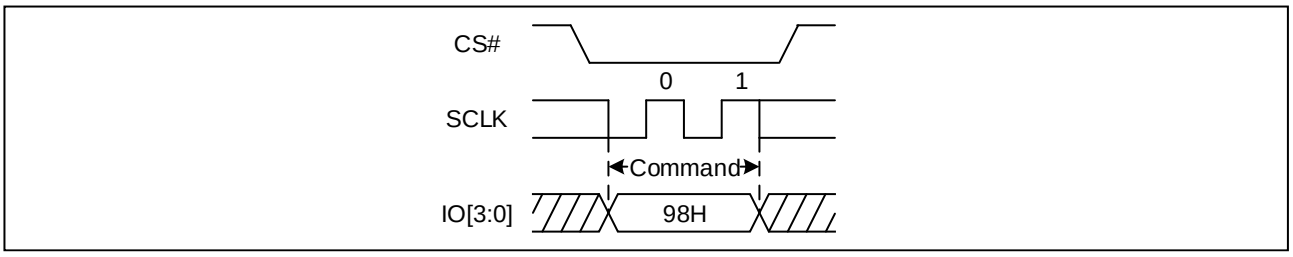


Figure 80 Global Block/Sector Unlock Sequence Diagram (QPI)

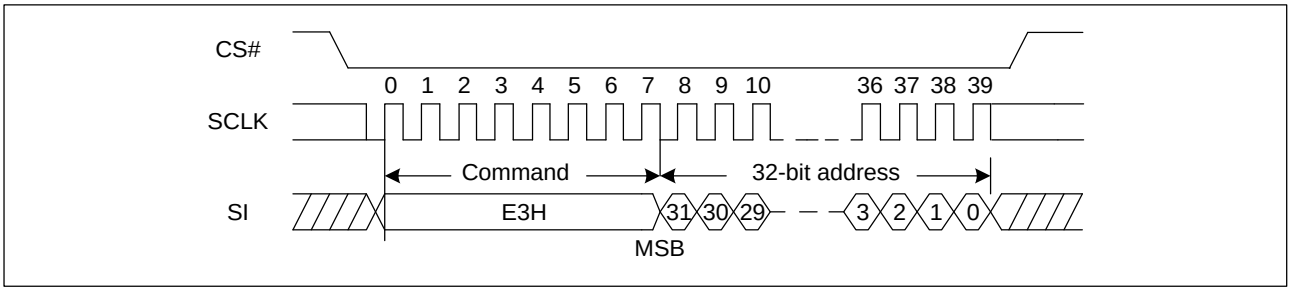


8.42 Set Nonvolatile Lock Register (E3h)

Before the Set NL Register and Clear All NL Registers commands are accepted besides the WEL bit= 1 requirement. The Set NL Register command sets the non-volatile NL Register block protection to 'FFh' of the target address within the range of either a sector or a block. When NL Register is '00h' (default), the corresponding sector or block is unprotected or unlocked state; and it can be set to 'FFh' to lock (protect) so the corresponding memory sector or block are protected against program or erase. Please check the NL Registers section for more information on the NL Registers mapping across the full memory.

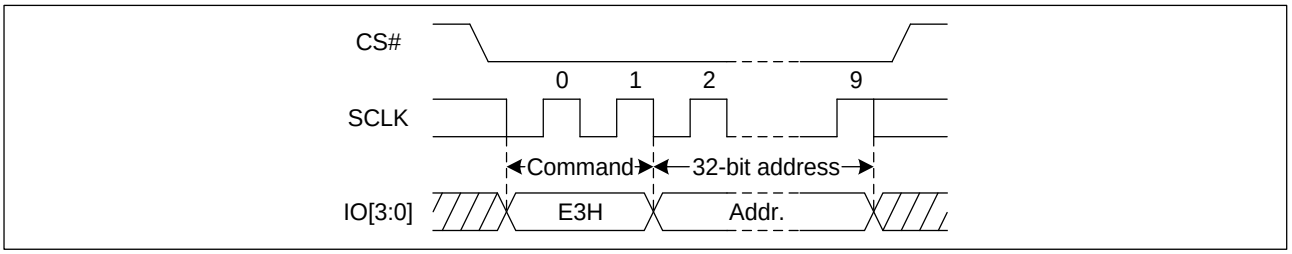
A Write Enable (WREN) command must be executed prior to initiating the Set NL Register command. The Set NL Register command is initiated by driving CS# low followed by latching in command opcode E3H and the 32-Bit Address on every rising edge of SCLK. For SPI sequence, CS# must be driven high after the least significant address bit input's SCLK (least significant address nibble input's SCLK for QPI), otherwise the Set NL Register command is not executed. As soon as CS# is driven high, the self-timed NL Register setting cycle (whose duration is tNLP) is initiated. The Write In Progress (WIP) bit is 1 during the self-timed NL Register setting cycle, and transition to 0 upon completion. When the cycle is completed, the Write Enable Latch (WEL) is reset. The NL Register corresponding to the input address used in the Set NL Register command sequence is also set to 'FFh' (protected).

Figure 81 Set NL Register Sequence Diagram (SPI)



Note: The Program NL Register command uses only 32-bit address input in either 3-Byte or 4-Byte Address mode.

Figure 82 Set NL Register Sequence Diagram (QPI)



Note: The Set NL Register command uses only 32-bit address input in either 3-Byte or 4-Byte Address mode.

8.43 Clear All Nonvolatile Lock Registers (E4h)

The Clear All NL Registers command clears the whole non-volatile NL Register to '00H' that unlocks all the sector/block protection. When a NL Register is 'FFh', the corresponding sector or block is protected or locked state; Each NL Register is set to 'FFh' individually, however they can only be cleared as a group (all NL Registers) that can unlock (unprotect) the full memory opening the memory for either program or erase operation.

A Write Enable (WREN) command must be executed prior to initiating the Clear All NL Registers command. The Clear All NL Registers command is initiated by driving CS# low followed by latching in command opcode E4H on every rising edge of SCLK. For SPI, CS# must be driven high after the 8th SCLK (after 2nd CLK for QPI), otherwise the Clear All NL Registers

command is not executed. As soon as CS# is driven high, the self-timed NL Registers clearing cycle (whose duration is tCNLR) is initiated. The Write In Progress (WIP) bit is 1 during the self-timed NL Registers clearing cycle, and transition to 0 upon completion. When the cycle is completed, the Write Enable Latch (WEL) is reset. All the NL Registers are cleared to '00H' (unprotected) after Clear All NL Registers completion.

Figure 83 Clear All NL Registers Sequence Diagram (SPI)

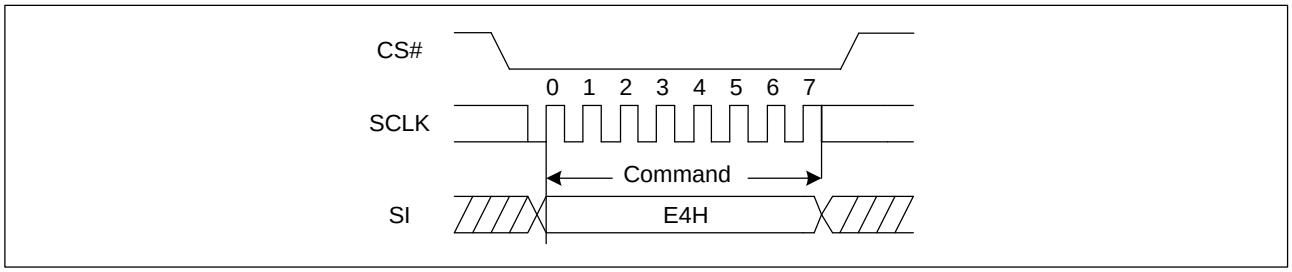
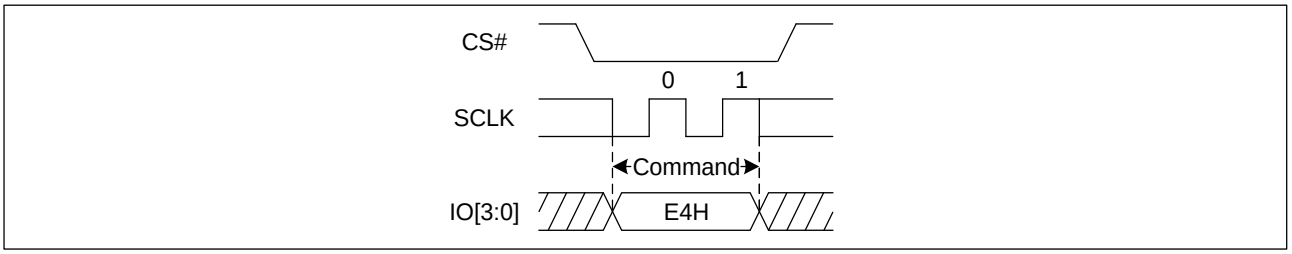


Figure 84 Clear All NL Registers Sequence Diagram (QPI)

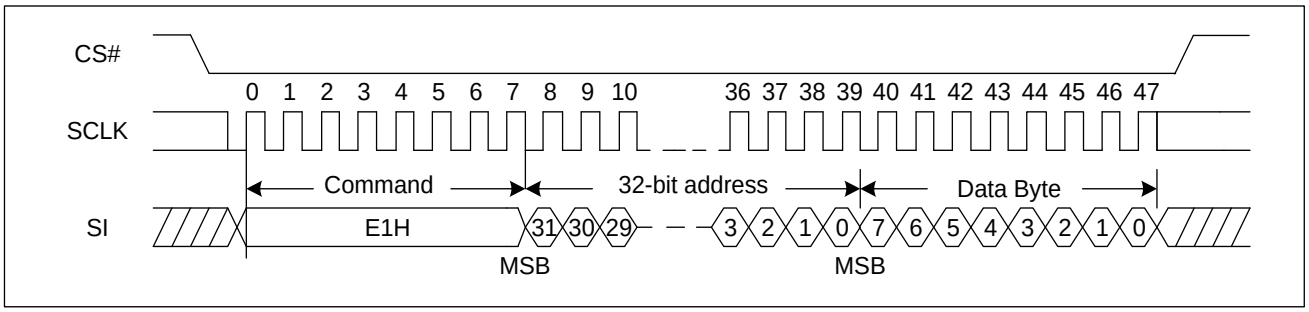


8.44 Write Volatile Lock Register (E1h)

The Write VL Register command writes to the VL Register either a 'FFh' data to protect or a '00h' data to unprotect a corresponding individual sector or block address. A byte size data input is used to do the write. If any other data other than 00h or FFh (ie. 01h, 02h… FEh) is used in the Write VL Register instruction data input sequence, the instruction is ignored. When a sector or block is protected, the corresponding VL Register is 'FFh' and when a sector or block is unprotected, the corresponding VL Register is '00H'. Please check the VL Register section for more information on the VL Registers mapping across the full memory.

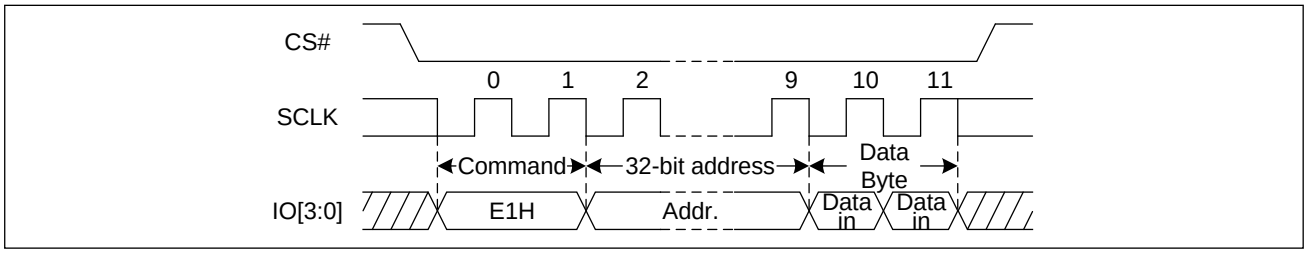
A Write Enable (WREN) command must be first executed before sending the Write VL Register command. Once properly setup, Write VL Register instruction is initiated by driving CS# low followed by sending the command opcode E1h, the 32-Bit Address targeting the sector or block to be protected or unprotected, and the byte of data to be written (either 00H or FFh will only be accepted). The command, address, and data input are latched in on the rising edge of the SCLK. As soon as CS# is driven high, the Write to VL Register cycle is initiated instantaneously (no wait time). When the cycle is completed, the Write Enable Latch (WEL) is reset.

Figure 85 Write VL Register Sequence Diagram (SPI)



Note: The Write VL Register command uses only 32-bit address input in either 3-Byte or 4-Byte Address mode.

Figure 86 Write VL Register Sequence Diagram (QPI)

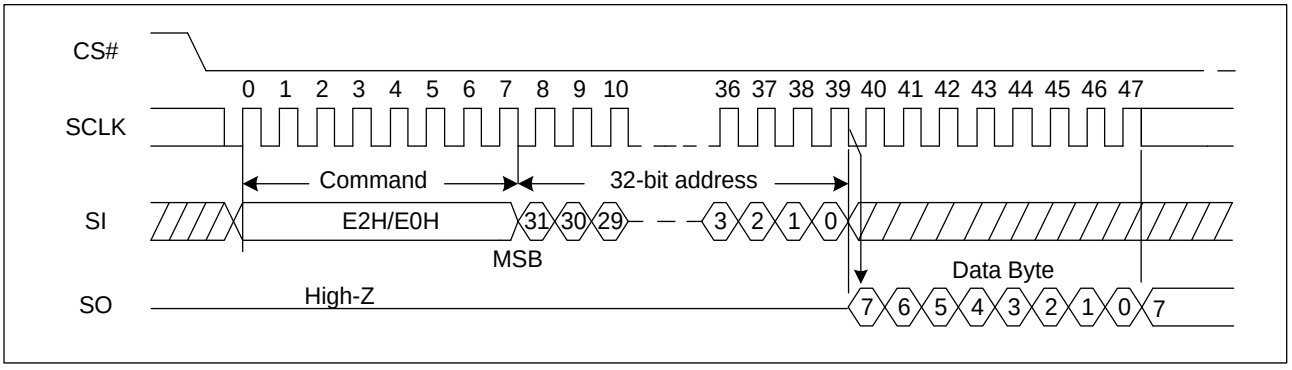


Note: The Write VL Register command uses only 32-bit address input in either 3-Byte or 4-Byte Address mode.

8.45 Read Nonvolatile Lock Register (E2h) / Read Volatile Lock Register(E0h)

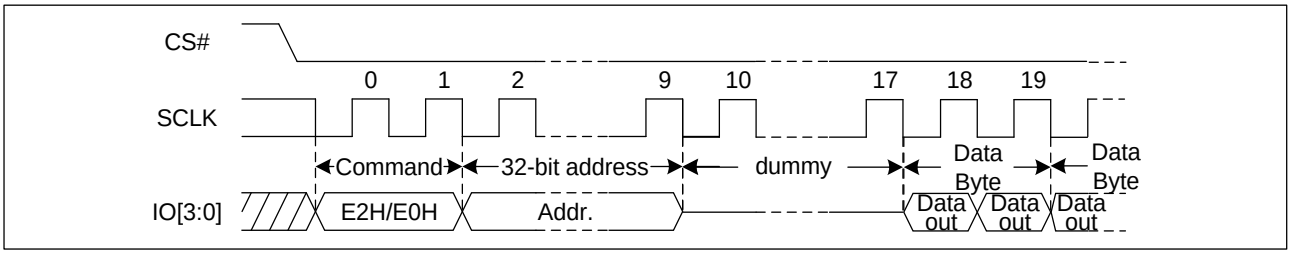
The Read NL Register (E2h)/Read VL Register (E0h) command sequence reads the NL/VL Register data of the corresponding sector or block used in the input address. The input command sequence is as follows: command E2h/E0h opcode and followed by a 4-Byte address (A31-A0). The input sequence uses the rising edge of SCLK to latch-in data. After the last input address SCLK falling edge, the NL/VL Register byte data follows as data output. Read NL Register/VL Register is ignored if executed in the middle of an Erase, Program or Write cycle.

Figure 87 Read NL Register/VL Register Sequence Diagram (SPI)



Note: The Read NL Register (E2h) / VL Register(E0H) command uses only 32-bit address input in either 3-Byte or 4-Byte Address mode.

Figure 88 Read NL Register/VL Register Sequence (QPI)



Note: The Read NL Register(E2h) / VL Register (E0H) command uses only 32-bit address input in either 3-Byte or 4-Byte Address mode.

8.46 Enable Reset (66h) and Reset (99h)

If the Reset command is accepted, any on-going internal operation will be terminated and the device will return to its default power-on state and lose all the current volatile settings, such as Volatile Status Register bits, Write Enable Latch status (WEL), Program/Erase Suspend status, Read Parameter setting (P7-P0), Deep Power Down Mode, Continuous Read Mode bit setting (M7-M0) and Wrap Bit Setting (W6-W4).

The “Enable Reset (66h)” and the “Reset (99h)” commands can be issued in either SPI or QPI mode. The “Enable Reset (66h)” and “Reset (99h)” command sequence as follow: CS# goes low → Sending Enable Reset command → CS# goes high → CS# goes low → Sending Reset command → CS# goes high. Once the Reset command is accepted by the device, the device will take approximately t_{RST}/t_{RST_E} to reset. During this period, no command will be accepted. Data corruption may happen if there is an on-going or suspended internal Erase or Program operation when Reset command sequence is accepted by the device. It is recommended to check the WIP bit and the SUS1/SUS2 bit in Status Register before issuing the Reset command sequence.

Figure 89 Enable Reset and Reset command Sequence Diagram (SPI)

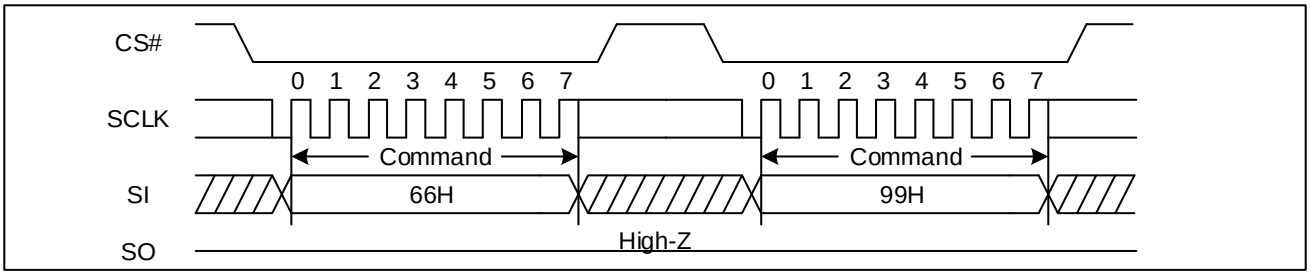
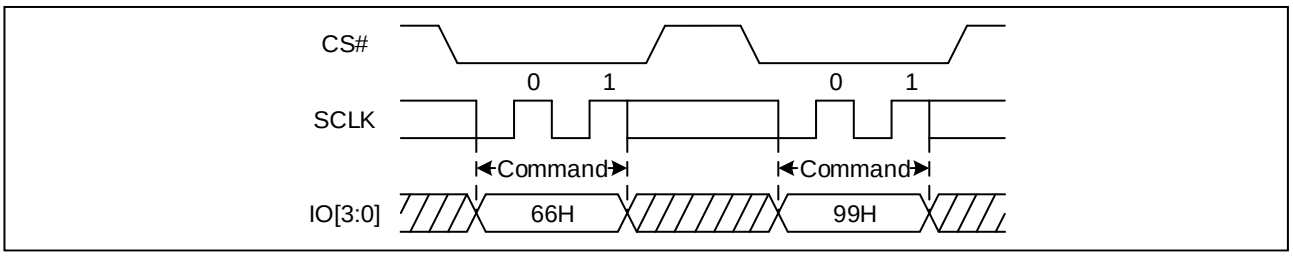


Figure 90 Enable Reset and Reset command Sequence Diagram (QPI)



8.47 Read Serial Flash Discoverable Parameter (5Ah)

The Serial Flash Discoverable Parameter (SFDP) standard provides a consistent method of describing the functional and feature capabilities of serial flash devices in a standard set of internal parameter tables. These parameter tables can be interrogated by host system software to enable adjustments needed to accommodate divergent features from multiple

vendors. The concept is similar to the one found in the Introduction of JEDEC Standard, JESD68 on CFI. SFDP is a standard of JEDEC Standard No.216B.

Figure 91 Read Serial Flash Discoverable Parameter command Sequence Diagram (SPI)

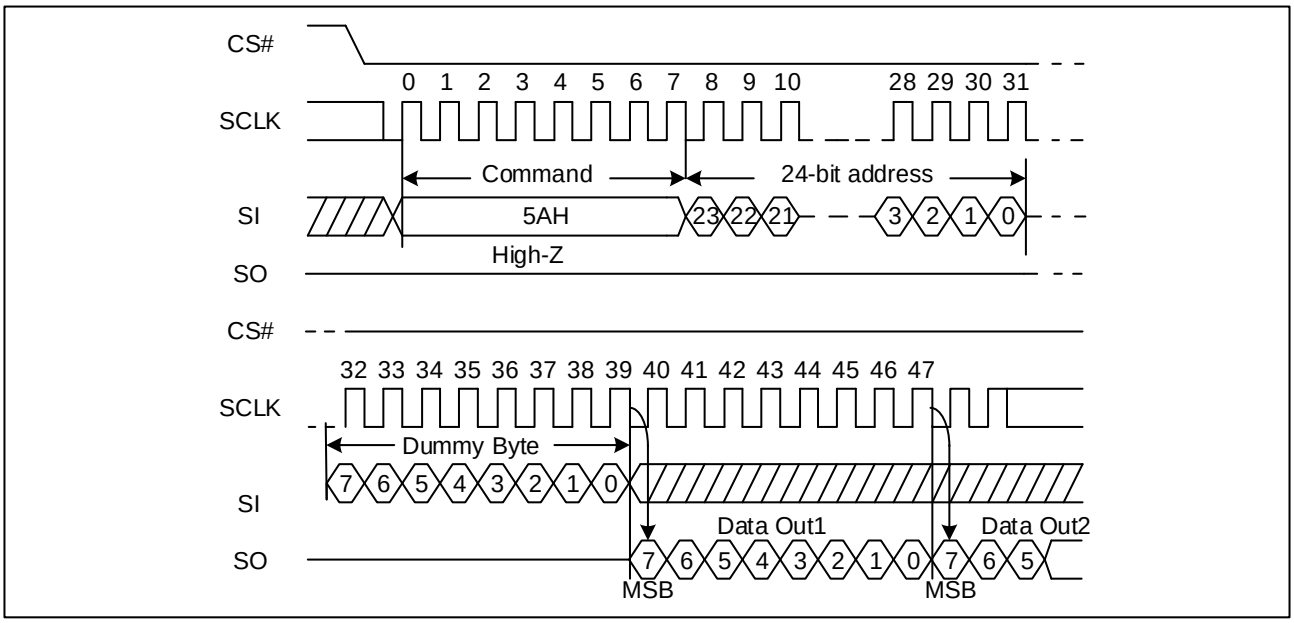


Figure 92 Read Serial Flash Discoverable Parameter command Sequence Diagram (QPI)

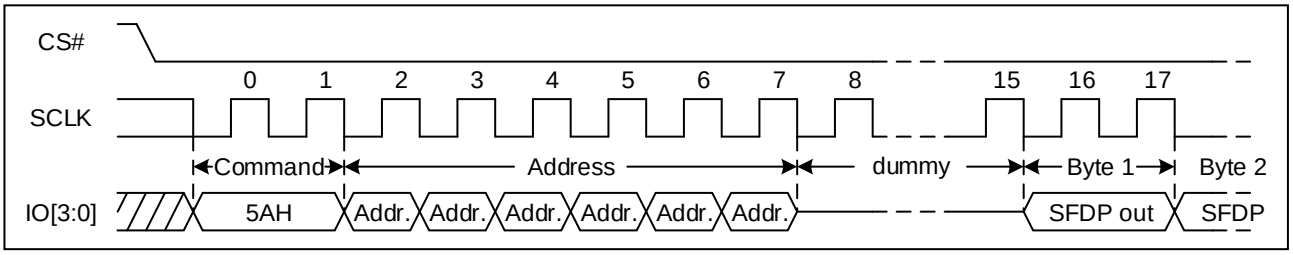


Table 19 Signature and Parameter Identification Data Values (Please contact GigaDevice for details)

9 RPMC COMMANDS DESCRIPTION

Table 20. Replay Protected Monotonic Counter (RPMC) Commands

Function	Opcode Phase 8 bits	Payload Phase Max 512 Bits		Comment
		Byte#	Field Description	
Command: Write Root Key Register	OP1	1 2 3 4-35 36-63	CmdType[7:0] = 00H CounterAddr[7:0] = 8 Bits Reserved[7:0] = 8 Bits RootKey[255:0] = 256 Bits TruncatedSign[223:0] = 224 Bits	OP1 + Payload phase driven by host controller. Root Key Register is written only once.
Command: Update HMAC Key Register	OP1	1 2 3 4-7 8-39	CmdType[7:0]= 01H CounterAddr[7:0]= 8 Bits Reserved[7:0] = 8 Bits KeyData[31:0] = 32 Bits, Signature[255:0] = 256 Bits	OP1 + Payload phase is Issued by host controller on every power up to initialize HMAC Key Register.
Command: Increment Monotonic Counter	OP1	1 2 3 4-7 8-39	CmdType[7:0] = 02H CounterAddr[7:0] = 8 Bits Reserved[7:0] = 8 Bits CounterData[31:0] = 32 Bits, Signature[255:0] = 256 Bits	OP1 + Payload Phase is Issued by host controller during runtime to increment the counter.
Command: Request Monotonic Counter	OP1	1 2 3 4-15 16-47	CmdType[7:0] = 03H CounterAddr[7:0] = 8 Bits Reserved[7:0] = 8 Bits Tag [95:0] = 96 Bits Signature[255:0] = 256 Bits	OP1 + Payload Phase is Issued by host controller during runtime to request counter data
Command: Read Data	OP2	2 3-14 15-18 19-50	ExtendedStatus[7:0] = 8 Bits Tag[95:0] = 96 Bits CounterData[31:0] = 32 Bits Signature[255:0] = 256 Bits	OP2 is issued by Host Controller generally after an OP1. SPI Flash device responds with the Payload phase to return Extended Status and counter data.

All individual fields are Byte wide fields. For a multi-byte field, Most Significant Byte is issued first; Least Significant Byte is issued last. Within a Byte, Most Significant Bit is issued first; Least Significant Bit is issued last. CmdType is always the first byte issued after OP1 commands. OP2 delay is the same as Fast Read Command delay which is 8 dummy bits.

Table 21. OP1 and OP2 are defined for 1-1-1 mode.

Byte #	0	1	2	3	4	5	6	…	..	..
Name	OP1	CmdType	Counter Address	As defined in the table above						
Name	OP2	8 Dummy clocks	Extended Status[7:0]	As defined in the table above						

After an OP1 command is received, the SPI Flash will indicate status busy indication using either the status register or extended status register as defined below.

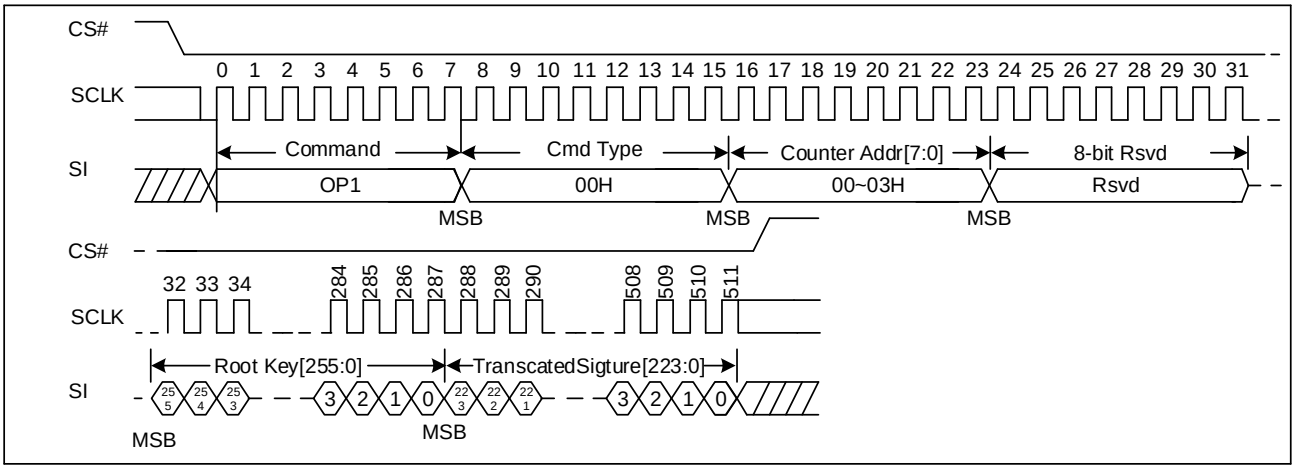
Table 22. Extended Status Register Definition

Extended Status[7:0]	Applicable CmdType(s)	Description
00000000	-	Power On State (OP2 issued directly after power-up).
10000000	00,01,02,03	This status is set on successful completion (no errors) of OP1 command.
0xxxxxx1	00,01,02,03,04-0FF	This bit is set to 1, when device is busy executing OP1 command. It is reset to 0 when OP1 command execution is done.
0xxxxx1x	00,01	This bit is set only when the correct payload size is received. When cmdtype = 0, this error bit must be set on Root Key Register Overwrite or Counter Address out of range or Truncated Signature mis-match error. For cmdtype = 01 this bit is set when the corresponding monotonic counter is uninitialized
0xxxx1xx	00,01,02,03	This bit is set on Signature Mismatch, Counter Address out of range when correct payload size is received; or Cmdtype is out of range; or incorrect payload size is received.
0xxx1xxx	02,03	This bit is set on HMAC Key Register or monotonic counter uninitialized on previous OP1 command when correct payload size is received
0xx1xxxx	02	This bit is set on Counter Data Mismatch on previous increment when correct payload size is received
0x1xxxxx	-	Fatal Error. It is set when no valid counter is found after initialization.
Current value		Extended status register will not be updated until first 8 bits of OP1 is received. The correct error type is reflected for any OP1 operation that exceeds a minimum of 16 clocks with active chip-select.

9.1 Command: Write Root Key Register

This command is used to initialize the Root Key Register corresponding to the received Counter Address with the received Root Key. It is suggested to be used in an OEM manufacturing environment when the SPI Flash Controller and SPI Flash are powered together for the first time.

Figure 93. Write Root Key Register Sequence Diagram



Truncated signature field is the same as least significant 224 bits of HMAC-SHA-256 based signature computed based on

received input parameters:

- HMAC message[31:0] = (OpCode[7:0], CmdType[7:0], CounterAddr[7:0], Reserved[7:0])
- HMAC Key[255:0] = Root_Key[255:0]

If Root Key != 256'HFF..FF then this command can be executed one time. If the received transaction is error free SPI Flash device successfully executes the command and posts "successful completion" extended status.

Root Key Register Write with root key is = 256'HFF…FF can be used as a temporary key.

If the received transaction has errors the SPI Flash does not execute the transaction and posts the corresponding error in extended status.

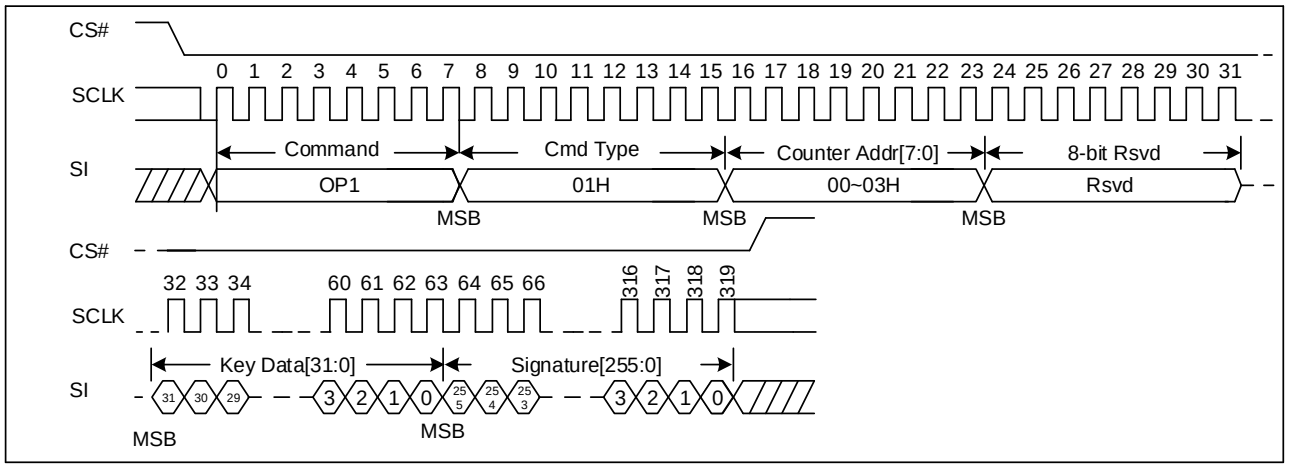
Table 23. Expected Extended Status [7:0] results

Extended Status[7:0]	Applicable CmdType(s)	Description
10000000	00	Successful completion
0xxxxxx1	00	If Busy_Polling_Method bit in SFDP table is zero, then this bit must be set to 1, when device is busy executing command. It is reset to 0 when OP1 command execution is done. If Busy_Polling_Method bit in SFDP table is one, then this bit is ignored by the controller.
0xxxxx1x	00	This bit is only set when correct payload size is received. It is set on Root Key Register Overwrite or Counter Address is out of range or when there is a truncated signature mismatch error
0xxxx1xx	00	This bit is set when incorrect payload size is received.

9.2 Command: Update HMAC Key Register

This command is used by the SPI Flash Controller to update the HMAC-Key register corresponding to the received Counter Address with a new HMAC key calculated based on received input. This command must be issued on every power cycle event on the interface. The HMAC key storage is volatile.

Figure 94. Update HMAC Key Register Sequence Diagram



Signature matches the HMAC-SHA-256 based signature computed based on received input parameters. This command performs two HMAC-SHA-256 operations.

- HMAC-SHA-256 Operation 1 Output = HMAC_Storage[255:0]
  - HMAC Message[31:0] = KeyData[31:0]
  - HMAC Key[255:0] = Root_Key_Register[CounterAddr][255:0]

- HMAC-SHA-256 Operation 2 Output = HMAC-SHA-256 based signature[255:0]
  - HMAC message[63:0] = (OpCode[7:0], CmdType[7:0].CounterAddr[7:0].Reserved[7:0], KeyData[31:0])
  - HMAC Key[255:0] = HMAC_Storage[255:0]

If the received transaction is error free SPI Flash device successfully executes the command and posts "successful completion" extended status.

If the received transaction has errors the SPI Flash does not execute the transaction and posts the corresponding error in extended status.

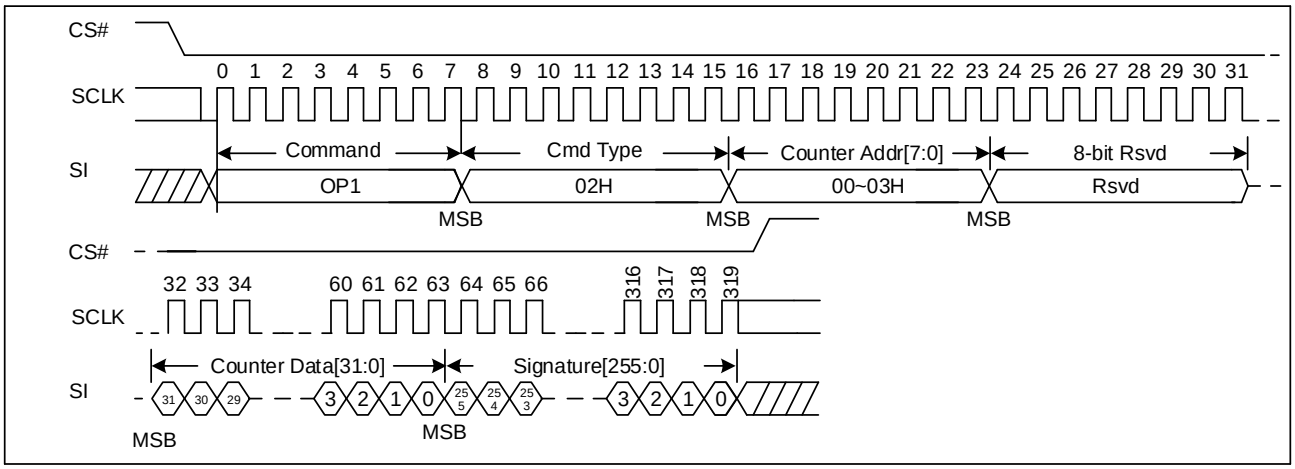
Table 24. Expected Extended Status [7:0] results

Extended Status[7:0]	Applicable CmdType(s)	Description
10000000	01	This status is set on successful completion (no errors) of OP1 command.
0xxxxxx1	01	This bit is set to 1, when device is busy executing OP1 command. It is reset to 0 when OP1 command execution is done.
0xxxxx1x	01	This bit is set only when the correct payload size is received. This bit is set when the corresponding monotonic counter is uninitialized
0xxxx1xx	01	This bit is set on Signature Mismatch, Counter Address out of range when correct payload size is received; or incorrect payload size is received.

9.3 Command: Increment Monotonic Counter

This command is used by the SPI Flash Controller to increment the Monotonic counter by 1 inside the SPI Flash Device.

Figure 95. Increment Monotonic Counter Sequence Diagram



The requested Signature matches the HMAC-SHA-256 based signature computed based on received input parameters. The received Counter Data matches the current value of the counter read from the SPI Flash.

- HMAC Message[63:0] = (OpCode[7:0], CmdType[7:0]. CounterAddr[7:0]. Reserved[7:0], CounterData[31:0])
- HMAC Key[255:0] = HMAC_Key_Register [Counter_Addreess][255:0]

If the received transaction is error free SPI Flash device successfully executes the command and posts "successful completion" extended status. If the received transaction has errors the SPI Flash does not execute the transaction and posts the corresponding error in extended status.

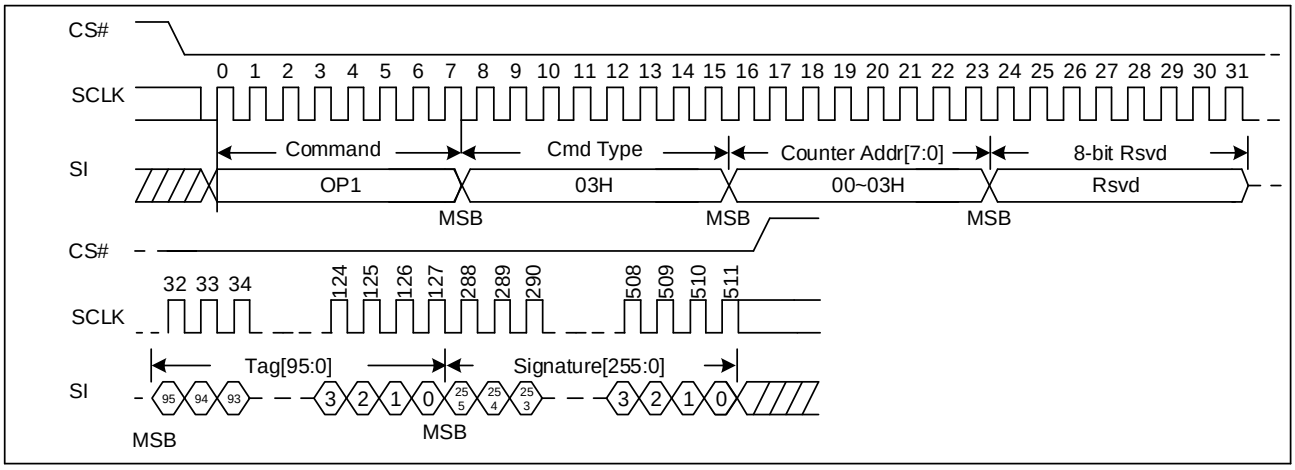
Table 25. Expected Extended Status [7:0] results

Extended Status[7:0]	Applicable CmdType(s)	Description
10000000	02	This status is set on successful completion (no errors) of OP1 command.
0xxxxxx1	02	This bit is set to 1, when device is busy executing OP1 command. It is reset to 0 when OP1 command execution is done.
0xxxx1xx	02	This bit is set on Signature Mismatch, Counter Address out of range when correct payload size is received; or incorrect payload size is received.
0xxx1xxx	02	This bit is set only when the correct payload size is received. This bit must be set on HMAC Key Register or Monotonic Counter is uninitialized on previous OP1 command.
0xx1xxxx	02	This bit is set only when the correct payload size is received. The bit must be set when the received counter data filed does not match the actual counter value read from the SPI Flash device.

9.4 Command: Request Monotonic Counter

This command is used by the SPI Flash Controller to request the Monotonic counter value inside the SPI Flash Device.

Figure 96. Request Monotonic Counter Sequence Diagram



The requested Signature matches the HMAC-SHA-256 based signature computed based on received input parameters.

- HMAC Message[127:0] = (OpCode[7:0], CmdType[7:0]. CounterAddr[7:0]. Reserved[7:0], Tag[95:0])
- HMAC Key[255:0] = HMAC_Key_Register[Counter_Addreess][255:0]

If the received transaction is error free SPI Flash device successfully executes the command and posts “successful completion” extended status. If the received transaction has errors the SPI Flash does not execute the transaction and posts the corresponding error in extended status.

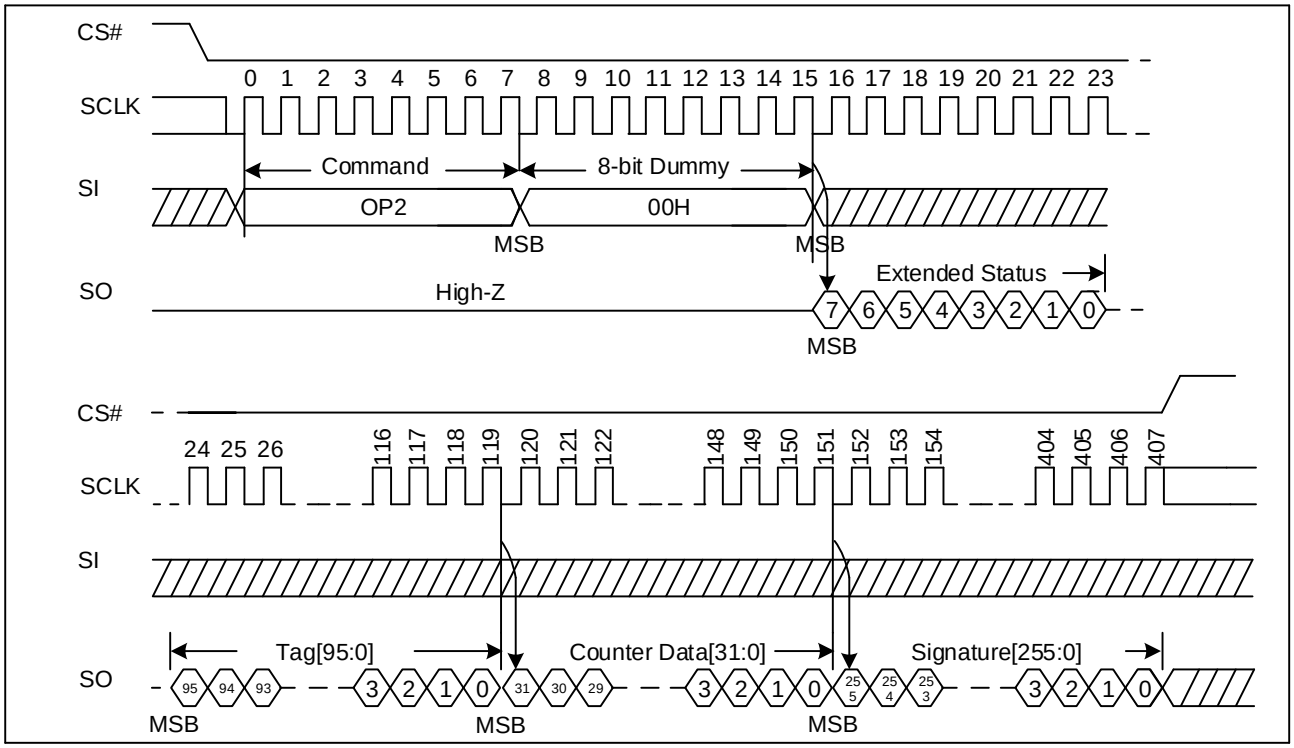
Table 26. Expected Extended Status [7:0] results

Extended Status[7:0]	Applicable CmdType(s)	Description
10000000	03	This status is set on successful completion (no errors) of OP1 command.
0xxxxxx1	03	This bit is set to 1, when device is busy executing OP1 command. It is reset to 0 when OP1 command execution is done.
0xxxx1xx	03	This bit is set on Signature Mismatch, Counter Address out of range when correct payload size is received; or Cmdtype is out of range; or incorrect payload size is received.
0xxx1xxx	03	This bit is set only when the correct payload size is received. This bit must be set on HMAC Key Register or Monotonic Counter is uninitialized on previous OP1 command.

9.5 Command: Read Data

This command is used by the SPI Flash Controller to read extended status from any previously issued OP1 command. In addition if previous OP1 command is Request Monotonic Counter and if SPI Flash returns successful completion extended status then it returns valid values in the Tag, Counter Data and Signature field. Otherwise the values returned in Tag, Counter and Signature field are invalid. The controller may abort the read prematurely prior to completely reading the entire payload. This may occur when the controller wants to simply read the extended status or when is observes an error being returned in the extended status field. The controller may also continue reading past the defined payload size of 49 bytes. Since this is an error condition, the SPI Flash may return any data past the defined payload size. The controller must ignore the data.

Figure 97. Read Data Sequence Diagram



If previous OP1 command is Request Monotonic Counter and if SPI Flash returns successful completion extended status then it returns valid values in the Tag, Counter Data and Signature field.It calculates HMAC-SHA-256 signatures based on following parameters.

- HMAC Message[127:0] = Tag [95:0], Counter_Data_Read[31:0]
- HMAC Key[255:0] = HMAC_Key_Register[Counter_Address][255:0]

Table 27. Extended Status Register Definition

Extended Status[7:0]	Applicable CmdType(s)	Description
00000000	-	Power On State (OP2 issued directly after power-up).
10000000	00, 01, 02, 03	This status is set on successful completion (no errors) of OP1 command.
0xxxxxx1	00, 01, 02, 03	This bit is set to 1, when device is busy executing OP1 command. It is reset to 0 when OP1 command execution is done.
0xxxxx1x	00, 01	This bit is set only when the correct payload size is received. When cmdtype = 0, this error bit must be set on Root Key Register Overwrite or Counter Address out of range or Truncated Signature mis-match error. For remaining cmdtype = 1 this bit is set when the corresponding monotonic counter is uninitialized
0xxxx1xx	01, 02, 03	This bit is set on Signature Mismatch, Counter Address out of range when correct payload size is received; or Cmdtype is out of range; or incorrect payload size is received.
0xxx1xxx	02, 03	This bit is set on HMAC Key Register or Monotonic Counter uninitialized on previous OP1 command when correct payload size is received
0xx1xxxx	02	This bit is set on Counter Data Mismatch on previous increment when correct payload size is received
0x1xxxxx	-	Fatal Error. It is set when no valid counter is found after initialization.
Current value	-	Extended status register will not be updated until first 8 bits of OP1 is received. The correct error type is reflected for any OP1 operation that exceeds a minimum of 16 clocks with active chip-select.

9.6 Operations Allowed/Disallowed During RPMC Operation

In the deep power down state OP1, OP2 commands are ignored until the part comes out of deep power down state.

WREN state does not affect the OP1 command execution inside the SPI Flash.

Suspend operation can be used to execute high-priority reads from the flash device while a long-latency operation is underway. However, OP1 is not recommended when the flash device is in WIP or suspended state.

In the table below, OP1 state is defined as the time starting with a transaction with OP1 op-code sent to the device and ending when the device clears the extended status busy bit. During OP1 state if a suspend transaction is received, the SPI Flash will ignore the suspend command and continue with the execution of the current OP1 command as described in the table below. P/E state is defined as the time starting with a transaction with write or erase op-code sent to the device and ending when the device clears

the status busy bit. P/E Suspended State starts when the device sets the program suspend status done bit after receiving a program suspend op-code. During P/E State and P/E Suspended State, OP1 is also allowed but not recommended

The table below shows all operation support in each state.

Table 28. RPMC Operation

Operation	OP1 state	P/E state	P/E Suspended State
Suspend	Ignored	Yes-> P/E Suspended State(not chip erase or write status operation) No ->remain P/E state (chip erase or write status operation)	No
Resume	Ignored	No	Yes -> P/E state
All reads except Read status	Yes	No	Yes
All writes/erases	Yes	No	No
OP1	No	Yes but not recommended	Yes but not recommended
Write status	Yes	No	No
OP2	Yes->OP1 busy state (when extended status busy is 1) ->OP1 done state (when extended status busy is 0)	Yes. Will indicate the status associated with the OP1 operation.	Yes. Will indicate the status associated with the OP1 operation
Read status	Yes. Will indicate the busy state associated with the subsequent transaction issued to the SPI Flash.	Yes. Will indicate the busy state associated with the subsequent transaction issued to the SPI Flash.	Yes. Will indicate the busy state associated with the subsequent transaction issued to the SPI Flash.

10 ELECTRICAL CHARACTERISTICS

10.1 Power-On Timing

Figure 98 Power-on Timing

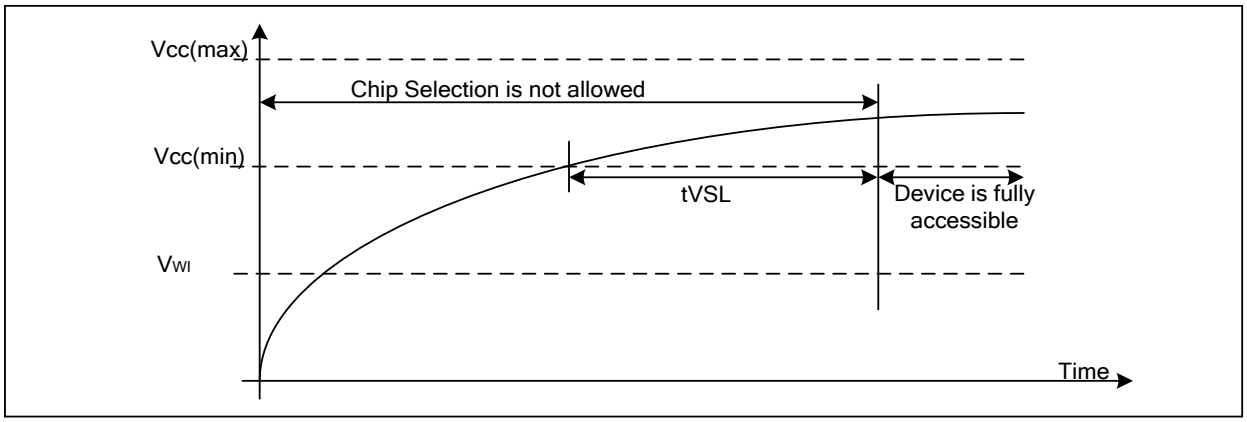


Table 29 Power-Up Timing and Write Inhibit Threshold

Symbol	Parameter	Min.	Max.	Unit
tVSL	VCC (min.) to device operation	1.5		ms
VWI	Write Inhibit Voltage	1	1.5	V

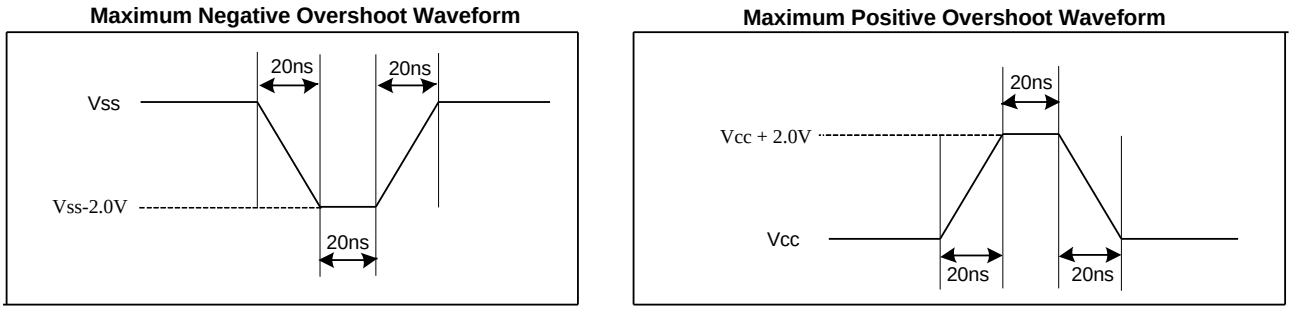
10.2 Initial Delivery State

The device is delivered with the memory array erased: all bits are set to 1 (each Byte contains FFh). The Status Register contains 00H, except that QE bit (S9) are set to 1.

10.3 Absolute Maximum Ratings

Parameter	Value	Unit
Ambient Operating Temperature (T_A)	-40 to 85 -40 to 105 -40 to 125	℃
Storage Temperature	-65 to 150	℃
Transient Input/Output Voltage (note: overshoot)	-2.0 to VCC+2.0	V
Applied Input/Output Voltage	-0.6 to VCC+0.4	V
VCC	-0.6 to 2.5	V

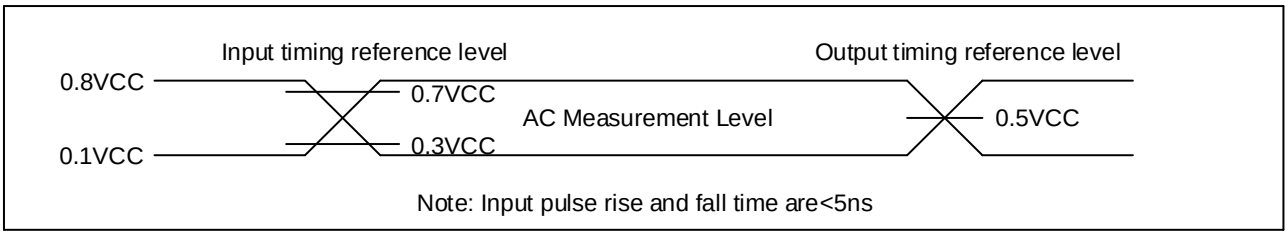
Figure 99. Input Test Waveform and Measurement Level



10.4 Capacitance Measurement Conditions

Symbol	Parameter	Min	Typ.	Max	Unit	Conditions
CIN	Input Capacitance			12	pF	VIN=0V
COUT	Output Capacitance			16	pF	VOUT=0V
C_L	Load Capacitance		30		pF	
	Input Rise And Fall time			5	ns	
	Input Pulse Voltage	0.1VCC to 0.8VCC			V	
	Input Timing Reference Voltage	0.3VCC to 0.7VCC			V	
	Output Timing Reference Voltage	0.5VCC			V	

Figure 100. Absolute Maximum Ratings Diagram



10.5 DC Characteristics

(T_A = -40℃~85℃, VCC=1.65~2.0V)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit.
I_{LI}	Input Leakage Current				±4	μA
I_{LO}	Output Leakage Current				±4	μA
I_{CC1}	Standby Current	CS#=VCC, VIN=VCC or VSS		16	90	μA
I_{CC2}	Deep Power-Down Current	CS#=VCC, VIN=VCC or VSS		3	40	μA
I_{CC3}	Operating Current (Read)	CLK=0.1VCC / 0.9VCC at 104MHz, Q=Open(x4 I/O)		12	20	mA
I_{CC4}	Operating Current (PP)	CS#=VCC		12	20	mA
I_{CC5}	Operating Current (WRSR)	CS#=VCC		12	20	mA
I_{CC6}	Operating Current (SE)	CS#=VCC		12	20	mA
I_{CC7}	Operating Current (BE)	CS#=VCC		12	20	mA
I_{CC8}	Operating Current (CE)	CS#=VCC		12	20	mA
V_{IL}	Input Low Voltage		-0.5		0.3VCC	V
V_{IH}	Input High Voltage		0.7VCC		VCC+0.4	V
V_{OL}	Output Low Voltage	I_{OL} = 100μA			0.2	V
V_{OH}	Output High Voltage	I_{OH} = -100μA	VCC-0.2			V

Notes:

1. Typical value at T_A = 25℃, VCC = 1.8V.
2. Value guaranteed by design and/or characterization, not 100% tested in production.

(T_A = -40℃~105℃, VCC=1.65~2.0V)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit.
I_{LI}	Input Leakage Current				±4	μA
I_{LO}	Output Leakage Current				±4	μA
I_{CC1}	Standby Current	CS#=VCC, VIN=VCC or VSS		16	180	μA
I_{CC2}	Deep Power-Down Current	CS#=VCC, VIN=VCC or VSS		3	70	μA
I_{CC3}	Operating Current (Read)	CLK=0.1VCC / 0.9VCC at 104MHz, Q=Open(x4 I/O)		12	25	mA
I_{CC4}	Operating Current (PP)	CS#=VCC		12	25	mA
I_{CC5}	Operating Current (WRSR)	CS#=VCC		12	25	mA
I_{CC6}	Operating Current (SE)	CS#=VCC		12	25	mA
I_{CC7}	Operating Current (BE)	CS#=VCC		12	25	mA
I_{CC8}	Operating Current (CE)	CS#=VCC		12	25	mA
V_{IL}	Input Low Voltage		-0.5		0.3VCC	V
V_{IH}	Input High Voltage		0.7VCC		VCC+0.4	V
V_{OL}	Output Low Voltage	I_{OL} = 100μA			0.2	V
V_{OH}	Output High Voltage	I_{OH} = -100μA	VCC-0.2			V

Notes:

1. Typical value at T_A = 25℃, VCC = 1.8V.
2. Value guaranteed by design and/or characterization, not 100% tested in production.

(T_A = -40℃~125℃, VCC=1.65~2.0V)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit.
I_{LI}	Input Leakage Current				±4	μA
I_{LO}	Output Leakage Current				±4	μA
I_{CC1}	Standby Current	CS#=VCC, VIN=VCC or VSS		16	290	μA
I_{CC2}	Deep Power-Down Current	CS#=VCC, VIN=VCC or VSS		3	120	μA
I_{CC3}	Operating Current (Read)	CLK=0.1VCC / 0.9VCC at 104MHz, Q=Open(x4 I/O)		12	25	mA
I_{CC4}	Operating Current (PP)	CS#=VCC		12	25	mA
I_{CC5}	Operating Current (WRSR)	CS#=VCC		12	25	mA
I_{CC6}	Operating Current (SE)	CS#=VCC		12	25	mA
I_{CC7}	Operating Current (BE)	CS#=VCC		12	25	mA
I_{CC8}	Operating Current (CE)	CS#=VCC		12	25	mA
V_{IL}	Input Low Voltage		-0.5		0.3VCC	V
V_{IH}	Input High Voltage		0.7VCC		VCC+0.4	V
V_{OL}	Output Low Voltage	I_{OL} = 100μA			0.2	V
V_{OH}	Output High Voltage	I_{OH} = -100μA	VCC-0.2			V

Notes:

1. Typical value at T_A = 25℃, VCC = 1.8V.
2. Value guaranteed by design and/or characterization, not 100% tested in production.

10.6 AC Characteristics

(T_A = -40℃~85℃, VCC=1.65~2.0V)

Symbol	Parameter	Min.	Typ.	Max.	Unit.
f_{C1}	Serial Clock Frequency for all instructions except 03h, 13h			104	MHz
f_R	Serial Clock Frequency For: Read (03h, 13h)			60	MHz
t_{CLH}	Serial Clock High Time	45% (1/fc_{Max})			ns
t_{CLL}	Serial Clock Low Time	45% (1/fc_{Max})			ns
t_{CLCH} t_{CHCL}	Serial Clock Rise/Fall Time (Slew Rate)	0.1			V/ns
t_{SLCH}	CS# Active Setup Time	10			ns
t_{CHSH}	CS# Active Hold Time	10			ns
t_{SHCH}	CS# Not Active Setup Time	10			ns
t_{CHSL}	CS# Not Active Hold Time	10			ns
t_{SHSL}	CS# High Time (Read)	40			ns
	CS# High Time (Write)	40			ns
t_{SHQZ}	Output Disable Time			12	ns
t_{CLQX}	Output Hold Time	1.2			ns
t_{DVCH}	Data In Setup Time	3			ns
t_{CHDX}	Data In Hold Time	3			ns
t_{CLQV}	Clock Low To Output Valid (loading=30pF)			9	ns
	Clock Low To Output Valid (loading=15pF)			7	ns
t_{WHSL}	Write Protect Setup Time Before CS# Low	20			ns
t_{SHWL}	Write Protect Hold Time After CS# High	100			ns
t_{DP}	CS# High To Deep Power-Down Mode			3	μs
t_{RES1}	CS# High To Standby Mode Without Electronic Signature Read			30	μs
t_{SUS}	CS# High To Next Command After Suspend			20	μs
t_{RS}(4)	Latency Between Resume And Next Suspend	100			μs
t_{RST}	CS# High To Next Command After Reset (Except From Erase)			30	μs
t_{RST_E}	CS# High To Next Command After Reset (From Erase)			25	ms
t_{NLP}	Program Nonvolatile Lock bit time		50		μs
t_{NLE}	Erase Nonvolatile Lock array		30	300	ms
t_W	Write Status/Non-Volatile Configuration Register Cycle Time		5	20	ms
t_{BP}	Byte Program Time		30	150	μs

t_{PP}	Page Programming Time		0.25	1.2	ms
t_{SE}	Sector Erase Time		30	300	ms
t_{BE1}	Block Erase Time (32K Bytes)		0.12	0.8	s
t_{BE2}	Block Erase Time (64K Bytes)		0.15	1.2	s
t_{CE}	Chip Erase Time (GD25LR256F)		75	180	s
t_{WRKR}	Write Root Key Register		0.17	2	ms
t_{UHKR}	Update HMAC Key Register		100	150	μs
t_{IMC}	Increment Monotonic Counter		0.08	250	ms
t_{RMC}	Request Monotonic Counter		0.1	1	ms

Notes:

1. Typical value at T_A = 25℃.
2. Value guaranteed by design and/or characterization, not 100% tested in production.
3. Time of CS# High To Next Command After Reset from 01h/11h/B1h command would be $t_W + t_{RST}$
4. Minimum timing must be observed before issuing the next suspend command, and a period equal to or longer than the minimum timing is required in order for the program or erase operation to make progress, but the operation time may exceed the maximum value.

(T_A = -40℃~105℃, VCC=1.65~2.0V)

Symbol	Parameter	Min.	Typ.	Max.	Unit.
f_{C1}	Serial Clock Frequency for all instructions except 03h, 13h			104	MHz
f_R	Serial Clock Frequency For: Read (03h, 13h)			60	MHz
t_{CLH}	Serial Clock High Time	45% (1/fc_{Max})			ns
t_{CLL}	Serial Clock Low Time	45% (1/fc_{Max})			ns
t_{CLCH} t_{CHCL}	Serial Clock Rise/Fall Time (Slew Rate)	0.1			V/ns
t_{SLCH}	CS# Active Setup Time	10			ns
t_{CHSH}	CS# Active Hold Time	10			ns
t_{SHCH}	CS# Not Active Setup Time	10			ns
t_{CHSL}	CS# Not Active Hold Time	10			ns
t_{SHSL}	CS# High Time (Read)	40			ns
	CS# High Time (Write)	40			ns
t_{SHQZ}	Output Disable Time			12	ns
t_{CLQX}	Output Hold Time	1.2			ns
t_{DVCH}	Data In Setup Time	3			ns
t_{CHDX}	Data In Hold Time	3			ns
t_{CLQV}	Clock Low To Output Valid (loading=30pF)			9	ns
	Clock Low To Output Valid (loading=15pF)			7	ns
t_{WHSL}	Write Protect Setup Time Before CS# Low	20			ns
t_{SHWL}	Write Protect Hold Time After CS# High	100			ns
t_{DP}	CS# High To Deep Power-Down Mode			3	μs
t_{RES1}	CS# High To Standby Mode Without Electronic Signature Read			30	μs
t_{SUS}	CS# High To Next Command After Suspend			20	μs
t_{RS}(4)	Latency Between Resume And Next Suspend	100			μs
t_{RST}	CS# High To Next Command After Reset (Except From Erase)			30	μs
t_{RST_E}	CS# High To Next Command After Reset (From Erase)			25	ms
t_{NLP}	Program Nonvolatile Lock bit time		50		μs
t_{NLE}	Erase Nonvolatile Lock array		30	400	ms
t_W	Write Status/Non-Volatile Configuration Register Cycle Time		5	20	ms
t_{BP}	Byte Program Time		30	160	μs
t_{PP}	Page Programming Time		0.25	1.5	ms

t_{SE}	Sector Erase Time		30	400	ms
t_{BE1}	Block Erase Time (32K Bytes)		0.12	1	s
t_{BE2}	Block Erase Time (64K Bytes)		0.15	1.5	s
t_{CE}	Chip Erase Time (GD25LR256F)		75	250	s
t_{WRKR}	Write Root Key Register		0.17	2	ms
t_{UHKR}	Update HMAC Key Register		100	150	μs
t_{IMC}	Increment Monotonic Counter		0.08	250	ms
t_{RMC}	Request Monotonic Counter		0.1	1	ms

Notes:

1. Typical value at T_A = 25℃.
2. Value guaranteed by design and/or characterization, not 100% tested in production.
3. Time of CS# High To Next Command After Reset from 01h/11h/B1h command would be $t_W + t_{RST}$
4. Minimum timing must be observed before issuing the next suspend command, and a period equal to or longer than the minimum timing is required in order for the program or erase operation to make progress, but the operation time may exceed the maximum value.

(T_A = -40℃~125℃, VCC=1.65~2.0V)

Symbol	Parameter	Min.	Typ.	Max.	Unit.
f_{C1}	Serial Clock Frequency for all instructions except 03h, 13h			104	MHz
f_R	Serial Clock Frequency For: Read (03h, 13h)			60	MHz
t_{CLH}	Serial Clock High Time	45% (1/fc_{Max})			ns
t_{CLL}	Serial Clock Low Time	45% (1/fc_{Max})			ns
t_{CLCH} t_{CHCL}	Serial Clock Rise/Fall Time (Slew Rate)	0.1			V/ns
t_{SLCH}	CS# Active Setup Time	10			ns
t_{CHSH}	CS# Active Hold Time	10			ns
t_{SHCH}	CS# Not Active Setup Time	10			ns
t_{CHSL}	CS# Not Active Hold Time	10			ns
t_{SHSL}	CS# High Time (Read)	40			ns
	CS# High Time (Write)	40			ns
t_{SHQZ}	Output Disable Time			12	ns
t_{CLQX}	Output Hold Time	1.2			ns
t_{DVCH}	Data In Setup Time	3			ns
t_{CHDX}	Data In Hold Time	3			ns
t_{CLQV}	Clock Low To Output Valid (loading=30pF)			9	ns
	Clock Low To Output Valid (loading=15pF)			7	ns
t_{WHSL}	Write Protect Setup Time Before CS# Low	20			ns
t_{SHWL}	Write Protect Hold Time After CS# High	100			ns
t_{DP}	CS# High To Deep Power-Down Mode			3	μs
t_{RES1}	CS# High To Standby Mode Without Electronic Signature Read			30	μs
t_{SUS}	CS# High To Next Command After Suspend			20	μs
t_{RS}(4)	Latency Between Resume And Next Suspend	100			μs
t_{RST}	CS# High To Next Command After Reset (Except From Erase)			30	μs
t_{RST_E}	CS# High To Next Command After Reset (From Erase)			25	ms
t_{NLP}	Program Nonvolatile Lock bit time		50		μs
t_{NLE}	Erase Nonvolatile Lock array		30	500	ms
t_W	Write Status/Non-Volatile Configuration Register Cycle Time		5	25	ms
t_{BP}	Byte Program Time		30	180	μs
t_{PP}	Page Programming Time		0.25	1.8	ms

t_{SE}	Sector Erase Time		30	500	ms
t_{BE1}	Block Erase Time (32K Bytes)		0.12	1.2	s
t_{BE2}	Block Erase Time (64K Bytes)		0.15	1.5	s
t_{CE}	Chip Erase Time (GD25LR256F)		75	250	s
t_{WRKR}	Write Root Key Register		0.17	2	ms
t_{UHKR}	Update HMAC Key Register		100	150	μs
t_{IMC}	Increment Monotonic Counter		0.08	250	ms
t_{RMC}	Request Monotonic Counter		0.1	1	ms

Notes:

1. Typical value at T_A = 25℃.
2. Value guaranteed by design and/or characterization, not 100% tested in production.
3. Time of CS# High To Next Command After Reset from 01h/11h/B1h command would be $t_W + t_{RST}$
4. Minimum timing must be observed before issuing the next suspend command, and a period equal to or longer than the minimum timing is required in order for the program or erase operation to make progress, but the operation time may exceed the maximum value.

Figure 101. Serial Input Timing

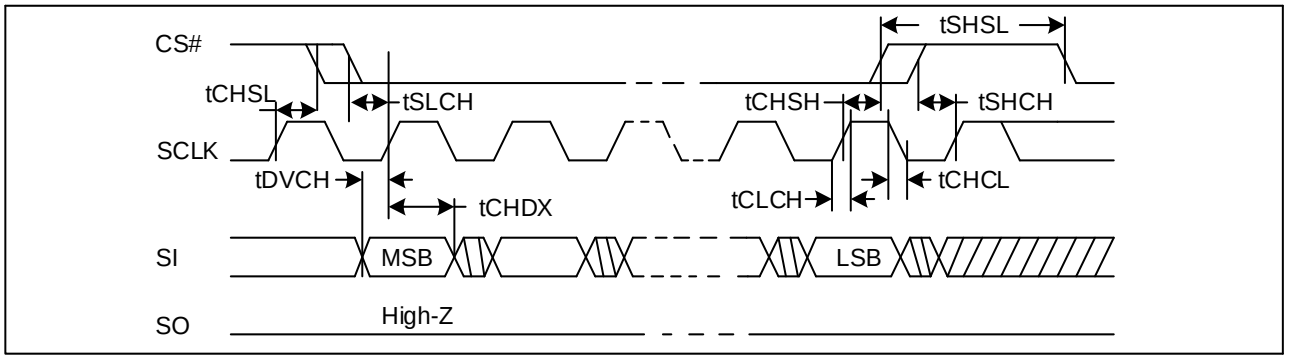


Figure 102. Output Timing

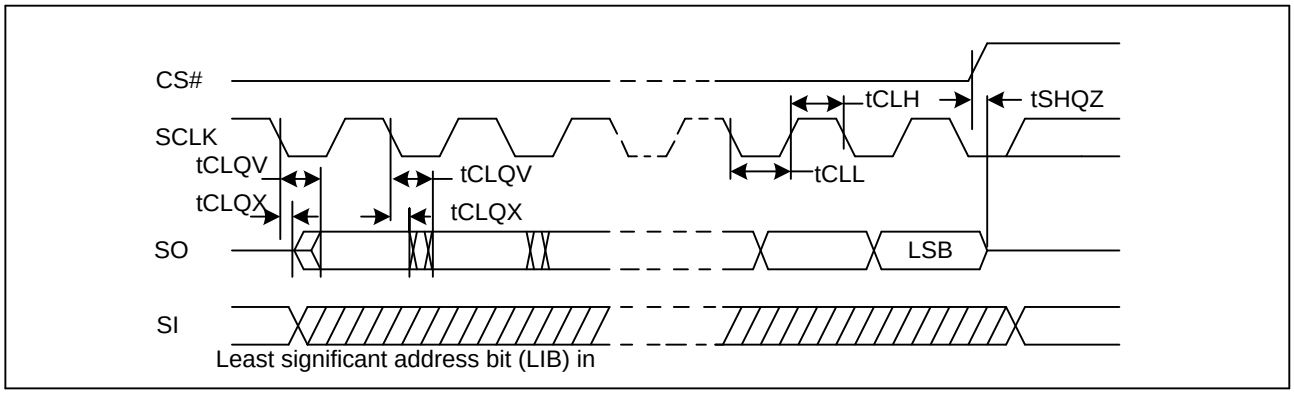


Figure 103. Resume to Suspend Timing Diagram

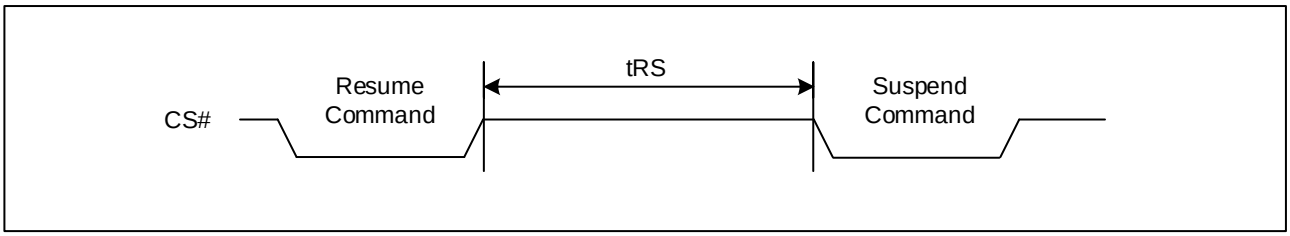


Figure 104. WP# Timing

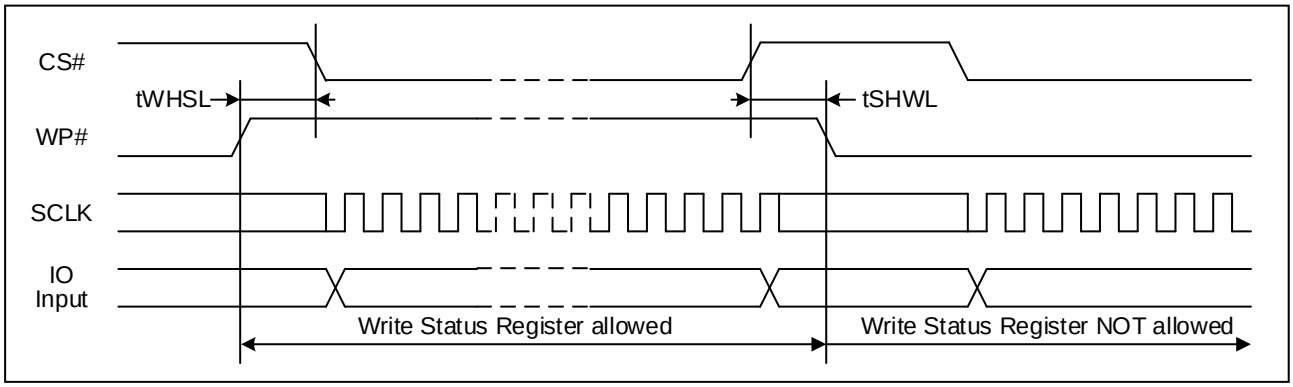


Figure 105. RESET Timing

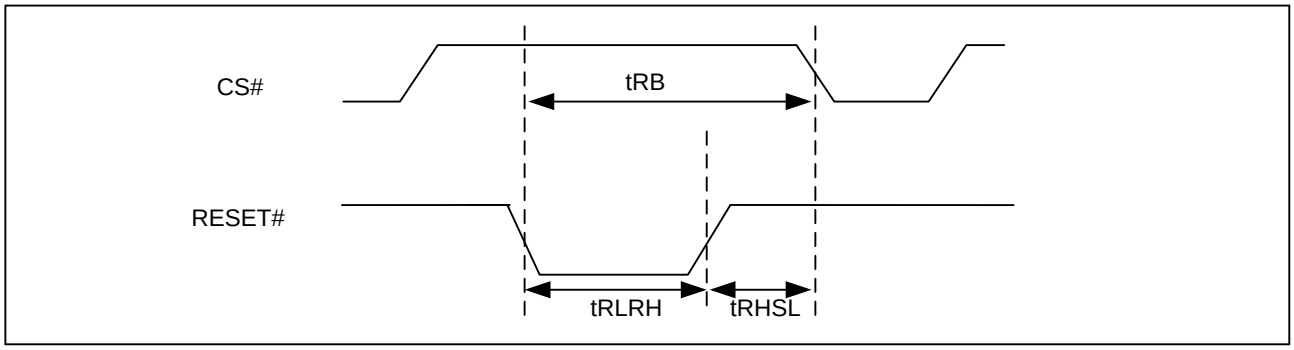


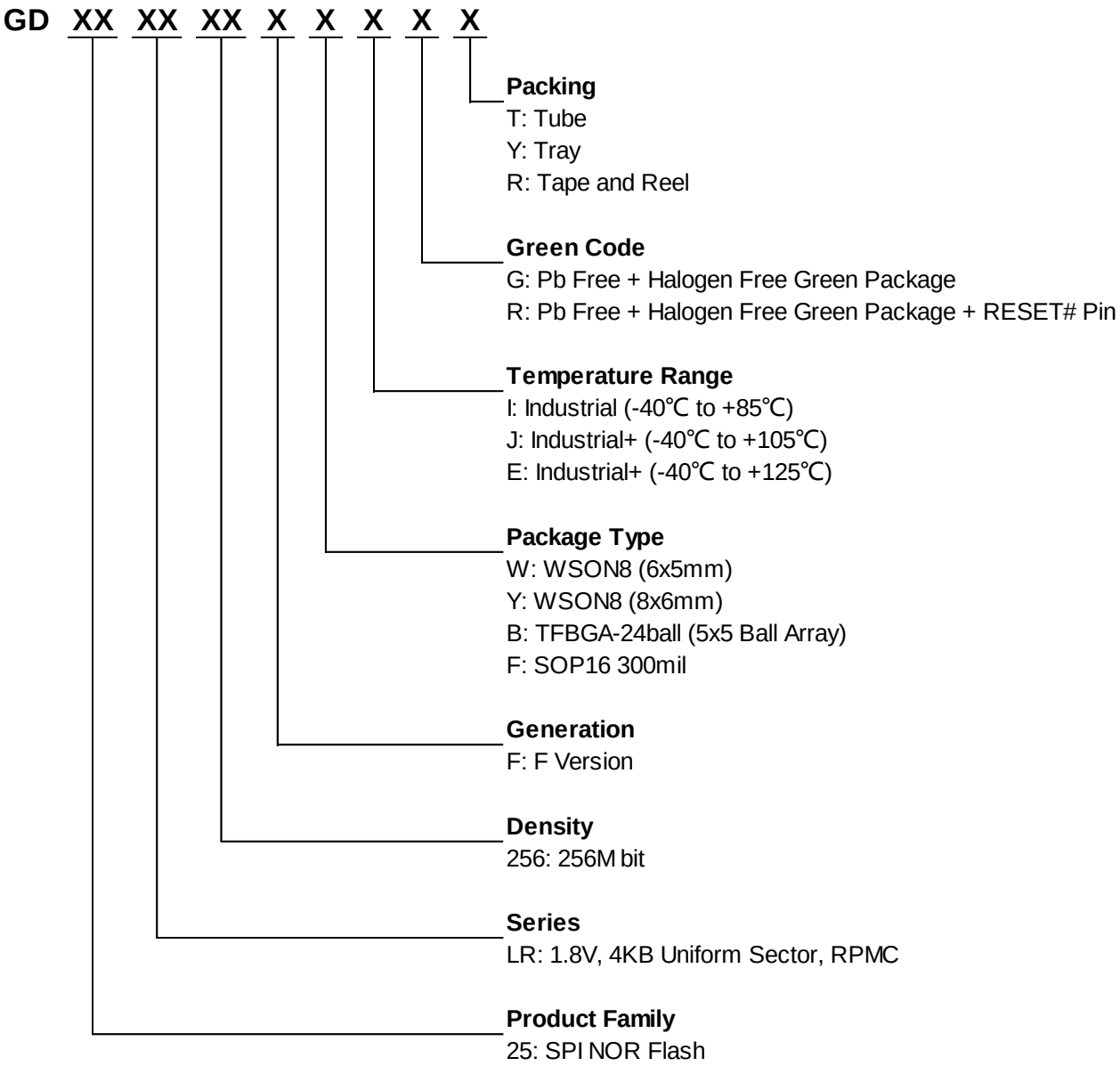
Table 30. Reset Timing

Symbol	Parameter	Min.	Typ.	Max.	Unit.
t_{RLRH}	Reset Pulse Width	1			μs
t_{RHSL}	Reset Hold time before next Operation	50			ns
t_{RB}	Reset Recovery Time (Except From Erase)			40	μs
	Reset Recovery Time (From Erase)			25	ms

Notes:

1. Time of Reset Recovery Time from 01h/11h/B1h command would be t_W + t_{RB}
2. The device need $t_{RB\ (max)}$ at most to get ready for all commands after RESET# low.

11 ORDERING INFORMATION



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11.1 Valid Part Numbers

Please contact GigaDevice regional sales for the latest product selection and available form factors.

Temperature Range I: Industrial (-40℃ to +85℃)

Product Number	Density	Package Type	Packing Options
GD25LR256FWIG	256Mbit	WSON8 (6x5mm)	Y/R
GD25LR256FYIG	256Mbit	WSON8 (8x6mm)	Y/R
GD25LR256FBIR	256Mbit	TFBGA-24ball (5x5 Ball Array)	Y/R
GD25LR256FFIR	256Mbit	SOP16 300mil	T/Y/R

Temperature RangeJ: Industrial (-40℃ to +105℃)

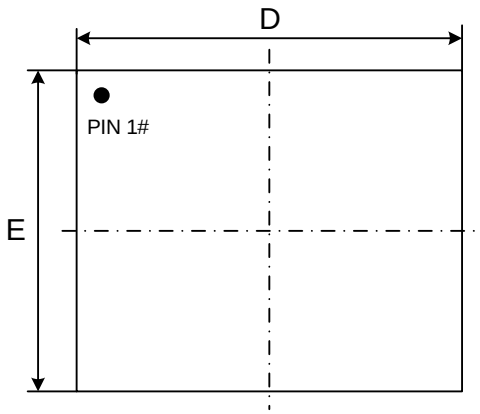
Product Number	Density	Package Type	Packing Options
GD25LR256FWJG	256Mbit	WSON8 (6x5mm)	Y/R
GD25LR256FYJG	256Mbit	WSON8 (8x6mm)	Y/R
GD25LR256FBJR	256Mbit	TFBGA-24ball (5x5 Ball Array)	Y/R
GD25LR256FFJR	256Mbit	SOP16 300mil	T/Y/R

Temperature Range E: Industrial (-40℃ to +125℃)

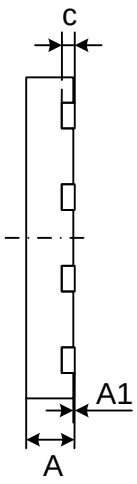
Product Number	Density	Package Type	Packing Options
GD25LR256FWEG	256Mbit	WSON8 (6x5mm)	Y/R
GD25LR256FYEG	256Mbit	WSON8 (8x6mm)	Y/R
GD25LR256FBER	256Mbit	TFBGA-24ball (5x5 Ball Array)	Y/R
GD25LR256FFER	256Mbit	SOP16 300mil	T/Y/R

12 PACKAGE INFORMATION

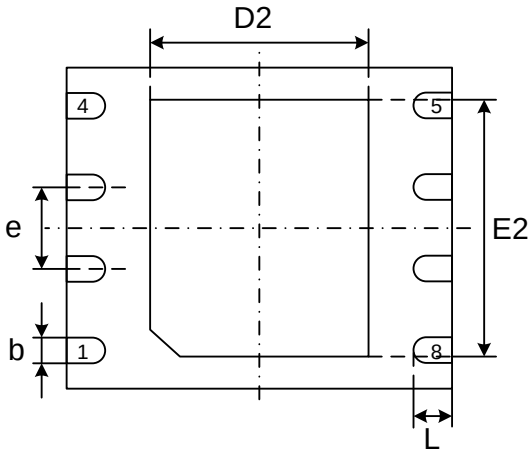
12.1. Package WSON8 (6x5mm)



Top View



Side View



Bottom View

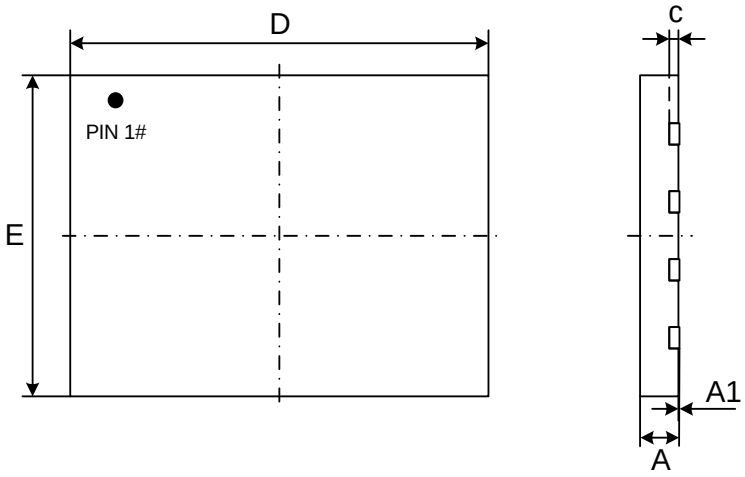
Dimensions

Symbol / Unit		A	A1	c	b	D	D2	E	E2	e	L
mm	Min	0.70	0.00	0.180	0.35	5.90	3.30	4.90	3.90	1.27	0.50
	Nom	0.75	0.02	0.203	0.40	6.00	3.40	5.00	4.00		0.60
	Max	0.80	0.05	0.250	0.50	6.10	3.50	5.10	4.10		0.75

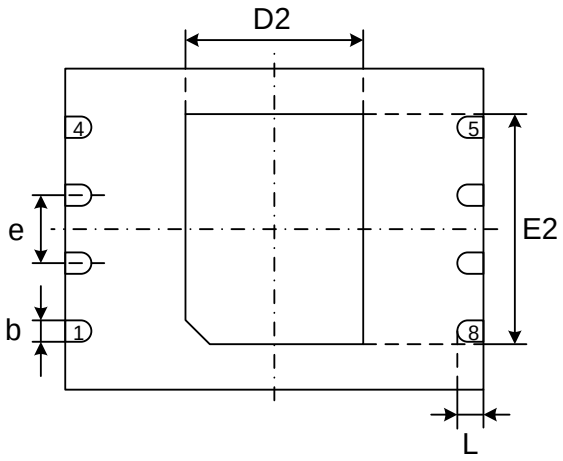
Note:

1. The exposed metal pad area on the bottom of the package is not connected to any internal signal. It is OK to connect it to the system ground (GND) or leave it floating.
2. Coplanarity ≤0.08mm. Package edge tolerance≤0.10mm.
3. The lead shape may be of little difference according to different package lead frames. These lead shapes are compatible with each other.

12.2. Package WSON8 (8x6mm)



Top View Side View



Bottom View

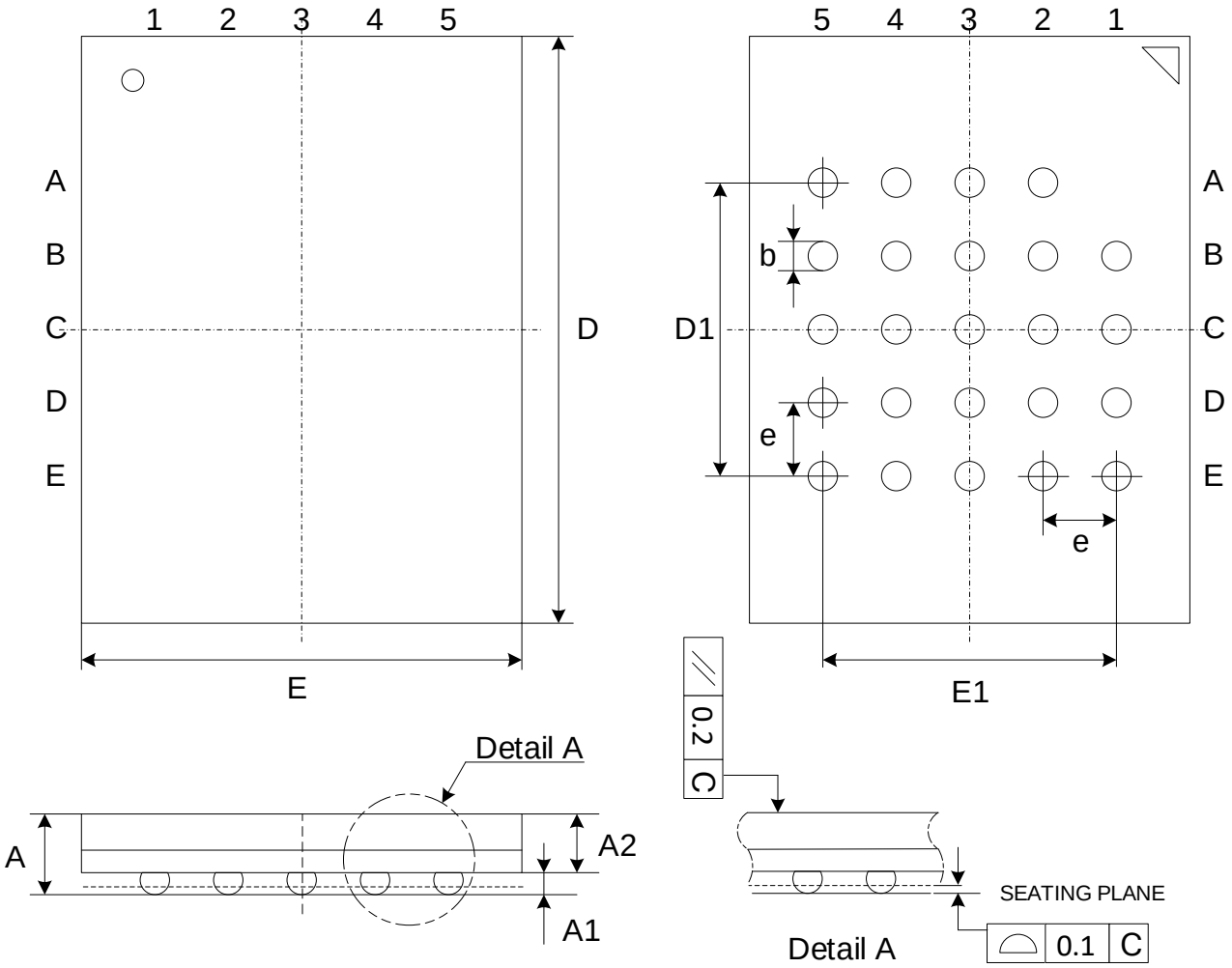
Dimensions

Symbol / Unit		A	A1	c	b	D	D2	E	E2	e	L
mm	Min	0.70	0.00	0.180	0.35	7.90	3.30	5.90	4.20	1.27	0.45
	Nom	0.75	0.02	0.203	0.40	8.00	3.40	6.00	4.30		0.50
	Max	0.80	0.05	0.250	0.45	8.10	3.50	6.10	4.40		0.55

Note:

1. The exposed metal pad area on the bottom of the package is not connected to any internal signal. It is OK to connect it to the system ground (GND) or leave it floating.
2. Coplanarity ≤0.08mm. Package edge tolerance≤0.10mm.
3. The lead shape may be of little difference according to different package lead frames. These lead shapes are compatible with each other.

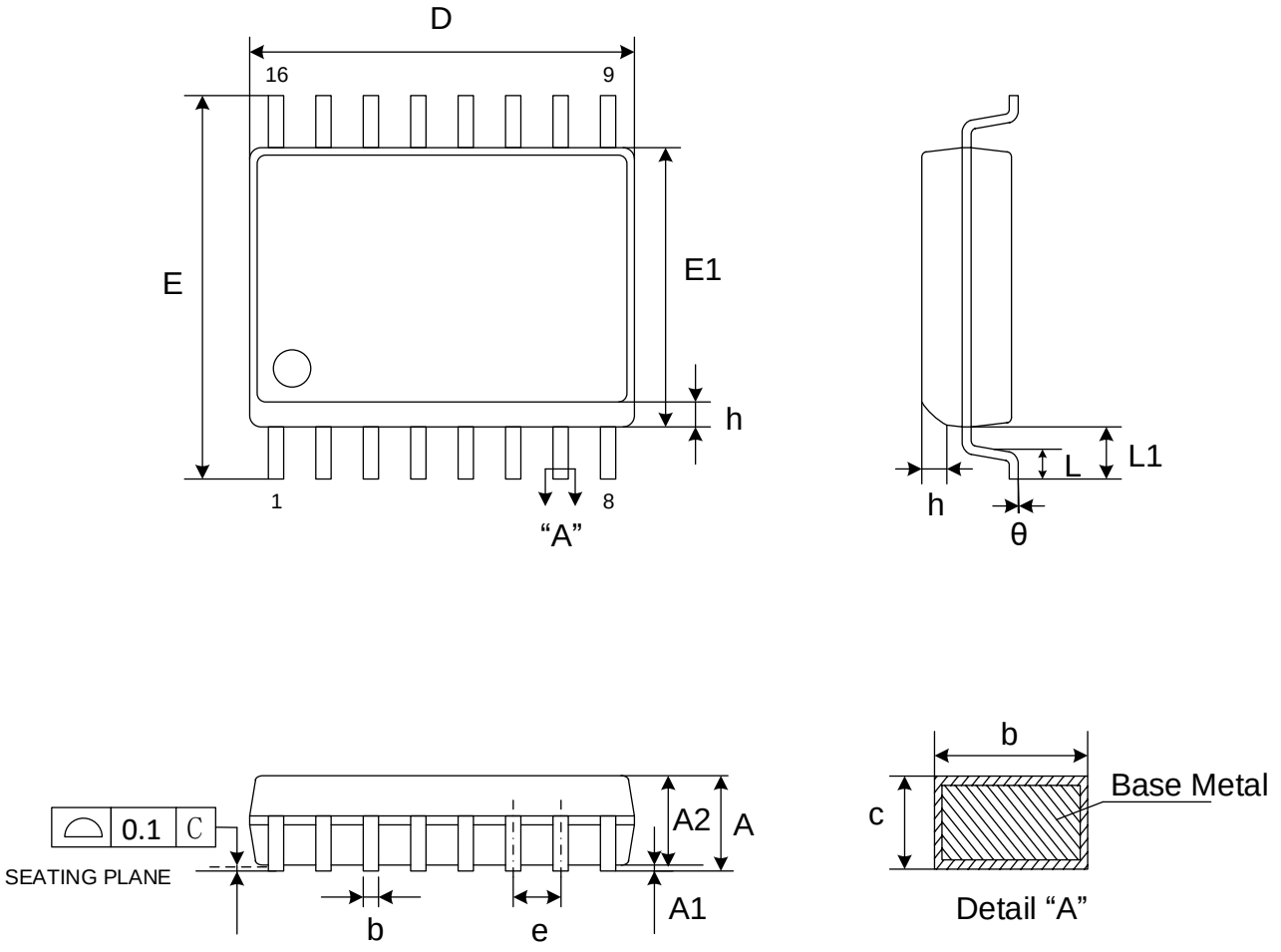
12.3. Package TFBGA-24BALL (5x5 ball array)



Dimensions

Symbol / Unit		A	A1	A2	b	E	E1	D	D1	e
mm	Min	-	0.25	-	0.35	5.90	4.00	7.90	4.00	1.00
	Nom	-	0.30	0.80	0.40	6.00		8.00		
	Max	1.20	0.35	-	0.45	6.10		8.10		

12.4. Package SOP16 300MIL



Dimensions

Symbol / Unit		A	A1	A2	b	c	D	E	E1	e	L	L1	h	θ
mm	Min	-	0.10	2.05	0.31	0.10	10.20	10.10	7.40	1.27	0.40	1.40	0.25	0
	Nom	-	0.20	-	0.41	0.25	10.30	10.30	7.50		-		-	-
	Max	2.65	0.30	2.55	0.51	0.33	10.40	10.50	7.60		1.27		0.75	8

Note:

1. Dimension D does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm per end.
2. Dimension E1 does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25mm per end.

13 REVISION HISTORY

Version No	Description	Page	Date
1.0	Initial Release	All	2023-8-11
1.1	Modify 75h description	P63	2023-10-23
	Modify t_{CLCH}/t_{CHCL}	P84	
1.2	Modify CMP bit description	P22	2023-12-26
	Modify Set Read Parameters(C0h) description	P52	
	Modify Chip Erase(CE)(60h/C7h)	P57	
	Modify Enable Reset(66h) and Reset(99h)	P70	
	Modify ILI,ILO	P81	
	Modify tNLP	P82	
	Modify tBP	P82	
	Modify tPP	P82	
	Modify Ordering Information	P86	
1.3	Modify Serial NOR Flash description	P5-6	2025-5-16
	Modify Typo	P17,P21	
	Add Hardware Reset Description of Data Protection	P11,P13	
	Modify"SRP1=1/SRP0=X" description and Note	P20	
	Add ADP bit description	P22	
	Modify Driver Strength Description	P26-27	
	Delete 32h Quad Page Program Sequence Diagram(QPI)	P53	
	Modify Program/Erase Suspend(PES)(75h) description	P61	
	Add -40℃~105℃ DC/AC Characteristics	P82,86-87	
	Add -40℃~125℃ DC/AC Characteristics	P83,88-89	
	Modify Ordering Information	P92-93	
	Modify Package TFBGA-24BALL(5x5 ball array)	P96	
	Modify Package SOP16 300mil Note	P97	

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