18-Cell Battery Monitor with Daisy Chain Interface

1 Features

- Measures up to 18 battery cells in series
- 2 mV maximum total measurement error
- Stackable architecture for high voltage systems
- Built-in isoSPI interface
  - 1 Mb isolated serial communications
  - Uses a single twisted pair, up to 100 meters
  - Low EMI susceptibility and emissions
  - Bidirectional for broken wire protection
- 290 µs to measure all cells in a system
- Synchronized voltage and current measurement
- 16-bit Δ-Σ ADC with programmable third-order noise filter
- Passive cell balancing up to 200 mA (maximum) with programmable pulse-width modulation
- 9 general-purpose digital I/O or analog inputs
  - Temperature or other sensor inputs
  - Configurable as an I2C or SPI master
- 9 µA sleep mode supply current
- 64-lead LQFP_EP package

2 Applications

- Backup battery systems
- Grid energy storage
- Residential energy storage
- UPS
- High power portable equipment

3 Description

The GD30BM1018 is a multi-cell battery stack monitor that measures up to 18 series connected battery cells with a total measurement error (TME) of less than 2.0 mV. The cell measurement range of 0 V to 5 V makes the GD30BM1018 suitable for most battery chemistries. All 18 cells can be measured in 290 µs, and lower data acquisition rates can be selected for high noise reduction.

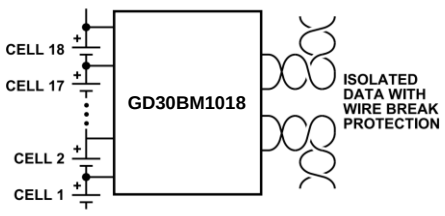
Multiple GD30BM1018 devices can be connected in series, permitting simultaneous cell monitoring of long, high voltage battery strings. Each GD30BM1018 has an isoSPI interface for high speed, RF immune, long distance communications. Multiple devices are connected in a daisy chain with one host processor connection for all devices. This daisy chain can be operated bi-directionally, ensuring communication integrity, even in the event of a fault along the communication path.

The GD30BM1018 can be powered directly from the battery stack or from an isolated supply. The GD30BM1018 includes passive balancing for each cell, with individual pulse-width modulation (PWM) duty cycle control for each cell. Other features include an on-board 5 V regulator, nine general-purpose I/O lines, and a sleep mode, where current consumption is reduced to 9 µA.

Device Information[1]

ORDERING CODE	PACKAGE	BODY SIZE (NOM)
GD30BM1018	LQFP64	10.00mm x 10.00mm

1. For packaging details, see *Package Information* section.



Simplified Application Schematic

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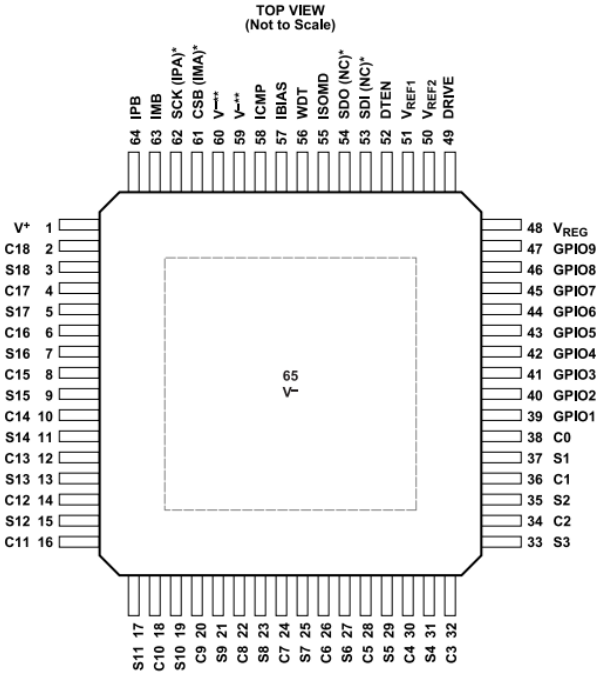
4 Device Overview

4.1 Pinout and Pin Assignment



*THE FUNCTION OF THESE PINS DEPENDS ON THE CONNECTION OF ISOMD:
ISOMD TIED TO V−: CSB, SCK, SDI, SDO
ISOMD TIED TO V_{REG}: IPA, IMA, NC, NC.
**THE V− PINS AND THE EXPOSED PAD MUST BE SHORTED TOGETHER, EXTERNAL TO THE IC.

NOTES
1. EXPOSED PAD (PIN 65) IS V−, MUST BE SOLDERED TO PCB.

4.2 Pin Description

PIN		FUNCTION
NAME	NUM	
V+	1	Positive Supply Pin.
C0 to C18	2, 4, 6, 8, 10, 12, 14, 16, 18, 20, 22, 24, 26, 28, 30, 32, 34, 36, 38	Cell Inputs.
S1 to S18	3, 5, 7, 9, 11, 13, 15, 17, 19, 21, 23, 25, 27, 29, 31, 33, 35, 37	Balance Inputs/Outputs. 18 internal N-channel metal-oxide semiconductor field effect transistors (MOSFETs) are connected between S(n) and C(n-1) for discharging cells.
GPIO1 to GPIO9	39 to 47	General Purpose I/O. GPIO1 to GPIO9 can be used as digital inputs or digital outputs or as analog inputs with a measurement range from V– to 5 V. GPIO3, GPIO4, and GPIO5 can be used as I2C or SPI ports.
VREG	48	5 V Regulator Input. Bypass with an external 1 µF capacitor.

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DRIVE	49	Connect the base of an NPN transistor to the DRIVE pin. Connect the collector to V+ and the emitter to V_{REG}.
VREF2	50	Buffered 2nd Reference Voltage for Driving Multiple 10 kΩ Thermistors. Bypass with an external 1F capacitor.
VREF1	51	ADC Reference Voltage. Bypass with an external 1 μF capacitor. No dc loads allowed.
DTEN	52	Discharge Timer Enable. Connect DTEN to VREG to enable the discharge timer.
SDI, SDO, CSB, SCK	53, 54, 61, 62	4-Wire SPI. Active low chip select (CSB), serial clock (SCK), and serial data in (SDI) are digital inputs. Serial data out (SDO) is an open drain NMOS output pin. SDO requires a 5 kΩ pull-up resistor.
ISOMD	55	Serial Interface Mode. Connecting ISOMD to VREG configures Pin 53, Pin 54, Pin 61, and Pin 62 of the GD30BM1018 for 2-wire isoSPI mode. Connecting ISOMD to V– configures the GD30BM1018 for 4-wire SPI mode.
WDT	56	Watchdog Timer Output Pin. This is an open drain negative metal-oxide semiconductor (NMOS) digital output. WDT can be left disconnected or connected with a 1 M resistor to VREG. If the GD30BM1018 does not receive a valid command within 2 seconds, the watchdog timer circuit resets the GD30BM1018 and the WDT pin goes high impedance.
IBIAS	57	Isolated Interface Current Bias. Tie IBIAS to V– through a resistor divider to set the interface output current level. When the isoSPI interface is enabled, the IBIAS pin voltage is 2 V. The IPA and IMA or IPB and IMB output current drive is set to 20 times the current, IB, sourced from the IBIAS pin.
ICMP	58	Isolated Interface Comparator Voltage Threshold Set. Tie ICMP to the resistor divider between IBIAS and V- to set the voltage threshold of the isoSPI receiver comparators. The comparator thresholds are set to half the voltage on the ICMP pin.
V–	59, 60	Negative Supply Pins. The V– pins must be shorted together, external to the IC.
IMA, IPA	61, 62	Isolated 2-Wire Serial Interface Port A. IMA (negative) and IPA (positive) are a differential input/output pair.
IMB, IPB	63, 64	Isolated 2-Wire Serial Interface Port B. IMB (negative) and IPB (positive) are a differential input/output pair.
EPAD (V–)	65	Exposed Pad (V–). The exposed pad must be soldered to the PCB.

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5 Parameter Information

Specifications are at T_A = 25°C, unless otherwise noted. The test conditions are V+ = 59.4 V and V_{REG} = 5.0 V, unless otherwise noted. The ISOMD pin is tied to the V– pin, unless otherwise noted.

5.1 ADC DC Characteristics

PARAMETER	TEST CONDITIONS/COMMENTS	MIN	TYP	MAX	UNIT
Measurement Resolution			0.1		mV/Bit
ADC Offset Voltage[1]			0.1		mV
ADC Gain Error[1]			0.01		%
TME in Normal Mode	C(n) to C(n–1) = 0		±0.2		mV
	GPIO(n) to V– = 0		±1.5		mV
	C(n) to C(n–1) = 2.0			±0.5	mV
	C(n) to C(n–1) = 2.0, apply over the full specified temperature range			±0.9	mV
	GPIO(n) to V– = 2.0, apply over the full specified temperature range			±5.5	mV
	C(n) to C(n–1) = 3.3			±0.5	mV
	C(n) to C(n–1) = 3.3, apply over the full specified temperature range			±1.3	mV
	GPIO(n) to V– = 3.3, apply over the full specified temperature range			±6.0	mV
	C(n) to C(n–1) = 4.2			±0.5	mV
	C(n) to C(n–1) = 4.2, apply over the full specified temperature range			±1.7	mV
	GPIO(n) to V– = 4.2, apply over the full specified temperature range			±6.0	mV
	C(n) to C(n–1) = 5.0		±0.5		mV
	GPIO(n) to V– = 5.0		±1.5		mV
	Sum of all cells, apply over the full specified temperature range		±0.2	±0.7	%
	Internal temperature, T = maximum specified temperature		±5		°C
	V_{REG} pin, apply over the full specified temperature range	–1.3	–0.75	0	%
	V_{REF2} pin, apply over the full specified temperature range	–0.65	0.05	0.20	%
	Digital supply voltage, V_{REGD}, apply over the full specified temperature range	–0.5	0.3	1.5	%
TME in Filtered Mode	C(n) to C(n–1) = 0		±1		mV
	GPIO(n) to V– = 0		±2		mV
	C(n) to C(n–1) = 2.0			±1.5	mV
	C(n) to C(n–1) = 2.0, apply over the full specified temperature range			±3.0	mV
	GPIO(n) to V– = 2.0, apply over the full specified temperature range			±6	mV
	C(n) to C(n–1) = 3.3			±1.8	mV
	C(n) to C(n–1) = 3.3, apply over the full specified temperature range			±4.0	mV
	GPIO(n) to V– = 3.3, apply over the full specified temperature range			±6.5	mV
	C(n) to C(n–1) = 4.2			±2.3	mV
	C(n) to C(n–1) = 4.2, apply over the full specified temperature range			±4.5	mV
	GPIO(n) to V– = 4.2, apply over the full specified temperature range			±6.5	mV

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ADC DC Characteristics (Continued)

PARAMETER	TEST CONDITIONS/COMMENTS	MIN	TYP	MAX	UNIT
TME in Filtered Mode	C(n) to C(n–1) = 5.0		±2		mV
	GPIO(n) to V– = 5.0		±2		mV
	Sum of all cells, apply over the full specified temperature range		±0.2	±0.6	%
	Internal temperature, T = maximum specified temperature		±5		°C
	V_{REG} pin, apply over the full specified temperature range	–1.2	–0.6	0	%
	V_{REF2} pin, apply over the full specified temperature range	–1.1	0.05	0.20	%
	Digital supply voltage, V_{REGD}, apply over the full specified temperature range	-0.5	0.2	1.5	%
TME in Fast Mode	C(n) to C(n–1) = 0		±2		mV
	GPIO(n) to V– = 0		±2		mV
	C(n) to C(n–1) = 2.0, apply over the full specified temperature range			±4	mV
	GPIO(n) to V– = 2.0, apply over the full specified temperature range			±6	mV
	C(n) to C(n–1) = 3.3, apply over the full specified temperature range			±10	mV
	GPIO(n) to V– = 3.3, apply over the full specified temperature range			±6	mV
	C(n) to C(n–1) = 4.2, apply over the full specified temperature range			±11	mV
	GPIO(n) to V– = 4.2, apply over the full specified temperature range			±6	mV
	C(n) to C(n–1) = 5.0		±9		mV
	GPIO(n) to V– = 5.0		±2		mV
	Sum of all cells, apply over the full specified temperature range		±0.3	±0.8	%
	Internal temperature, T = maximum specified temperature		±5		°C
	V_{REG} pin, apply over the full specified temperature range	–1.15	–0.66	0	%
	V_{REF2} pin, apply over the full specified temperature range	–0.4	0.3	0.32	%
	Digital supply voltage, V_{REGD}, apply over the full specified temperature range	–2.5	0.3	2	%
Input Range	C(n), n = 1 to 18, apply over the full specified temperature range	C(n-1)		C(n-1)+5	V
	C0, apply over the full specified temperature range	0		1	V
	GPIO(n), n = 1 to 9, apply over the full specified temperature range	0		5	V
Input Leakage Current (I_L) When Inputs Are Not Being Measured	C(n), n = 0 to 18, apply over the full specified temperature range		10	±250	nA
	GPIO(n), n = 1 to 9, apply over the full specified temperature range		10	±250	nA
Input Current When Inputs Are Being Measured (State: Core = Measure)	C(n), n = 0 to 18		±1		µA
	GPIO(n), n = 1 to 9		±1		µA
Input Current During Open Wire Detection	Apply over the full specified temperature range	70	100	130	µA

1. The ADC specifications are guaranteed by the TME specification.

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5.2 Voltage Reference Characteristics

PARAMETER	TEST CONDITIONS/COMMENTS	MIN	TYP	MAX	UNIT
1st Reference Voltage (V_{REF1})	V_{REF1} pin, no load, apply over the full specified temperature range	3.266	3.276	3.286	V
1st Reference Voltage Temperature Coefficient (T_C)	V_{REF1} pin, no load		1		ppm/°C
1st Reference Voltage Thermal Hysteresis	V_{REF1} pin, no load		20		ppm
1st Reference Voltage Long Term Drift	V_{REF1} pin, no load		20		ppm/√KHR
2nd Reference Voltage (V_{REF2})	V_{REF2} pin, no load, apply over the full specified temperature range	2.97	3	3.01	V
	V_{REF2} pin, 5 kΩ load to V–, apply over the full specified temperature range	2.969	3	3.011	V
2nd Reference Voltage TC	V_{REF2} pin, no load		60		ppm/°C
2nd Reference Voltage Thermal Hysteresis	V_{REF2} pin, no load		100		ppm
2nd Reference Voltage Long Term Drift	V_{REF2} pin, no load		60		ppm/√KHR

5.3 General DC Characteristics

PARAMETER	TEST CONDITIONS/COMMENTS	MIN	TYP	MAX	UNIT
V+ Supply Current (I_{VP})	State: core = sleep, isoSPI = idle, V_{REG} = 0 V		9.4	10.5	µA
	State: core = sleep, isoSPI = idle, V_{REG} = 0 V, apply over the full specified temperature range		9.4	11	µA
	State: core = sleep, isoSPI = idle, V_{REG} = 5 V		3	5	µA
	State: core = sleep, isoSPI = idle, V_{REG} = 5 V, apply over the full specified temperature range		3	9	µA
	State: core = standby	190	200	210	µA
	State: core = standby, apply over the full specified temperature range	170	200	225	µA
	State: core = REFUP	0.77	0.8	0.82	mA
	State: core = REFUP, apply over the full specified temperature range	0.71	0.8	0.85	mA
	State: core = measure	0.65	0.95	1.35	mA
	State: core = measure, apply over the full specified temperature range	0.6	0.95	1.4	mA

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General DC Characteristics (Continued)

PARAMETER	TEST CONDITIONS/COMMENTS	MIN	TYP	MAX	UNIT
V_{REG} Supply Current ($I_{REG(CORE)}$)	State: core = sleep, isoSPI = idle, V_{REG} = 5 V		3.1	6	µA
	State: core = sleep, isoSPI = idle, V_{REG} = 5 V, apply over the full specified temperature range		3.1	9	µA
	State: core = standby	0.87	0.88	0.89	mA
	State: core = standby, apply over the full specified temperature range	0.86	0.88	0.91	mA
	State: core = REFUP	4.9	5.0	5.1	mA
	State: core = REFUP, apply over the full specified temperature range	4.7	5.0	5.3	mA
	State: core = measure	10	11	12	mA
	State: core = measure, apply over the full specified temperature range	11.5	11	12.5	mA
Additional V_{REG} Supply Current If isoSPI Is in Ready/Active States ($I_{REG(isoSPI)}$) Note: Active State Current Assumes t_{CLK} = 1 µs	ISOMD = 0, RB1 + RB2 = 2 kΩ, ready, apply over the full specified temperature range	3.6	4.5	5.2	mA
	ISOMD = 0, RB1 + RB2 = 2 kΩ, active, apply over the full specified temperature range	5.6	6.8	8.1	mA
	ISOMD = 1, RB1 + RB2 = 2 kΩ, ready, apply over the full specified temperature range	4.0	5.2	6.5	mA
	ISOMD = 1, RB1 + RB2 = 2 kΩ, active, apply over the full specified temperature range	7.0	8.5	10.5	mA
	ISOMD = 0, RB1 + RB2 = 20 kΩ, ready, apply over the full specified temperature range	1.0	1.8	2.4	mA
	ISOMD = 0, RB1 + RB2 = 20 kΩ, active, apply over the full specified temperature range	1.3	2.3	3.3	mA
	ISOMD = 1, RB1 + RB2 = 20 kΩ, ready, apply over the full specified temperature range	1.6	2.5	3.5	mA
	ISOMD = 1, RB1 + RB2 = 20 kΩ, active, apply over the full specified temperature range	1.8	3.1	4.8	mA
V+ Supply Voltage	TME specifications met, apply over the full specified temperature range	16	60	99	V
V+ to C18 Voltage	TME specifications met, apply over the full specified temperature range	–0.3			V
V+ to C12 Voltage	TME specifications met, apply over the full specified temperature range			40	V
C13 Voltage	TME specifications met, apply over the full specified temperature range	25			V
C7 Voltage	TME specifications met, apply over the full specified temperature range	1			V

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General DC Characteristics (Continued)

PARAMETER	TEST CONDITIONS/COMMENTS	MIN	TYP	MAX	UNIT
VREG Supply Voltage (V_{REG})	TME supply rejection < 1 mV/V, apply over the full specified temperature range	4.5	5	5.5	V
DRIVE Output Voltage	Sourcing 1 μA	5.4	5.7	5.9	V
	Sourcing 1 μA, apply over the full specified temperature range	5.2	5.7	6.1	V
	Sourcing 500 μA, apply over the full specified temperature range	5.1	5.7	6.1	V
Digital Supply Voltage (V_{REGD})	Apply over the full specified temperature range	2.7	3	3.6	V
Discharge Switch On Resistance	V_{CELL} = 3.6 V, apply over the full specified temperature range		4	10	Ω
Thermal Shutdown Temperature			150		°C
Watchdog Timer Pin Low ($V_{OL(WDT)}$)	WDT pin sinking 4 mA, apply over the full specified temperature range			0.4	V
General-Purpose I/O Pin Low ($V_{OL(GPIO)}$)	GPIO pin sinking 4 mA (used as digital output), apply over the full specified temperature range			0.4	V

1. The active state current is calculated from dc measurements. The active state current is the additional average supply current into VREG when there are continuous 1 MHz communications on the isoSPI ports with 50% data 1s and 50% data 0s. Slower clock rates reduce the supply current.

5.4 ADC Timing Characteristics

PARAMETER	TEST CONDITIONS/COMMENTS	MIN	TYP	MAX	UNIT
(t_{CYCLE}) Measurement and Calibration Cycle Time When Starting from the REFUP State in Normal Mode	Measure 18 cells, apply over the full specified temperature range	2027	2343	2488	μs
	Measure 3 cells, apply over the full specified temperature range	352	407	432	μs
	Measure 18 cells and 2 GPIO inputs, apply over the full specified temperature range	2717	3140	3335	μs
Measurement and Calibration Cycle Time When Starting from the REFUP State in Filtered Mode	Measure 18 cells, apply over the full specified temperature range	174.2	201.3	213.8	ms
	Measure 3 cells, apply over the full specified temperature range	29.1	33.6	35.7	ms
	Measure 18 cells and 2 GPIO inputs, apply over the full specified temperature range	232.3	268.5	285.1	ms
Measurement and Calibration Cycle Time When Starting from the REFUP State in Fast Mode	Measure 18 cells, apply over the full specified temperature range	970	1121	1191	μs
	Measure 3 cells, apply over the full specified temperature range	176	203	215	μs
	Measure 18 cells and 2 GPIO inputs, apply over the full specified temperature range	1307	1511	1605	μs

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ADC Timing Characteristics (Continued)

PARAMETER	TEST CONDITIONS/COMMENTS	MIN	TYP	MAX	UNIT
Skew Time (t_{SKEW1}). The Time Difference Between Cell 18 and GPIO1 Measurements, Command = ADCVAX	Fast mode, apply over the full specified temperature range	168	194	206	µs
	Normal mode, apply over the full specified temperature range	470	543	577	µs
Skew Time(t_{SKEW2}). The Time Difference Between Cell 18 and Cell 1 Measurements, Command = ADCV	Fast mode, apply over the full specified temperature range	202	233	248	µs
	Normal mode, apply over the full specified temperature range	580	670	711	µs
Regulator Start-Up Time (t_{WAKE})	V_{REG} generated from the DRIVE pin (apply over the full specified temperature range		200	400	µs
Watchdog or Discharge Timer (t_{SLEEP})	DTEN pin = 0 or DCTO, Bits[3:0] = 0000, apply over the full	1.8	2	2.2	sec
	specified temperature range				
	DTEN pin = 1 and DCTO, Bits[3:0] ≠ 0000	0.5		120	min
Reference Wake-Up Time (t_{REFUP}). Added to t_{CYCLE} Time When Starting from the Standby State. t_{REFUP} = 0 When Starting from Other States	t_{REFUP} is independent of the number of channels measured and the ADC mode, apply over the full specified temperature range	2.7	3.5	4.4	ms
ADC Clock Frequency (f_S)			3.3		MHz

5.5 SPI DC Characteristics

PARAMETER	TEST CONDITIONS/COMMENTS	MIN	TYP	MAX	UNIT
SPI Pin Digital Input Voltage High ($V_{IH(SPI)}$)	CSB, SCK, and SDI pins, apply over the full specified temperature range	2.3			V
SPI Pin Digital Input Voltage Low ($V_{IL(SPI)}$)	CSB, SCK, and SDI pins, apply over the full specified temperature range			0.8	V
Configuration Pin Digital Input Voltage High ($V_{IH(CFG)}$)	ISOMD, DTEN, and GPIO1 to GPIO9 pins, apply over the full specified temperature range	2.7			V
Configuration Pin Digital Input Voltage Low ($V_{IL(CFG)}$)	ISOMD, DTEN, and GPIO1 to GPIO9 pins, apply over the full specified temperature range			1.2	V
Digital Input Current ($I_{LEAK(DIG)}$)	CSB, SCK, SDI, ISOMD, and DTEN pins, apply over the full specified temperature range			±1	µA

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SPI DC Characteristics (Continued)

PARAMETER	TEST CONDITIONS/COMMENTS	MIN	TYP	MAX	UNIT
Digital Output Low ($V_{OL(SDO)}$)	SDO pin sinking 1 mA, apply over the full specified temperature range			0.3	V

5.6 ISOSPI DC Characteristics

PARAMETER	TEST CONDITIONS/COMMENTS	MIN	TYP	MAX	UNIT
Voltage on IBIAS Pin (V_{BIAS})	Ready/active state, apply over the full specified temperature range	1.9	2.0	2.1	V
	Idle state		0		V
Isolated Interface Bias Current (I_B)	R_{BIAS} = 2 kΩ to 20 kΩ, apply over the full specified temperature range	0.1		1.0	mA
Isolated Interface Current Gain (A_{IB})	Transmitter pulse amplitude (V_A) = ≤ 1.6 V, IB = 1 mA, apply over the full specified temperature range	18	20	22	mA/mA
	I_B = 0.1 mA, apply over the full specified temperature range	18	20	24.5	mA/mA
Transmitter Pulse Amplitude (V_A)	V_A = IPx voltage (V_{IPx}) – IMx voltage (V_{IMx}), apply over the full specified temperature range			1.6	V
Threshold-Setting Voltage on ICMP Pin (V_{ICMP})	Receiver comparator threshold voltage (V_{TCMP}) = receiver comparator threshold voltage gain (A_{TCMP}) × V_{ICMP}, apply over the full specified temperature range	0.2		1.5	V
Input Leakage Current on ICMP Pin ($I_{LEAK (ICMP)}$)	V_{ICMP} = 0 V to V_{REG}, apply over the full specified temperature range			±1	µA
Leakage Current on IPx and IMx Pins ($I_{LEAK (IPx/IMx)}$)	Idle state, V_{IPx} or V_{IMx}, 0 V to V_{REG}, apply over the full specified temperature range			±1	µA
Receiver Comparator Threshold Voltage Gain (A_{TCMP})	Receiver common-mode bias (V_{CM}) = $V_{REG/2}$ to V_{REG}–0.2 V, V_{ICMP} = 0.2 V to 1.5 V, apply over the full specified temperature range	0.4	0.5	0.6	V/V
Receiver Common-Mode Bias (V_{CM})	IPx and IMx not driving	(V_{REG} - V_{ICMP}/3 - 167 mV)			V
Receiver Input Resistance (R_{IN})	Single-ended to the IPA, IMA, IPB, and IMB pins, apply over the full specified temperature range	26	35	45	kΩ

5.7 ISOSPI Idle/Wake-up Characteristics

PARAMETER	TEST CONDITIONS/COMMENTS	MIN	TYP	MAX	UNIT
Differential Wake-Up Voltage (V_{WAKE})	Dwell time at V_{WAKE} before wake detection (t_{DWELL}) = 240 ns, apply over the full specified temperature range	200			mV
t_{DWELL}	V_{WAKE} = 200 mV, apply over the full specified temperature range	240			ns
Start-Up Time After Wake Detection (t_{READY})	Apply over the full specified temperature range			10	µs
Idle Timeout Duration (t_{IDLE})	Apply over the full specified temperature range	4.3	5.5	6.7	ms

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5.8 ISOSPI Pulse Timing Characteristics

PARAMETER	TEST CONDITIONS/COMMENTS	MIN	TYP	MAX	UNIT
Chip Select Half Pulse Width ($t_{1/2PW(CS)}$)	Transmitter, apply over the full specified temperature range	120	150	180	ns
Chip Select Signal Filter ($t_{FILT(CS)}$)	Receiver, apply over the full specified temperature range	70	90	110	ns
Chip Select Pulse Inversion Delay ($t_{INV(CS)}$)	Transmitter, apply over the full specified temperature range	120	155	190	ns
Chip Select Valid Pulse Window ($t_{WNDW(CS)}$)	Receiver, apply over the full specified temperature range	220	270	330	ns
Data Half Pulse Width ($t_{1/2PW(D)}$)	Transmitter, apply over the full specified temperature range	40	50	60	ns
Data Signal Filter ($t_{FILT(D)}$)	Receiver, apply over the full specified temperature range	10	25	35	ns
Data Pulse Inversion Delay ($t_{INV(D)}$)	Transmitter, apply over the full specified temperature range	40	55	65	ns
Data Valid Pulse Window ($t_{WNDW(D)}$)	Receiver, apply over the full specified temperature range	70	90	110	ns

5.9 SPI Timing Requirements

PARAMETER	TEST CONDITIONS/COMMENTS	MIN	TYP	MAX	UNIT
SCK Period (t_{CLK}) [1]	Apply over the full specified temperature range	1			µs
SDI Setup Time Before SCK Rising Edge (t_1)	Apply over the full specified temperature range	25			ns
SDI Hold Time After SCK Rising Edge (t_2) d	Apply over the full specified temperature range	25			ns
SCK Low (t_3)	$t_{CLK} = t_3 + t_4 \geq 1$ µs, apply over the full specified temperature range	200			ns
SCK High (t_4)	$t_{CLK} = t_3 + t_4 \geq 1$ µs, apply over the full specified temperature range	200			ns
CSB Rising Edge to CSB Falling Edge (t_5)	Apply over the full specified temperature range	0.65			µs
SCK Rising Edge to CSB Rising Edge (t_6) [1]	Apply over the full specified temperature range	0.8			µs
CSB Falling Edge to SCK Rising Edge (t_7)[1]	Apply over the full specified temperature range	1			µs

1. These timing specifications are dependent on the delay through the cable and include allowances for 50 ns of delay in each direction. 50 ns corresponds to 10 m of Category 5 (CAT-5) cable (which has a velocity of propagation of 66% the speed of light). Using longer cables requires derating these specs by the amount of additional delay.

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5.10 ISOSPI Timing Characteristics

PARAMETER	TEST CONDITIONS/COMMENTS	MIN	TYP	MAX	UNIT
SCK Falling Edge to SDO Valid (t_8) 1	Apply over the full specified temperature range			60	ns
SCK Rising Edge to Short ±1 Transmit (t_9)	Apply over the full specified temperature range			50	ns
CSB Transition to Long ±1 Transmit (t_{10})	Apply over the full specified temperature range			60	ns
CSB Rising Edge to SDO Rising (t_{11}) 1	Apply over the full specified temperature range			200	ns
Data Return Delay (t_{RTN})	Apply over the full specified temperature range	325	375	425	ns
Chip-Select Daisy-Chain Delay ($t_{DSY(CS)}$)	Apply over the full specified temperature range		120	180	ns
Data Daisy-Chain Delay ($t_{DSY(D)}$)	Apply over the full specified temperature range	200	250	300	ns
Data Daisy-Chain Lag (vs. Chip Select) (t_{LAG})	= ($t_{DSY(D)}$ + $t_{1/2PW(D)}$) - ($t_{DSY(CS)}$ + $t_{1/2PW(CS)}$), apply over the full specified temperature range	0	35	70	ns
Chip Select High to Low Pulse Governor ($t_{5(GOV)}$)	Apply over the full specified temperature range	0.6		0.82	µs
Data to Chip-Select Pulse Governor ($t_{6(GOV)}$)	Apply over the full specified temperature range	0.8		1.05	µs
isoSPI Port Reversal Blocking t_{BLOCK} Window	Apply over the full specified temperature range	2		10	µs

1. These specifications do not include rise or fall time of SDO. Although fall time (typically 5 ns due to the internal pull-down transistor) is not a concern, the rising edge transition time (t_{RISE}) is dependent on the pull-up resistance and load capacitance on the SDO pin. The time constant must be chosen such that SDO meets the setup time requirements of the microcontroller unit (MCU).

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5.11 Absolute Maximum Ratings

PARAMETER	RATING
Total Supply Voltage, V+ to V–	112.5 V
Supply Voltage (Relative to C12), V+ to C12	50 V
Input Voltage (Relative to V–)	
C0	–0.3 V to +6 V
C18	–0.3 V to MIN (V+ + 5.5 V, 112.5 V)
C(n), S(n)	–0.3 V to MIN (8 x n, 112.5 V)
IPA, IMA, IPB, and IMB	–0.3 V to VREG + 0.3 V, ⩽6 V
DRIVE	–0.3 V to +7 V
All Other Pins	–0.3 V to +6 V
Voltage Between Inputs	
C(n) to C(n-1) and S(n) to C(n-1)	–0.3 V to +8 V
C18 to C15, C15 to C12, C12 to C9, C9	–0.3 V to +21 V
to C6, C6 to C3, and C3 to C0	
Current In and Out of Pins	
All Pins Except V_{REG}, IPA, IMA, IPB,	10 mA
IMB, C(n), and S(n)	
IPA, IMA, IPB, and IMB	30 mA
Specified Junction Temperature Range	
Junction Temperature (T_{JMAX})	150°C
Storage Temperature Range	–65°C to +150°C

5.12 Electrical Sensitivity

SYMBOL	CONDITIONS	VALUE	UNIT
$V_{ESD(HBM)}$	Human-body model (HBM), ANSI/ESDA/JEDEC JS-001-2017[1]	±1000	V
$V_{ESD(CDM)}$	Charge-device model (CDM), ANSI/ESDA/JEDEC JS-002-2022[2]	±750	V

1. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
2. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.13 Thermal Resistance

SYMBOL[1]	CONDITIONS	LQFP64	UNIT
Θ_{JA}	Natural convection, 2S2P PCB	17	°C/W
Θ_{JC}	Cold plate, 2S2P PCB	2.5	°C/W

1. Thermal characteristics are based on simulation, and meet JEDEC document JESD51-7.

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5.14 Typical Characteristics

T_A = 25°C, unless otherwise noted.

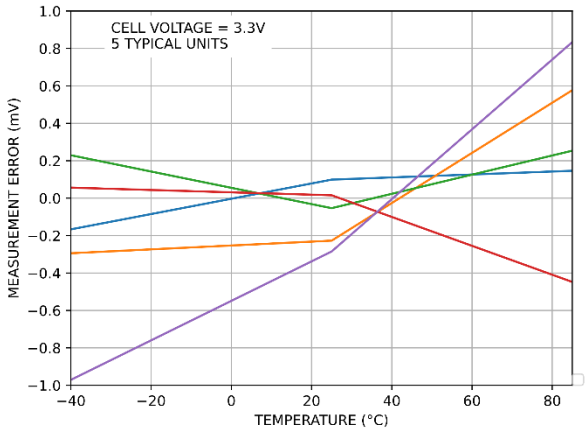

Figure 1. Measurement Error vs. Temperature

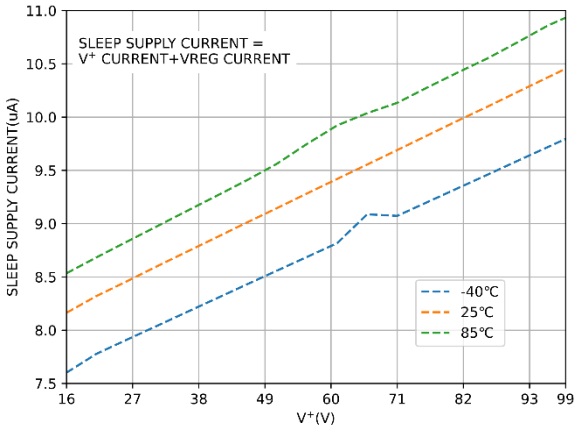

Figure 2. Sleep Supply Current vs. V+

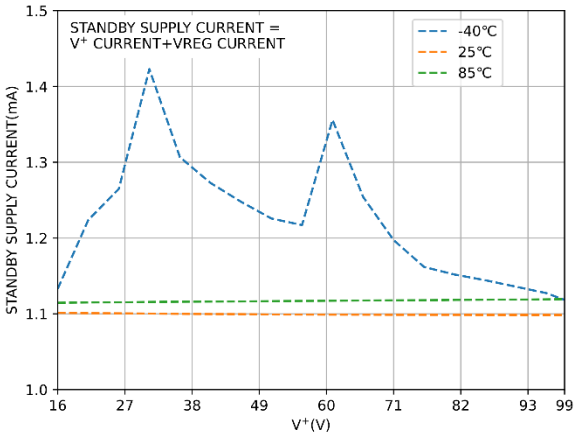

Figure 3. Standby Supply Current vs. V+

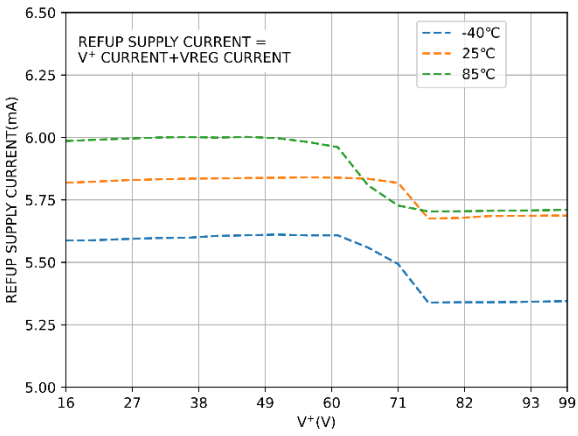

Figure 4. REFUP Supply Current vs. V+

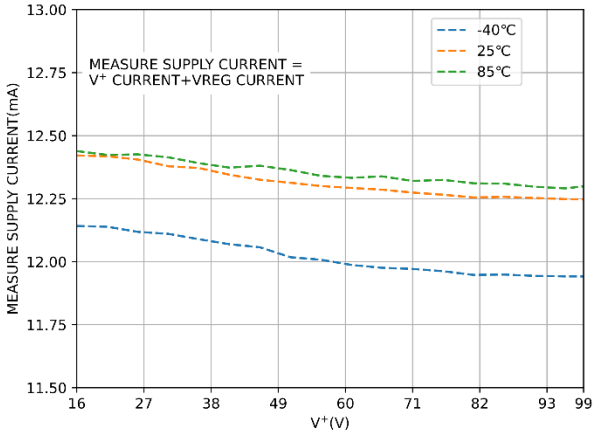

Figure 5. Measurement Supply Current vs. V+

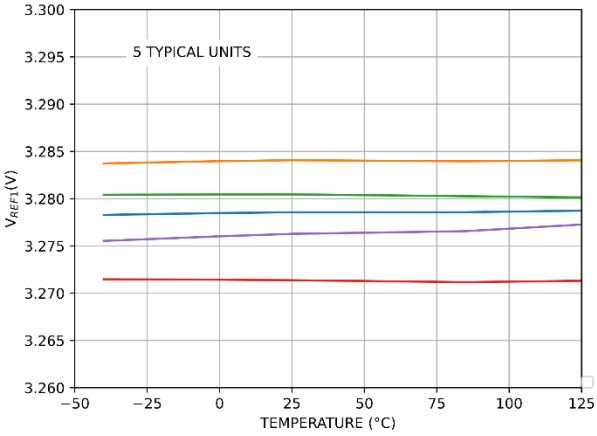

Figure 6. VREF1 vs. Temperature

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Typical Characteristics(Continued)

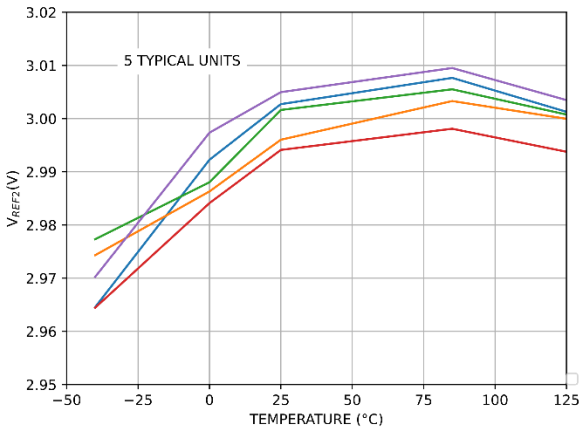

Figure 7. VREF2 vs. Temperature

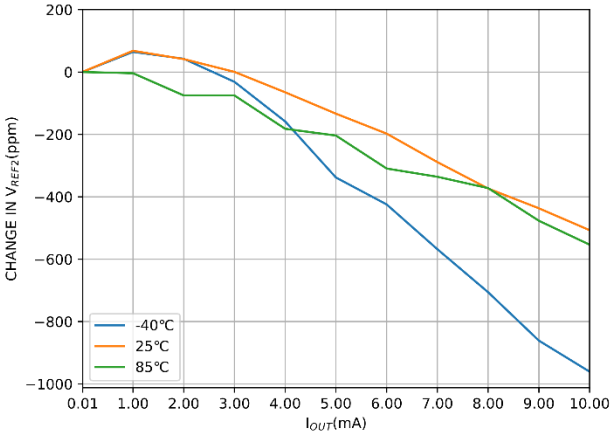

Figure 8. VREF2 Load Regulation

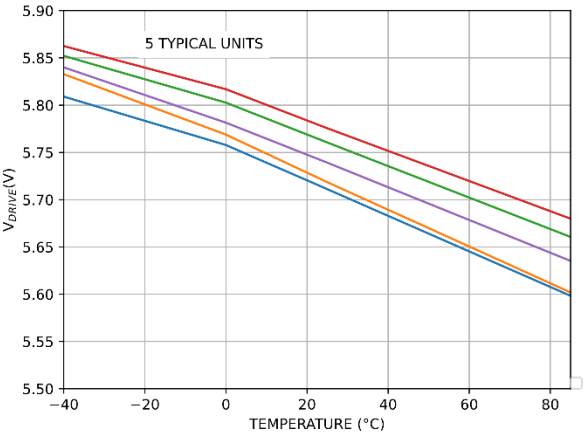

Figure 9. VDRIVE vs. Temperature

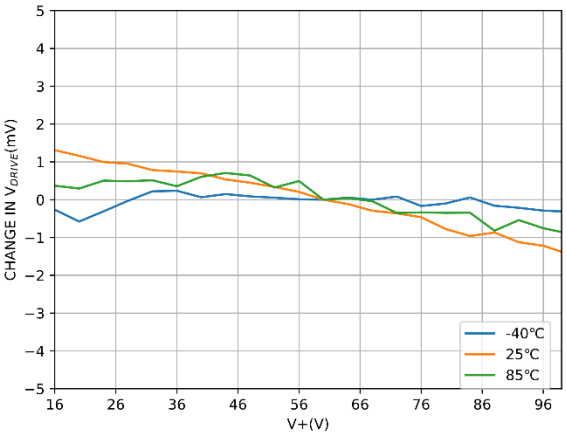

Figure 10. VDRIVE and V+ Line Regulation

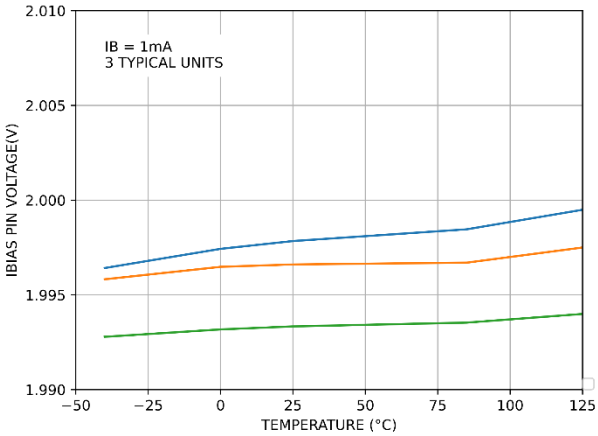

Figure 11. IBIAS Pin Voltage vs. Temperature

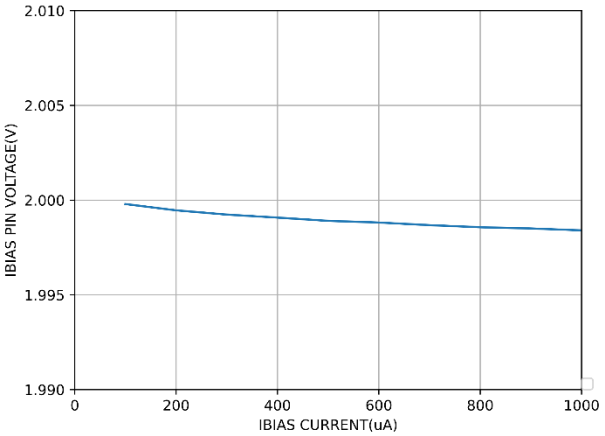

Figure 12. IBIAS Pin Voltage Load Regulation

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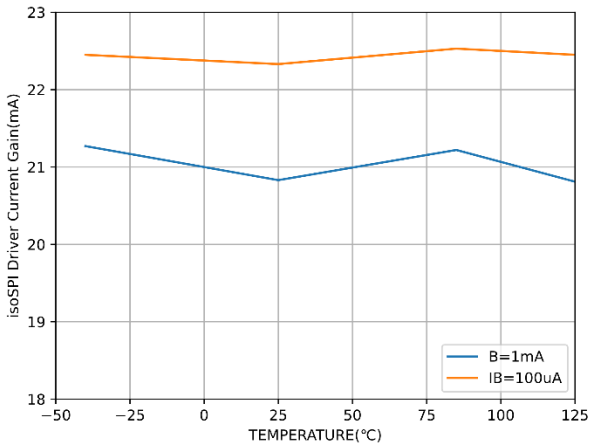

Figure 13. isoSPI Driver Current Gain(Port A and Port B) vs. Temperature

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6 Functional Description

6.1 Block Diagram

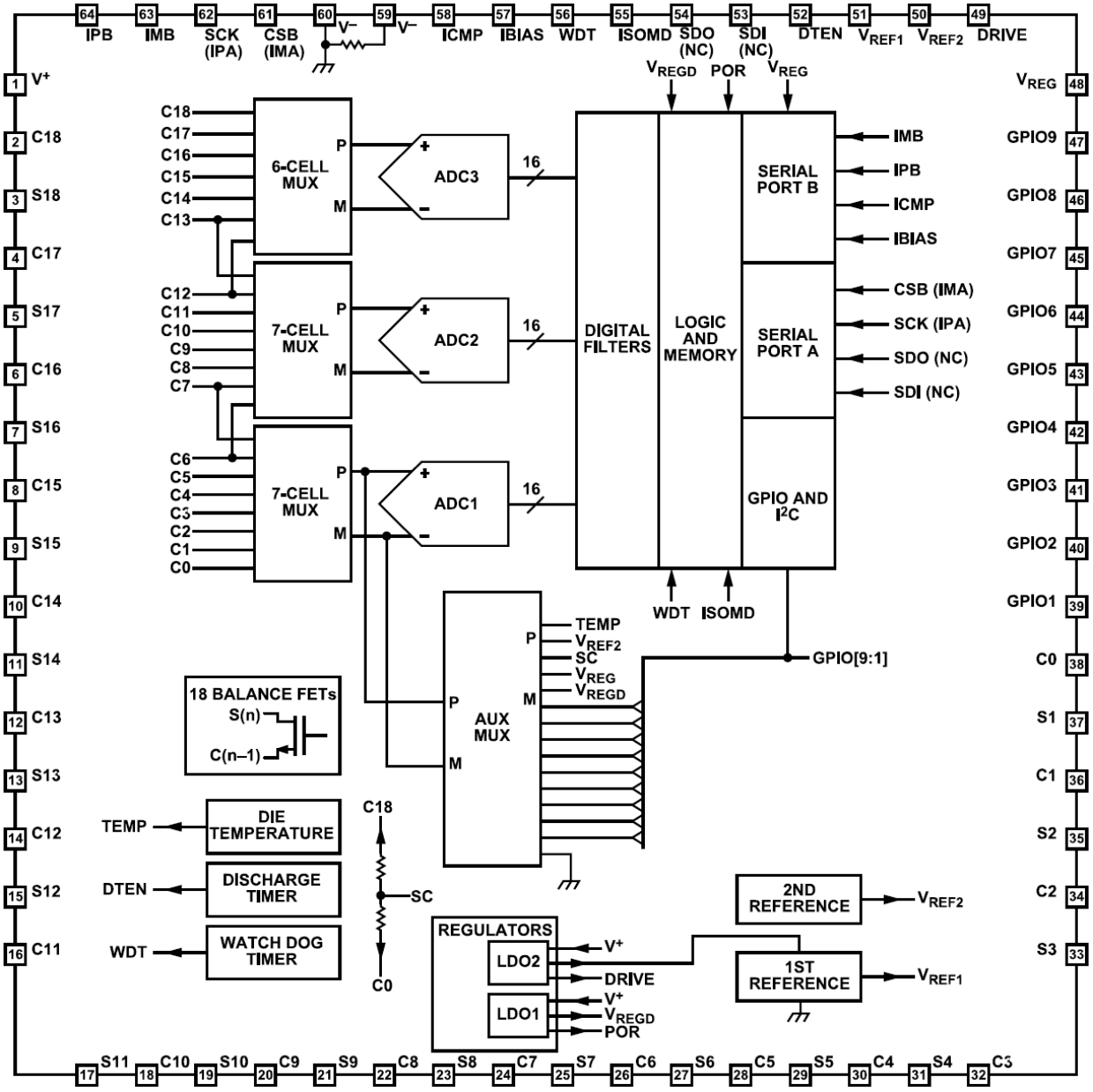

Figure 14. GD30BM1018 Functional Block Diagram

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7 Operation

7.1 State Diagram

The operation of the GD30BM1018 is divided into two separate sections: the core circuit and the isoSPI circuit. Both sections have an independent set of operating states, as well as a shutdown timeout.

7.2 GD30BM1018 Core State Descriptions

7.2.1 Sleep State

The reference and ADCs are powered down. The watchdog timer (see the Watchdog and Discharge Timer section) has timed out. The discharge timer is either disabled or timed out. The supply currents are reduced to minimum levels. The isoSPI ports are in the idle state. The DRIVE pin is 0 V.

If a wake-up signal is received (see the Waking Up the Serial Interface section), the GD30BM1018 enters the standby state.

7.2.2 Standby State

The reference and the ADCs are off. The watchdog timer and/or the discharge timer is running. The DRIVE pin powers the V_{REG} pin to 5 V through an external transistor. Alternatively, V_{REG} can be powered by an external supply.

When a valid ADC command is received or the REFON bit is set to 1 in Configuration Register Group A, the IC pauses for t_{REFUP} to allow the reference to power up and then enters either the REFUP or measure state. Otherwise, if no valid commands are received for t_{SLEEP} (when both the watchdog and discharge timer expire), the GD30BM1018 returns to the sleep state. If the discharge timer is disabled, only the watchdog timer is relevant.

7.2.3 REFUP State

To reach this state, the REFON bit in Configuration Register Group A must be set to 1 (using the WRCFGA command, see Table 33). The ADCs are off. The reference is powered up so that the GD30BM1018 can initiate ADC conversions more quickly than from the standby state.

When a valid ADC command is received, the IC goes to the measure state to begin the conversion. Otherwise, the GD30BM1018 returns to the standby state when the REFON bit is set to 0, either manually (using WRCFGA command) or automatically when the watchdog timer expires (the GD30BM1018 then moves straight into the sleep state if both timers are expired).

7.2.4 Measure State

The GD30BM1018 performs ADC conversions in the measure state. The reference and ADCs are powered up.

After ADC conversions complete, the GD30BM1018 transitions to either the REFUP or standby state, depending on the REFON bit. Additional ADC conversions can be initiated more quickly by setting REFON = 1 to take advantage of the REFUP state.

Note that non ADC commands do not cause a core state transition. Only an ADC conversion or diagnostic commands place the core in the measure state.

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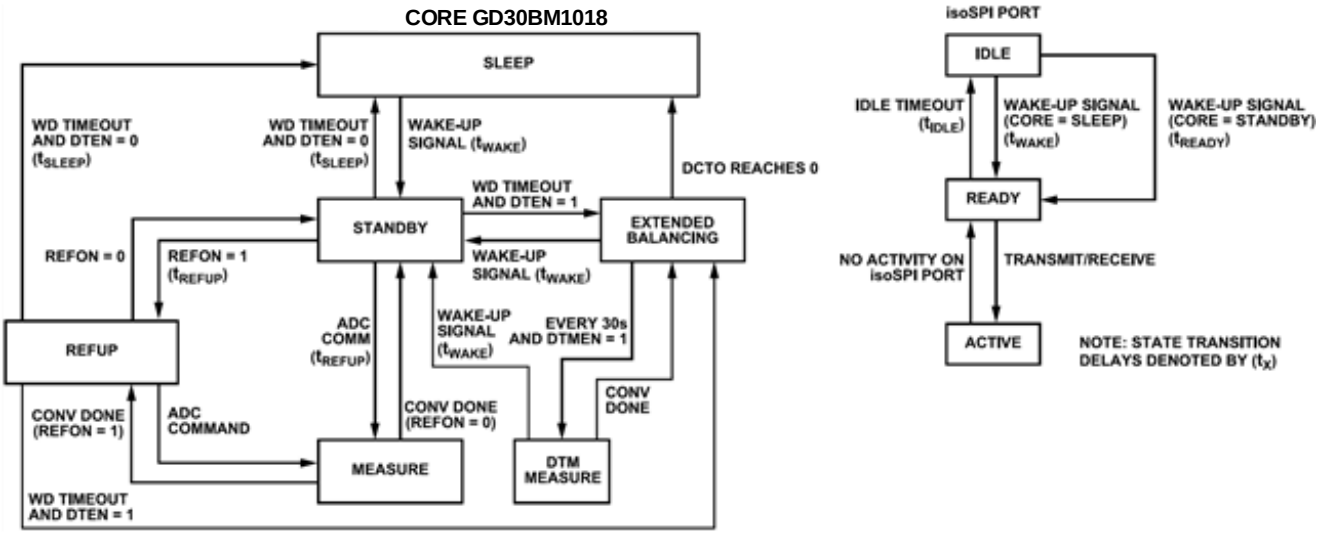

Figure 15. GD30BM1018 Operation State Diagram

7.3 ISOSPI State Descriptions

The GD30BM1018 has two isoSPI ports (Port A and Port B) for daisy-chain communication.

7.3.1 Idle State

In the idle state, the isoSPI ports are powered down.

When isoSPI Port A or Port B receives a wake-up signal (see the *Waking up the Serial Interface* section), the isoSPI enters the ready state. This transition happens quickly (within t_{READY}) if the core is in the standby state. If the core is in the sleep state when the isoSPI receives a wake-up signal, the core transitions to the ready state within t_{WAKE}.

7.3.2 Ready State

In the ready state, the isoSPI port(s) are ready for communication. The serial interface current in the ready state depends on the status of the ISOMD pin and $R_{BIAS} = R_{B1} + R_{B2}$ (the external resistors tied to the IBIAS pin). If there is no activity (that is, no wake-up signal) on Port A or Port B for greater than t_{IDLE}, the GD30BM1018 enters the idle state. When the serial interface is transmitting or receiving data, the GD30BM1018 enters the active state.

7.3.3 Active State

In the active state, the GD30BM1018 is transmitting and receiving data using one or both of the isoSPI ports. The serial interface consumes maximum power in the active state. The supply current increases with clock frequency as the density of isoSPI pulses increases.

7.4 Power Consumption

The GD30BM1018 is powered via two pins: V+ and V_{REG}. The V+ input requires voltage greater than or equal to the top cell voltage minus 0.3 V and provides power to the high voltage elements of the core circuits. The V_{REG} input requires 5 V and provides power to the remaining core circuits and the isoSPI circuitry. The V_{REG} input can be powered through an external transistor, driven by the regulated DRIVE output pin. Alternatively, V_{REG} can be powered by an external supply.

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The power consumption varies according to the operational states. Table 1 and Table 2 provide equations to approximate the supply pin currents in each state. The V+ pin current depends only on the core state. However, the V_{REG} pin current depends on both the core state and isoSPI state, and can therefore be divided into two components. The isoSPI interface draws current only from the V_{REG} pin.

$$I_{REG} = I_{REG(CORE)} + I_{REG(isoSPI)} \quad (1)$$

In the sleep state, the V_{REG} pin draws approximately 3.1 µA if powered by an external supply. Otherwise, the V+ pin supplies the necessary current.

Table 1. Core Supply Current

State	I_{VP}	$I_{REG(CORE)}$
Sleep		
V_{REG} = 0 V	6.1 µA	0 µA
V_{REG} = 5 V	3 µA	3.1 µA
Standby	14 µA	35 µA
REFUP	550 µA	900 µA
Measure	950 µA	15 mA

Table 2. isoSPI Supply Current Equations

isoSPI	ISOMD Connection	$I_{REG(isoSPI)}$
Idle	Not applicable	0 mA
Ready	V_{REG}	$2.2mA + 3 \times I_B$
	V−	$1.5mA + 3 \times I_B$
Active	V_{REG}	$\text{Write}: 2.5mA + \left(3 + 20 \times \frac{100ns}{t_{CLK}}\right) \times I_B$
		$\text{Read}: 2.5mA + \left(3 + 20 \times \frac{100ns \times 1.5}{t_{CLK}}\right) \times I_B$
	V−	$1.8mA + \left(3 + 20 \times \frac{100ns}{t_{CLK}}\right) \times I_B$

7.5 ADC Operation

There are three ADCs inside the GD30BM1018. The three ADCs operate simultaneously when measuring 18 cells. Only one ADC is used to measure the general-purpose inputs. This section uses the term ADC to refer to one or all ADCs, depending on the operation being performed. This section refers to ADC1, ADC2, and ADC3 when it is necessary to distinguish between the three circuits, such as in the timing diagrams.

7.5.1 ADC Mode

The ADCOPT bit (CFGAR0, Bit 0) in Configuration Register Group A and the mode selection bits, MD, Bits[1:0], in the conversion command together provide eight modes of operation for the ADC which correspond to different

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oversampling ratios (OSRs). The accuracy and timing of these modes are summarized in Table 3. In each mode, the ADC first measures the inputs and then performs a calibration of each channel. The names of the modes are based on the -3 dB bandwidth of the ADC measurement.

Mode 7 kHz (normal): In this mode, the ADC has high resolution and low TME. This mode is considered the normal operating mode because of the optimum combination of speed and accuracy.

Mode 27 kHz (fast): In this mode, the ADC has maximum throughput but has some increase in TME. Therefore, this mode is also referred to as the fast mode. The increase in speed comes from a reduction in the OSR. This increase results in an increase in noise and average measurement error.

Mode 26 Hz (filtered): In this mode, the ADC digital filter -3 dB frequency is lowered to 26 Hz by increasing the OSR. This mode is also referred to as the filtered mode due to its low -3 dB frequency. The accuracy is similar to the 7 kHz (normal) mode with lower noise.

Modes 14 kHz, 3 kHz, 2 kHz, 1 kHz, and 422 Hz: Modes 14 kHz, 3 kHz, 2 kHz, 1 kHz, and 422 Hz provide additional options to set the ADC digital filter -3 dB at 13.5 kHz, 3.4 kHz, 1.7 kHz, 845 Hz, and 422 Hz, respectively. The accuracy of the 14 kHz mode is similar to the 27 kHz (fast) mode. The accuracy of the 3 kHz, 2 kHz, 1 kHz, and 422 Hz modes is similar to the 7 kHz (normal) mode.

The filter bandwidths and the conversion times for these modes are provided in Table 3. If the core is in the standby state, an additional t_{REFUP} time is required to power up the reference before beginning the ADC conversions. The reference can remain powered up between ADC conversions if the REFON bit in Configuration Register Group A is set to 1 so that the core is in REFUP state after delay t_{REFUP}. The subsequent ADC commands do not have the t_{REFUP} delay before beginning ADC conversions.

Table 3. ADC Filter Bandwidth and Accuracy

Mode	–3 dB Filter BW	–40 dB Filter BW	TME Specification at 3.3 V, 25°C	TME Specification at 3.3 V,–40°C, +85°C
27 kHz (Fast Mode)	27 kHz	84 KHz	±5mV	±10.0mV
14 kHz	13.5 KHz	42 KHz	±5mV	±10.0mV
7 kHz (Normal Mode)	6.8 KHz	21 KHz	±0.5mV	±1.3mV
3 kHz	3.4 KHz	10.5 KHz	±2mV	±4mV
2 kHz	1.7 KHz	5.3 KHz	±2mV	±4mV
1 kHz	845 KHz	2.6 KHz	±2mV	±4mV
422 Hz	422 Hz	1.3 KHz	±2mV	±4mV
26 Hz (Filtered Mode)	26 Hz	82 Hz	±2mV	±4mV

7.5.2 ADC Range and Resolution

The C inputs and GPIO inputs have the same range and resolution. The ADC inside the GD30BM1018 has an approximate range from –0.82 V to +5.73 V. Negative readings are rounded to 0 V. The format of the data is a 16-bit unsigned integer where the LSB represents 100 µV. Therefore, a reading of 0x80E8 (33,000 decimal) indicates a measurement of 3.3 V.

The specified range of the ADC is 0 V to 5 V. In Table 4, the precision range of the ADC is arbitrarily defined as 0.5 V to 4.5 V. This range is where the quantization noise is relatively constant even in the lower OSR modes. Table 4 summarizes the total noise in this range for all eight ADC operating modes. Also shown in Table 4 is the

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noise free resolution. For example, 14-bit noise free resolution in normal mode implies that the top 14 bits are noise free with a dc input, but that the 15th and 16th LSBs flicker.

7.5.3 Measuring Cell Voltages (ADCV Command)

The ADCV command initiates the measurement of the battery cell inputs, Pin C0 through Pin C18. This command has options to select the number of channels to measure and the ADC mode. See the Commands section for the ADCV command format.

Figure 16 shows the timing of the ADCV command that measures all 18 cells. After the receipt of the ADCV command to measure all 18 cells, ADC1 sequentially measures the bottom 6 cells. ADC2 measures the middle 6 cells and ADC3 measures the top 6 cells. After the cell measurements complete, each channel is calibrated to remove any offset errors.

Table 5 shows the conversion times for the ADCV command measuring all 18 cells. The total conversion time is given by t_{6C} which indicates the end of the calibration step.

Figure 17 shows the timing of the ADCV command that measures only 3 cells.

Table 4. ADC Range and Resolution

Mode	Full Range[1]	Specified Range	Precision Range[2]	LSB	Format	Maximum Noise	Noise Free Resolution[3]
27 kHz (Fast)	–0.8192 V to +5.7344 V	0 V to 5 V	0.5 V to 4.5 V	100 µV	Unsigned 16 bits	±4 mV p-p	10 bits
14 kHz	–0.8192 V to +5.7344 V	0 V to 5 V	0.5 V to 4.5 V	100 µV	Unsigned 16 bits	±1 mV p-p	12 bits
7 kHz (Normal)	–0.8192 V to +5.7344 V	0 V to 5 V	0.5 V to 4.5 V	100 µV	Unsigned 16 bits	±250 µV p-p	14 bits
3 kHz	–0.8192 V to +5.7344 V	0 V to 5 V	0.5 V to 4.5 V	100 µV	Unsigned 16 bits	±150 µV p-p	14 bits
2 kHz	–0.8192 V to +5.7344 V	0 V to 5 V	0.5 V to 4.5 V	100 µV	Unsigned 16 bits	±100 µV p-p	15 bits
1 kHz	–0.8192 V to +5.7344 V	0 V to 5 V	0.5 V to 4.5 V	100 µV	Unsigned 16 bits	±100 µV p-p	15 bits
422 Hz	–0.8192 V to +5.7344 V	0 V to 5 V	0.5 V to 4.5 V	100 µV	Unsigned 16 bits	±100 µV p-p	15 bits
26 Hz (Filtered)	–0.8192 V to +5.7344 V	0 V to 5 V	0.5 V to 4.5 V	100 µV	Unsigned 16 bits	±50 µV p-p	16 bits

1. Negative readings are rounded to 0 V.
2. Precision range is the range over which the noise is less than the maximum noise.
3. Noise free resolution is a measure of the noise level within the precision range.

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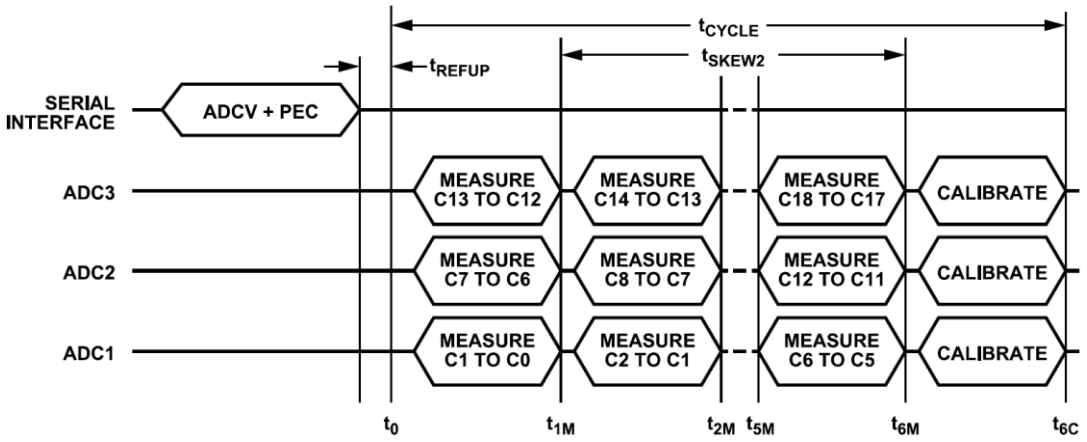

Figure 16. Timing for ADCV Command Measuring all 18 Cells

Table 5. Conversion and Synchronization Times for ADCV Command Measuring All 18 Cells in Different Modes

	Conversion Times (μs)						Synchronization Time (μs)
Mode	**t_0**	**t_{1M}**	**t_{2M}**	**t_{5M}**	**t_{6M}**	**t_{6C}**	**t_{SKEW2}**
27 kHz	0	58	104	244	291	1,121	233
14 kHz	0	87	163	390	466	1,296	379
7 kHz	0	145	279	681	815	2343	670
3 kHz	0	261	512	1263	1513	3041	1252
2 kHz	0	494	977	2426	2909	4437	2415
1 kHz	0	960	1,908	4753	5702	7230	4742
422 Hz	0	1890	3770	9408	11,287	12,816	9397
26 Hz	0	29,818	59,624	149,044	178,851	201,325	149,033

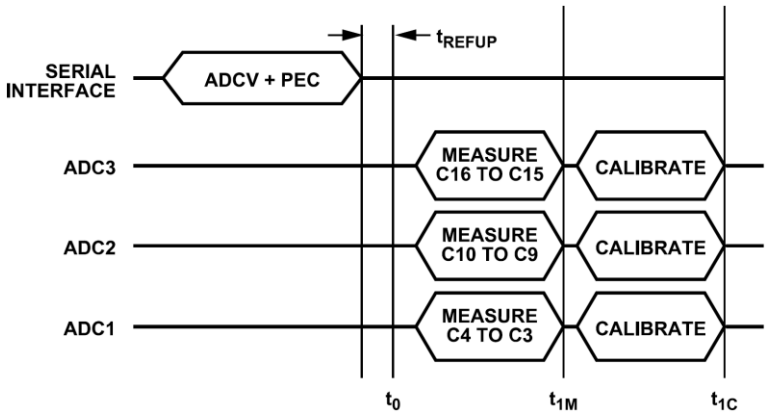

Figure 17. Timing for ADCV Command Measuring 3 Cells

Table 6 shows the conversion time for the ADCV command measuring only 3 cells. t_{1C} indicates the total conversion time for this command.

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Table 6. Conversion Times for ADCV Command Measuring 3 Cells in Different Modes

	Conversion Times (μs)		
Mode	**t_0**	**t_{1M}**	**t_{1C}**
27 kHz	0	58	203
14 kHz	0	87	232
7 kHz	0	145	407
3 kHz	0	261	523
2 kHz	0	494	756
1 kHz	0	960	1221
422 Hz	0	1890	2152
26 Hz	0	29,818	33,570

7.5.4 Undervoltage and Overvoltage Monitoring

Whenever the C inputs are measured, the results are compared to undervoltage and overvoltage thresholds stored in the memory. If the reading of a cell is above the overvoltage limit, a bit in the memory is set as a flag. Similarly, measurement results below the undervoltage limit cause a flag to be set. The overvoltage and undervoltage thresholds are stored in Configuration Register Group A. The flags are stored in Status Register Group B and Auxiliary Register Group D.

7.5.5 Auxiliary(GPIO) Measurement (ADAX Command)

The ADAX command initiates the measurement of the GPIO inputs. This command has options to select which GPIO input to measure (GPIO1 to GPIO9) and which ADC mode to use. The ADAX command also measures the 2nd reference. There are options in the ADAX command to measure subsets of the GPIOs and the 2nd reference separately or to measure all nine GPIOs and the 2nd reference in a single command. See the Commands section for the ADAX command format. All auxiliary measurements are relative to the V－ pin voltage. This command can be used to read external temperatures by connecting temperature sensors to the GPIOs. These sensors can be powered from the 2nd reference, which is also measured by the ADAX command, resulting in precise ratio metric measurements.

Figure 18 shows the timing of the ADAX command measuring all nine GPIOs and the 2nd reference. All 10 measurements are carried out on ADC1 alone. The 2nd reference is measured after GPIO5 and before GPIO6. Table 7 shows the conversion time for the ADAX command measuring all nine GPIOs and the 2nd reference. t_{10C} indicates the total conversion time.

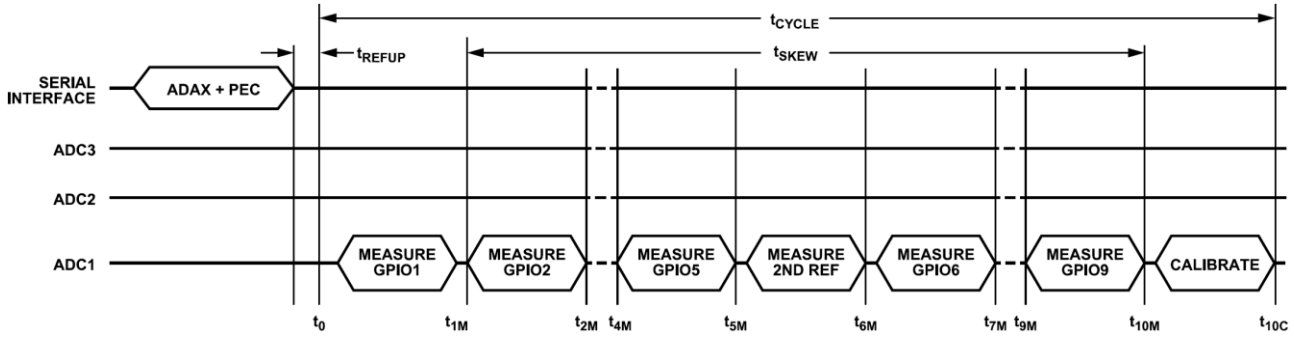

Figure 18. Timing for ADAX Command Measuring All GPIOs and 2nd Reference

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Table 7. Conversion and Synchronization Times for ADAX Command Measuring All GPIOs and 2nd Reference in Different Modes

	Conversion Times (µs)						Synchronization Time (µs)
Mode	**t_0**	**t_{1M}**	**t_{2M}**	**t_{9M}**	**t_{10M}**	**t_{10C}**	**t_{SKEW}**
27 kHz	0	58	104	431	478	1825	420
14 kHz	0	87	163	693	769	2116	682
7 kHz	0	145	279	1217	1350	3862	1205
3 kHz	0	261	512	2264	2514	5025	2253
2 kHz	0	494	977	4358	4841	7353	4347
1 kHz	0	960	1908	8547	9496	12,007	8536
422 Hz	0	1890	3770	16,926	18,805	21,316	16,915
26 Hz	0	29,818	59,624	268,271	298,078	335,498	268,260

7.5.6 Auxiliary(GPIO) Measurement with Digital Redundancy (ADAXD Command)

The ADAXD command operates similarly to the ADAX command except that an additional diagnostic is performed using digital redundancy. PS, Bits[1:0] in Configuration Register Group B must be set to 0 or 1 during the ADAXD command to enable redundancy. See the ADC Conversion with Digital Redundancy section.

The execution time of the ADAX command and the ADAXD command is the same.

7.5.7 Measuring Cell Voltages and GPIOs (ADCVAX Command)

The ADCVAX command combines 18 cell measurements with 2 GPIO measurements (GPIO1 and GPIO2). This command simplifies the synchronization of battery cell voltage and current measurements when current sensors are connected to the GPIO1 or GPIO2 inputs. Figure 19 shows the timing of the ADCVAX command. See the *Commands* section for the ADCVAX command format. The synchronization of the current and voltage measurements, t_{SKEW1}, in fast mode is within 194 µs.

Table 8 shows the conversion and synchronization time for the ADCVAX command in different modes. The total conversion time for the command is given by t_{8C}.

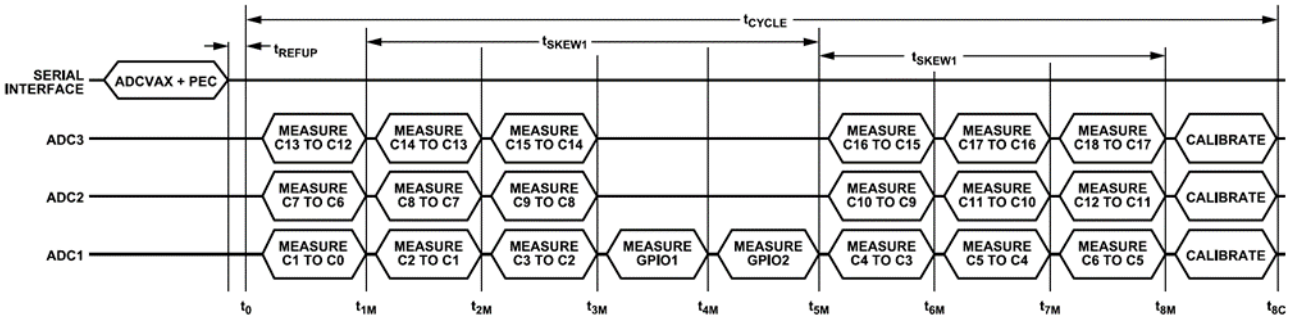

Figure 19. Timing of ADCVAX Command

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Table 8. Conversion and Synchronization Times for ADCVAX Command in Different Modes

	Conversion Times (µs)										Synchronization Time (µs)
Mode	t_0	t_{1M}	t_{2M}	t_{3M}	t_{4M}	t_{5M}	t_{6M}	t_{7M}	t_{8M}	t_{8C}	t_{SKEW1}
27 kHz	0	58	104	151	205	252	306	352	399	1511	194
14 kHz	0	87	163	238	321	397	480	556	632	1744	310
7 kHz	0	145	279	413	554	688	829	963	1097	3140	543
3 kHz	0	261	512	762	1020	1270	1527	1778	2028	4071	1008
2 kHz	0	494	977	1460	1,950	2433	2924	3407	3890	5933	1939
1 kHz	0	960	1908	2857	3812	4761	5717	6665	7613	9657	3801
422 Hz	0	1890	3770	5649	7536	9415	11,302	13,181	15,061	17,104	7525
26 Hz	0	29,818	59,624	89,431	119,245	149,052	178,866	208,672	238,479	268,450	119,234

7.6 Data Acquisition System Diagnostics

The battery monitoring data acquisition system is comprised of the multiplexers, ADCs, 1st reference, digital filters, and memory. To ensure long term reliable performance, there are several diagnostic commands that can be used to verify the proper operation of these circuits.

7.6.1 Measuring Internal Device Parameters (ADSTAT Command)

The ADSTAT command is a diagnostic command that measures the following internal device parameters: Sum of all cells (SC), internal die temperature (ITMP), analog power supply (VA), and digital power supply (VD). These parameters are described in *Sum of All Cells Measurement* section, *Internal Die Temperature Measurement* section, and *Power Supply Measurement* section. All 8 ADC modes described in the *ADC Mode* section are available for these conversions. See the *Commands* section for the ADSTAT command format. Figure 20 shows the timing of the ADSTAT command measuring all 4 internal device parameters.

Table 9 shows the conversion time of the ADSTAT command measuring all 4 internal parameters. t_{4C} indicates the total conversion time for the ADSTAT command.

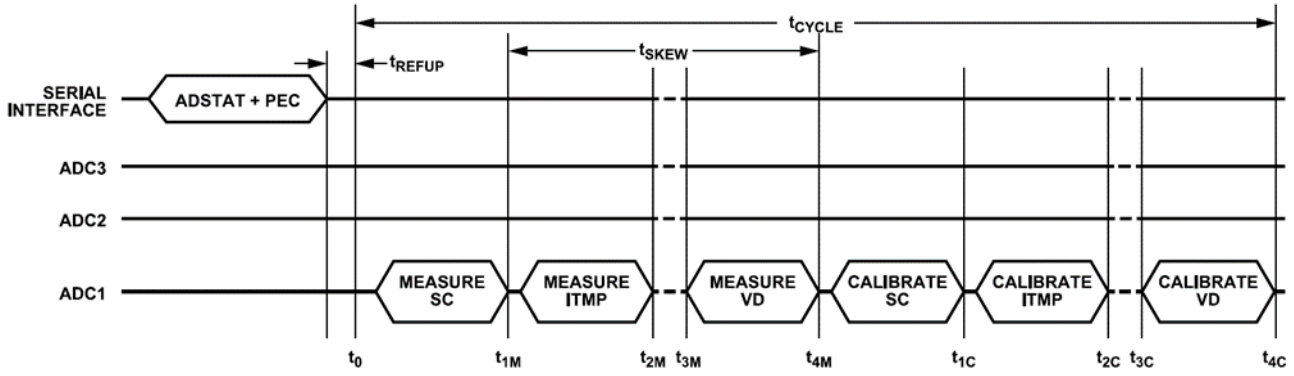

Figure 20. Timing for ADSTAT Command Measuring SC, ITMP, VA, and VD

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Table 9. Conversion and Synchronization Times for ADSTAT Command Measuring SC, ITMP, VA, and VD in Different Modes

	Conversion Times (µs)						Synchronization Time (µs)
Mode	t_0	t_{1M}	t_{2M}	t_{3M}	t_{4M}	t_{4C}	t_{SKEW}
27 kHz	0	58	104	151	198	742	140
14 kHz	0	87	163	238	314	858	227
7 kHz	0	145	279	413	547	1556	402
3 kHz	0	261	512	762	1012	2022	751
2 kHz	0	494	977	1460	1943	2953	1449
1 kHz	0	960	1908	2857	3805	4814	2845
422 Hz	0	1890	3770	5649	7529	8538	5638
26 Hz	0	29,818	59,624	89,431	119,238	134,211	89,420

7.6.2 Sum of All Cells Measurement

The sum of all cells (SC) measurement is the voltage between C18 and C0 with a 30:1 attenuation. The 16-bit ADC value of sum of all cells measurement is stored in Status Register Group A. Any potential difference between the C0 and V– pins results in an error in the SC measurement equal to this difference. From the SC value, the sum of all cell voltage measurements is given by:

$$\text{Sum of all cells} = SC \times 30 \times 100\ \mu V \tag{2}$$

7.6.3 Internal Die Temperature Measurement

The ADSTAT command can measure the internal die temperature (ITMP). The 16-bit ADC value of the ITMP is stored in Status Register Group A. From ITMP, the actual die temperature is calculated using the expression:

$$\text{Internal Die Temperature } (°C) = ITMP \times (100\mu V / (7.6mV))°C - 276°C \tag{3}$$

7.6.4 Power Supply Measurement

The ADSTAT command is also used to measure the analog power supply (V_{REG}) and digital power supply (V_{REGD}). The 16-bit ADC value of the analog power supply measurement (VA) is stored in Status Register Group A. The 16-bit ADC value of the digital power supply measurement (VD) is stored in Status Register Group B. From VA and VD, the power supply measurements are given by:

$$\text{Analog power supply measurement } (V_{REG}) = VA \times 100\mu V \tag{4}$$

$$\text{Digital power supply measurement } (V_{REGD}) = VD \times 100\mu V \tag{5}$$

The value of V_{REG} is determined by external components. V_{REG} must be between 4.5 V and 5.5 V to maintain accuracy. The value of V_{REGD} is determined by internal components. The normal range of V_{REGD} is 2.7 V to 3.6 V.

7.6.5 Measuring Internal Device Parameters with Digital Redundancy (ADSTATD Command)

The ADSTATD command operates similarly to the ADSTAT command except that an additional diagnostic is performed using digital redundancy. PS, Bits[1:0] in Configuration Register Group B must be set to 0 or 1 during

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the ADSTATD command to enable redundancy. See the *ADC Conversion with Digital Redundancy* section.

The execution time of the ADSTAT command and the ADSTATD command is the same.

7.6.6 ADC Conversion with Digital Redundancy

Each of the three internal ADCs contains its own digital integration and differentiation machine. The GD30BM1018 also contains a fourth digital integration and differentiation machine that is used for redundancy and error checking.

All of the ADC and self test commands, except ADAX and ADSTAT, can operate with digital redundancy. This includes ADCV, ADOW, CVST, ADOL, ADAXD, AXOW, AXST, ADSTATD, STATST, ADCVAX, and ADCVSC. When performing an ADC conversion with redundancy, the analog modulator sends its bit stream to both the primary digital machine and the redundant digital machine. At the end of the conversion, the results from the two machines are compared. If any mismatch occurs, a value of 0xFF0X (≥6.528 V) is written to the result register. This value is outside of the clamping range of the ADC and the host identifies this as a fault indication. The last four bits are used to indicate which nibble(s) of the result values did not match.

Table 10. Indication of Digital Redundancy Fault Bit Location

Result	Indication
0b1111_1111_0000_0XXX	No fault detected in Bit 15 to Bit 12
0b1111_1111_0000_1XXX	Fault detected in Bit 15 to Bit 12
0b1111_1111_0000_X0XX	No fault detected in Bit 11 to Bit 8
0b1111_1111_0000_X1XX	Fault detected in Bit 11 to Bit 8
0b1111_1111_0000_XX0X	No fault detected in Bit 7 to Bit 4
0b1111_1111_0000_XX1X	Fault detected in Bit 7 to Bit 4
0b1111_1111_0000_XXX0	No fault detected in Bit 3 to Bit 0
0b1111_1111_0000_XXX1	Fault detected in Bit 3 to Bit 0

Because there is a single redundant digital machine, the machine can apply redundancy to only one ADC at a time. By default, the GD30BM1018 automatically selects the ADC path redundancy. However, the user can choose an ADC redundancy path selection by writing to the PS, Bits[1:0] in Configuration Register Group B.

Table 11 shows all possible ADC path redundancy selections.

When the FDRF bit in Configuration Register Group B is written to 1, this bit forces the digital redundancy comparison to fail during subsequent ADC conversions.

7.6.7 Measuring Cell Voltages and Sum of All Cells (ADCVSC Command)

The ADCVSC command combines 18 cell measurements and the sum of all cells measurement. This command simplifies the synchronization of the individual battery cell voltage and the total sum of all cells measurements. Figure 21 shows the timing of the ADCVSC command. See the *Commands* section for the ADCVSC command format. The synchronization of the cell voltage and sum of all cells measurements, t_{SKEW}, in fast mode is within 147 µs.

Table 12 shows the conversion and synchronization time for the ADCVSC command in different modes. The total conversion time for the command is given by t_{7C}.

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Table 11. ADC Path Redundancy Selection

	PS, Bits[1:0] = 00		PS, Bits[1:0] = 01		PS, Bits[1:0] = 10		PS, Bits[1:0] = 11	
		Redundant		Redundant		Redundant		Redundant
Measure	Path Select	Measure	Path Select	Measure	Path Select	Measure	Path Select	Measure
Cells 1, 7, 13	ADC1	Cell 1	ADC1	Cell 1	ADC2	Cell 7	ADC3	Cell 13
Cells 2, 8, 14	ADC2	Cell 8	ADC1	Cell 2	ADC2	Cell 8	ADC3	Cell 14
Cells 3, 9, 15	ADC3	Cell 15	ADC1	Cell 3	ADC2	Cell 9	ADC3	Cell 15
Cells 4, 10, 16	ADC1	Cell 4	ADC1	Cell 4	ADC2	Cell 10	ADC3	Cell 16
Cells 5, 11, 17	ADC2	Cell 11	ADC1	Cell 5	ADC2	Cell 11	ADC3	Cell 17
Cells 6, 12, 18	ADC3	Cell 18	ADC1	Cell 6	ADC2	Cell 12	ADC3	Cell 18
Cell 7 (ADOL)	ADC2	Cell 7	ADC1	Cell 7	ADC2	Cell 7	ADC3	N/A 1
Cell 13 (ADOL)	ADC2	Cell 13	ADC1	N/A1	ADC2	Cell 13	ADC3	Cell 13
GPIO[n]2	ADC1	GPIO[n]	ADC1	GPIO[n]	ADC2	N/A1	ADC3	N/A 1
2nd Reference[2]	ADC1	2nd Reference	ADC1	2nd Reference	ADC2	N/A1	ADC3	N/A 1
SC2	ADC1	SC	ADC1	SC	ADC2	N/A1	ADC3	N/A 1
ITMP2	ADC1	ITMP	ADC1	ITMP	ADC2	N/A1	ADC3	N/A 1
VA2	ADC1	VA	ADC1	VA	ADC2	N/A1	ADC3	N/A 1
VD 2	ADC1	VD	ADC1	VD	ADC2	N/A1	ADC3	N/A 1

1. N/A means not applicable.
2. Note that the ADAX and ADSTAT commands are identical to the ADAXD and ADSTATD commands except that ADAX and ADSTAT do not apply any digital redundancy.

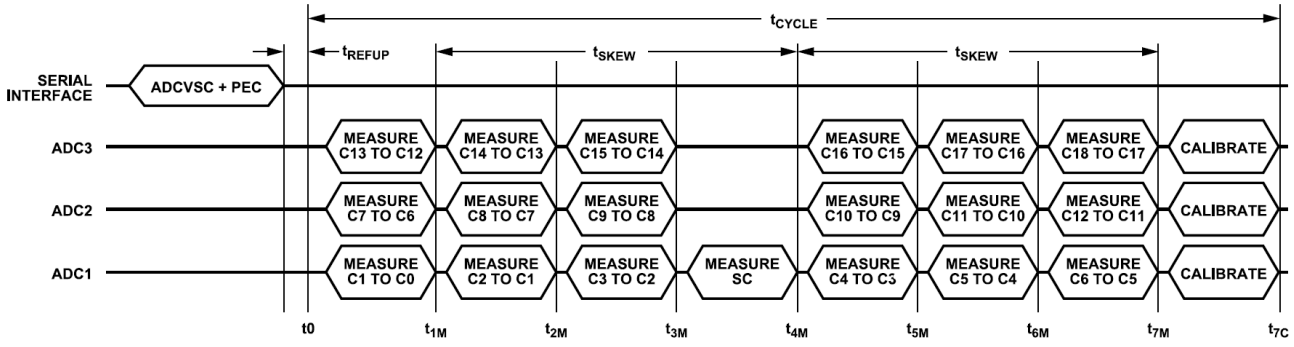

Figure 21. Timing of ADCVSC Command Measuring All 19 Cells, SC

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Table 12. Conversion and Synchronization Times for ADCVSC Command in Different Modes

	Conversion Times (µs)									Synchronization Time (µs)
Mode	**t_0**	**t_{1M}**	**t_{2M}**	**t_{3M}**	**t_{4M}**	**t_{5M}**	**t_{6M}**	**t_{7M}**	**t_{7C}**	**t_{SKEW}**
27 kHz	0	58	104	151	205	259	306	352	1331	147
14 kHz	0	87	163	238	321	404	480	556	1534	235
7 kHz	0	145	279	413	554	695	829	963	2756	409
3 kHz	0	261	512	762	1020	1277	1527	1778	3571	758
2 kHz	0	494	977	1460	1950	2441	2924	3407	5200	1456
1 kHz	0	960	1908	2857	3812	4768	5717	6665	8458	2853
422 Hz	0	1890	3770	5649	7536	9423	11,302	13,181	14,974	5645
26 Hz	0	29,818	59,624	89,431	119,245	149,059	178,866	208,672	234,902	89,427

7.6.8 Overlap Cell Measurement (ADOL Command)

The ADOL command first simultaneously measures Cell 7 with ADC1 and ADC2. Then, the ADOL command simultaneously measures Cell 13 with both ADC2 and ADC3. The host can compare the results against each other to look for inconsistencies that may indicate a fault. The result of the Cell 7 measurement from ADC2 is placed in Cell Voltage Register Group C where the Cell 7 result normally resides. The result from ADC1 is placed in Cell Voltage Register Group C where the Cell 8 result normally resides. The result of the Cell 13 measurement from ADC3 is placed in Cell Voltage Register Group E where the Cell 13 result normally resides. The result from ADC2 is placed in Cell Voltage Register Group E where the Cell 14 result normally resides. Figure 22 shows the timing of the ADOL command. See the *Commands* section for the ADOL command format.

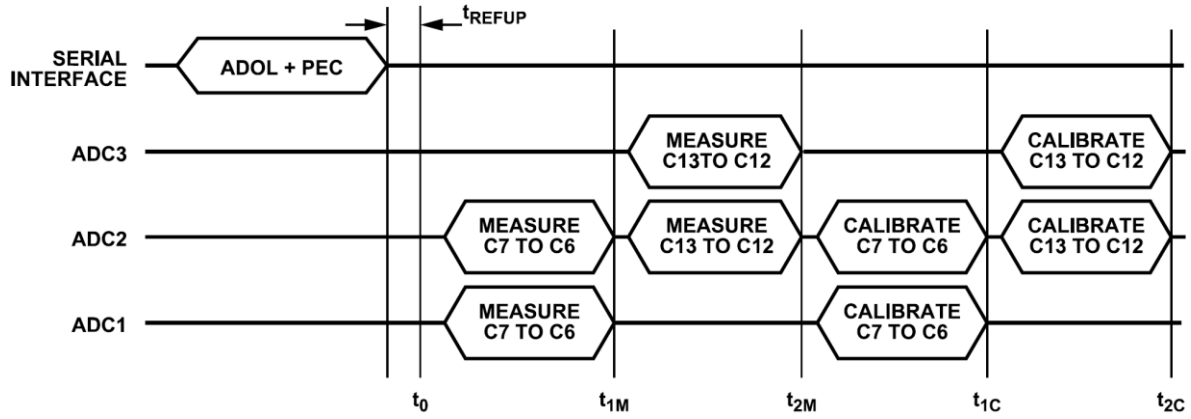

Figure 22. Timing for ADOL Command

Table 13 shows the conversion time for the ADOL command. t2C indicates the total conversion time for this command.

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Table 13. Conversion Times for ADOL Command

	Conversion Times (μs)			
Mode	**t_0**	**t_{1M}**	**t_{2M}**	**t_{2C}**
27 kHz	0	58	106	384
14 kHz	0	87	164	442
7 kHz	0	146	281	791
3 kHz	0	262	513	1024
2 kHz	0	495	979	1490
1 kHz	0	960	1910	2420
422 Hz	0	1891	3772	4282
26 Hz	0	29,818	59,626	67,119

7.6.9 Digital Filter Check

The Δ-Σ ADC is composed of a 1-bit pulse density modulator followed by a digital filter. A pulse density modulated bit stream has a higher percentage of 1s for higher analog input voltages. The digital filter converts this high frequency 1-bit stream into a single 16-bit word.

This is why a Δ-Σ ADC is often referred to as an oversampling converter.

The self test commands verify the operation of the digital filters and memory. Figure 23 shows the operation of the ADC during self test. The output of the 1-bit pulse density modulator is replaced by a 1-bit test signal. The test signal passes through the digital filter and is converted to a 16-bit value. The 1-bit test signal undergoes the same digital conversion as the regular 1-bit signal from the modulator, so the conversion time for any self test command is exactly the same as the corresponding regular ADC conversion command. The 16-bit ADC value is stored in the same register groups as the corresponding regular ADC conversion command. The test signals are designed to place alternating one-zero patterns in the registers. Table 14 provides a list of the self test commands. If the digital filters and memory are working properly, then the registers contain the values shown in Table 14. For more details see the *Commands* section.

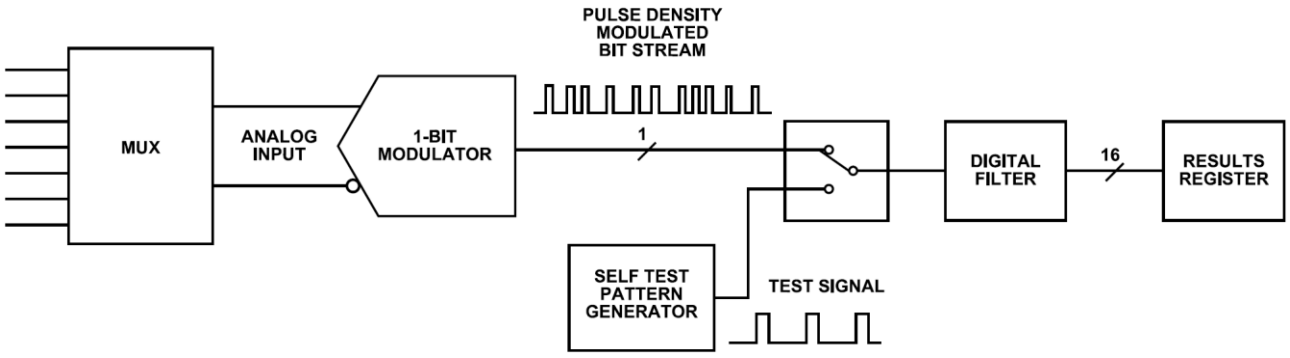

Figure 23. Operation of GD30BM1018 ADC Self Test

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Table 14. Self Test Command Summary

		Output Pattern in Different ADC Modes			
Command	**Self Test Option**	**27 kHz**	**14 kHz**	**7 kHz, 3 kHz, 2 kHz, 1 kHz, 422 Hz, 26 Hz**	**Results Register Groups**
CVST	ST, Bits[1:0] = 01 ST, Bits[1:0] = 10	0x9565 0x6A9A	0x9553 0x6AAC	0x9555 0x6AAA	C1V to C18V (CVA, CVB, CVC, CVD, CVE, CVF)
AXST	ST, Bits[1:0] = 01 ST, Bits[1:0] = 10	0x9565 0x6A9A	0x9553 0x6AAC	0x9555 0x6AAA	G1V to GV9, REF (AUXA, AUXB, AUXC, AUXD)
STATST	ST, Bits[1:0] = 01 ST, Bits[1:0] = 10	0x9565 0x6A9A	0x9553 0x6AAC	0x9555 0x6AAA	SC, ITMP, VA, VD (STATA, STATB)

7.6.10 Accuracy Check

Measuring an independent voltage reference is the optimal means to verify the accuracy of a data acquisition system. The GD30BM1018 contains a 2nd reference for this purpose. The ADAX command initiates the measurement of the 2nd reference. The results are placed in Auxiliary Register Group B. The range of the result depends on the ADC1 measurement accuracy and the accuracy of the 2nd reference, including thermal hysteresis and long term drift. Readings outside the 2.992 V to 3.012 V range indicate the system is out of its specified tolerance. ADC2 is verified by comparing it to ADC1 using the ADOL command. ADC3 is verified by comparing it to ADC2 using the ADOL command.

7.6.11 Mux Decoder Check

The diagnostic command DIAGN ensures the proper operation of each multiplexer channel. The command cycles through all channels and sets the MUXFAIL bit to 1 in Status Register Group Bif any channel decoder fails. The MUXFAIL bit is set to 0 if the channel decoder passes the test. The MUXFAIL bit is also set to 1 on a power-on reset (POR) or after a CLRSTAT command.

The DIAGN command takes approximately 400 µs to complete if the core is in the REFUP state and about 4.5 ms to complete if the core is in the standby state. The polling methods described in the *Polling Methods* section can be used to determine the completion of the DIAGN command.

7.6.12 ADC Clear Commands

GD30BM1018 has 3 clear ADC commands: CLRCELL, CLRAUX, and CLRSTAT. These commands clear the registers that store all ADC conversion results.

The CLRCELL command clears Cell Voltage Register Groups A, B, C, D, E, and F. All bytes in these registers are set to 0xFF by the CLRCELL command.

The CLRAUX command clears Auxiliary Register Groups A, B, C, and D. All bytes in these registers, except the last four registers of Group D, are set to 0xFF by the CLRAUX command.

The CLRSTAT command clears Status Register Groups A and B, except for the REV and RSVD bits in Status Register Group B. A read back of the REV bits returns the revision code of the part. RSVD bits always read back 0s. All overvoltage (OV) and undervoltage (UV) flags, MUXFAIL bit, and THSD bit in Status Register Group B and

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Auxiliary Register Group D are set to 1 by the CLRSTAT command. The THSD bit is set to 0 after the RDSTATB command. The registers storing SC, I TMP, VA, and VD are all set to 0xFF by the CLRSTAT command.

7.6.13 Open Wire Check (ADOW Command)

The ADOW command is used to check for any open wires between the ADCs of the GD30BM1018 and the external cells. This command performs ADC conversions on the C pin inputs identically to the ADCV command, except for two internal current sources sink or source current into the two C pins while they are being measured. The pull-up (PUP) bit of the ADOW command determines whether the current sources are sinking or sourcing 100 µA.

The following simple algorithm can be used to check for an open wire on any of the 19 C pins:

1. Run the 18-cell command ADOW with PUP = 1 at least twice. Read the cell voltages for cells 1 through 18 once at the end and store them in array $CELL_{PU}(n)$.
2. Run the 18-cell command ADOW with PUP = 0 at least twice. Read the cell voltages for cells 1 through 18 once at the end and store them in array $CELL_{PD}(n)$.
3. Take the difference between the pull-up and pull-down measurements made in Step 1 and Step 2 for cells 2 to 18: $CELL_{\Delta}(n) = CELL_{PU}(n) – CELL_{PD}(n)$.
4. For all values of n from 1 to 17: If $CELL_{\Delta}(n+1) < –400$ mV, then C(n) is open. If $CELL_{PU}(1) = 0.0000$, then C(0) is open. If $CELL_{PD}(18) = 0.0000$, then C(18) is open.

The above algorithm detects open wires using normal mode conversions with as much as 10 nF of capacitance remaining on the GD30BM1018 side of the open wire. However, if more external capacitance is on the open C pin, then the length of time that the open wire conversions run in Step 1 and Step 2 must be increased to give the 100 µA current sources time to create a large enough difference for the algorithm to detect an open connection. This action can be accomplished by running more than two ADOW commands in Step 1 and Step 2, or by using filtered mode conversions instead of normal mode conversions. Refer to Table 15 to determine how many conversions are necessary.

Table 15. Number of ADOW Commands Required

	Number of ADOW Commands Required in Step 1 and Step 2	
External C Pin Capacitance	**Normal Mode**	**Filtered Mode**
≤10 nF	2	2
100 nF	10	2
1 µF	100	2
C	1 + ROUNDUP (C/10 nF)	2

7.6.14 Auxiliary Open Wire Check (AXOW Command)

The AXOW command is used to check for any open wires between the GPIO pins of the GD30BM1018 and the external circuit. This command performs ADC conversions on the GPIO pin inputs identically to the ADAX command, except internal current sources sink or source current into each GPIO pin while it is being measured. The pull-up (PUP) bit of the AXOW command determines whether the current sources are sinking or sourcing 100 µA.

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7.6.15 Thermal Shutdown

To protect the GD30BM1018 from overheating, there is a thermal shutdown circuit included inside the IC. If the temperature detected on the die rises above approximately 150°C, the thermal shutdown circuit trips and resets the configuration register groups and S Control Register Group (including S control bits in PWM/S Control Register Group B) to their default states and turns off all discharge switches. When a thermal shutdown event has occurred, the THSD bit in Status Register Group B goes high. The CLRSTAT command can also set the THSD bit high for diagnostic purposes. This bit is cleared when a read operation is performed on Status Register Group B (RDSTATB command). The CLRSTAT command sets the THSD bit high for diagnostic purposes but does not reset the configuration register groups.

7.6.16 Revision Code

The Status Register Group B contains a 4-bit revision code (REV). If software detection of the device revision is necessary, contact the factory for details. Otherwise, ignore the code. In all cases, however, the values of all bits must be used when calculating the packet error code (PEC) on data reads.

7.7 Watchdog and Discharge Timer

When there is no valid command for more than 2 seconds, the watchdog timer expires, which resets the configuration register bytes CFGAR0-3 and the GPIO bits in Configuration Register Group B in all cases. CFGAR4, CFGAR5, the S Control Register Group (including S control bits in PWM/S Control Register Group B) and the remainder of Configuration Register Group B are reset by the watchdog timer when the discharge timer is disabled. The WDT pin is pulled high by the external pull-up when the watchdog time elapses. The watchdog timer is always enabled, and the timer resets after every valid command with matching command PEC.

The discharge timer is used to keep the discharge switches turned on for programmable time duration. If the discharge timer is being used, the discharge switches are not turned off when the watchdog timer is activated.

To enable the discharge timer, connect the DTEN pin to V_{REG} (see Figure 24). In this configuration, the discharge switches remain on for the programmed time duration that is determined by the DCTO value written in Configuration Register Group A. Table 17 shows the various time settings and the corresponding DCTO value.

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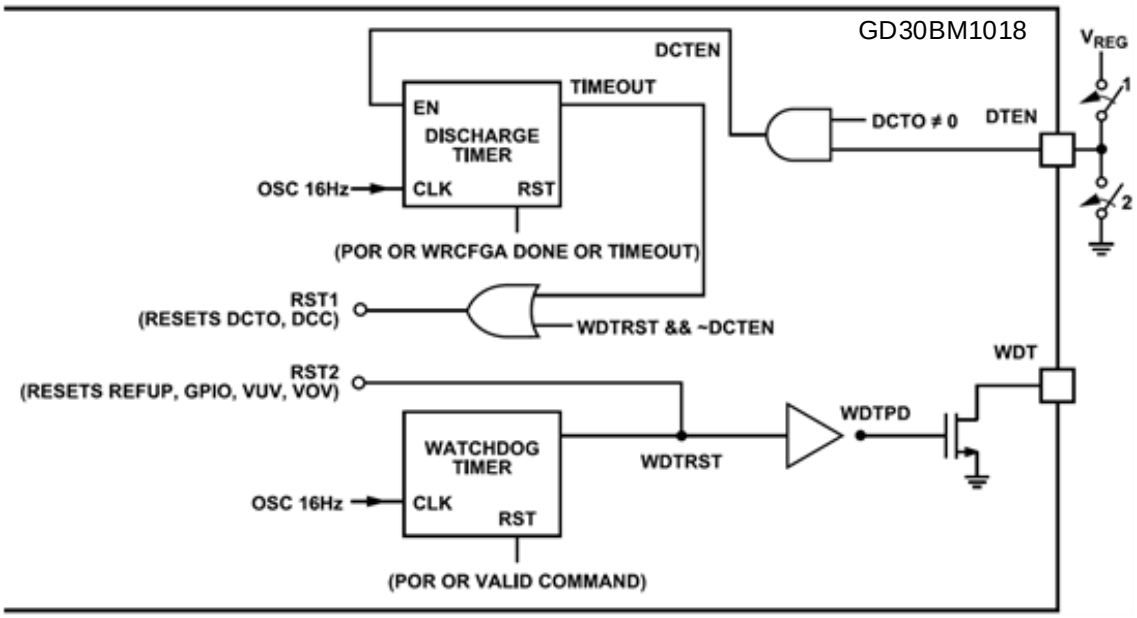

Figure 24. Watchdog and Discharge Timer

Table 16. DCTO Settings

DCTO	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
Time (Minutes)	Disabled	0.5	1	2	3	4	5	10	15	20	30	40	60	75	90	120

Table 17. Discharge Timer Settings

	Watchdog Timer	Discharge Timer
DTEN = 0, DCTO = XXXX	Resets CFGAR0-5, CFGBR0-1 and SCTRL when it fires	Disabled
DTEN = 1, DCTO = 0000	Resets CFGAR0-5, CFGBR0-1 and SCTRL when it fires	Disabled
DTEN = 1, DCTO = 0000	Resets CFGAR0-3 and GPIO Bits in CFGBR0 when it fires	Resets CFGAR4-5, SCTRL, and remainder of CFGBR0-1 when it fires

Table 17 summarizes the status of the configuration register groups after a watchdog timer or discharge timer event. The status of the discharge timer can be determined by reading Configuration Register Group A using the RDCFGA command. The DCTO value indicates the time left before the discharge timer expires, as shown in Table 18.

Table 18. Status of the Discharge Timer

DCTO (Read Value)	Discharge Timer Left (Minutes)
0	Disabled (or) timer has timed out
1	0 < timer ≤ 0.5
2	0.5 < timer ≤ 1
3	1 < timer ≤ 2
4	2 < timer ≤ 3
5	3 < timer ≤ 4
6	4 < timer ≤ 5

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DCTO (Read Value)	Discharge Timer Left (Minutes)
7	5 < timer ≤ 10
8	10 < timer ≤ 15
9	15 < timer ≤ 20
A	20 < timer ≤ 30
B	30 < timer ≤ 40
C	40 < timer ≤ 60
D	60 < timer ≤ 75
E	75 < timer ≤ 90
F	90 < timer ≤ 120

Unlike the watchdog timer, the discharge timer does not reset when there is a valid command. The discharge timer can only be reset after a valid WRCFGA (Write Configuration Register Group A) command. There is a possibility that the discharge timer expires in the middle of some commands.

If the discharge timer activates in the middle of a WRCFGA command, the configuration register groups and S Control Register Group (including S control bits in PWM/S Control Register Group B) reset as per Table 17. However, at the end of the valid WRCFGA command, the new data is copied to Configuration Register Group A. The new configuration data is not lost when the discharge timer is activated.

If the discharge timer activates in the middle of an RDCFGA or RDCFGB command, the configuration register groups reset as per Table 17. As a result, the read back data from bytes CFGAR4 and CFGAR5 and CFGBR0 and CFGBR1 may be corrupted. If the discharge timer activates in the middle of a RDSCTRL or RDPSB command, the S Control Register Group (including S control bits in PWM/S Control Register Group B) resets, as per Table 17. As a result, the read back data may be corrupted.

7.8 S Pin Pulse-Width Modulation for Cell Balancing

For additional control of cell discharging, the host may configure the S pins to operate using PWM. While the watchdog timer is not expired, the DCC bits in the configuration register groups control the S pins directly. After the watchdog timer expires, PWM operation begins and continues for the remainder of the selected discharge time or until a wake-up event occurs (and the watchdog timer is reset). During PWM operation, the DCC bits must be set to 1 for the PWM feature to operate.

Once PWM operation begins, the configurations in the PWM register can cause some or all S pins to be periodically deasserted to achieve the desired duty cycle as shown in Table 19. Each PWM signal operates on a 30 second period. For each cycle, the duty cycle can be programmed from 0% to 100% in increments of 1/15 = 6.67% (2 seconds).

Each S pin PWM signal is sequenced at different intervals to ensure that no two pins switch on or off at the same time. The switching interval between channels is 62.5 ms, and 1.125 sec is required for all 18 pins to switch (18 × 62.5 ms).

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Table 19. S Pin Pulse-Width Modulation Settings

DCC Bit (Configuration Register Groups)	PWMC Setting	On Time (sec)	Off Time (sec)	Duty Cycle (%)
0	4'bXXXX	0	Continuously Off	0
1	4'b1111	Continuously On	0	100.0
1	4'b1110	28	2	93.3
1	4'b1101	26	4	86.7
1	4'b1100	24	6	80.0
1	4'b1011	22	8	73.3
1	4'b1010	20	10	66.7
1	4'b1001	18	12	60.0
1	4'b1000	16	14	53.3
1	4'b0111	14	16	46.7
1	4'b0110	12	18	40.0
1	4'b0101	10	20	33.3
1	4'b0100	8	22	26.7
1	4'b0011	6	24	20.0
1	4'b0010	4	26	13.3
1	4'b0001	2	28	6.7
1	4'b0000	0	Continuously Off	0

The default values of the PWM control settings (located in PWM Register Group and PWM/S Control Register Group B) are all 1s. Upon entering sleep mode, the PWM control settings are initialized to their default values.

7.9 Discharge Timer Monitor

The GD30BM1018 has the ability to periodically monitor cell voltages while the discharge timer is active. The host writes the DTMEN bit in Configuration Register Group B to 1 to enable this feature.

When the discharge timer monitor is enabled and the watchdog timer has expired, the GD30BM1018 performs a conversion of all cell voltages in 7 kHz (normal) mode every 30 seconds. The overvoltage and undervoltage comparisons are performed and flags are set if cells have crossed a threshold. For any undervoltage cells, the discharge timer monitor automatically clears the associated DCC bit in Configuration Register Group A or Configuration Register Group B so that the cell is no longer discharged. Clearing the DCC bit also disables PWM discharge. With this feature, the host can write the undervoltage threshold to the desired discharge level and use the discharge timer monitor to discharge all, or selected, cells (using either constant discharge or PWM discharge) down to that level.

During discharge timer monitoring, digital redundancy checking is performed on the cell voltage measurements. If a digital redundancy failure occurs, all DCC bits are cleared.

7.10 I2C/SPI Master on GD30BM1018 Using GPIOs

The I/O ports GPIO3, GPIO4, and GPIO5 on the GD30BM1018 can be used as an I2C or SPI master port to communicate to an I 2C or SPI slave. In the case of an I2C master, GPIO4 and GPIO5 form the SDA and SCL ports of the I2C interface, respectively. In the case of an SPI master, GPIO3, GPIO4, and GPIO5 are the CSBM,

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SDIOM, and SCKM ports of the SPI, respectively. The SPI master on the GD30BM1018 supports SPI Mode 3 (CHPA = 1 and CPOL = 1).

The GPIOs are open-drain outputs, so an external pull-up is required on these ports to operate as an I2C or SPI master. It is also important to write the GPIO bits to 1 in the configuration register groups so these ports are not pulled low internally by the device.

7.10.1 COMM Register

GD30BM1018 has a 6-byte COMM register, as shown in Table 20. This register stores all data and control bits required for I2C or SPI communication to a slave. The COMM register contains three bytes of data Dn, Bits[7:0] to be transmitted to or received from the slave device. ICOMn, Bits[3:0] specify control actions before transmitting/receiving each data byte. FCOMn, Bits[3:0] specify control actions after transmitting/receiving each data byte.

If ICOMn, Bit 3 in the COMM register is set to 1, the device becomes an SPI master, and if the bit is set to 0, the device becomes an I2C master.

Table 21 describes the valid write codes for ICOMn, Bits[3:0] and FCOMn, Bits[3:0] and their behavior when using the device as an I2C master.

Table 22 describes the valid write codes for ICOMn, Bits[3:0] and FCOMn, Bits[3:0] and their behavior when using the device as an SPI master.

Note that only the codes listed in Table 21 and Table 22 are valid for ICOMn, Bits[3:0] and FCOMn, Bits[3:0]. Writing any other code that is not listed in Table 21 and Table 22 to ICOMn, Bits[3:0] and FCOMn, Bits[3:0] may result in unexpected behavior on the I2C or SPI port.

Table 20. COMM Register Memory Map

Register	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
COMM0	R/W	ICOM0, Bit 3	ICOM0, Bit 2	ICOM0, Bit 1	ICOM0, Bit 0	D0, Bit 7	D0, Bit 6	D0, Bit 5	D0, Bit 4
COMM1	R/W	D0, Bit 3	D0, Bit 2	D0, Bit 1	D0, Bit 0	FCOM0, Bit 3	FCOM0, Bit 2	FCOM0, Bit 1	FCOM0, Bit 0
COMM2	R/W	ICOM1, Bit 3	ICOM1, Bit 2	ICOM1, Bit 1	ICOM1, Bit 0	D1, Bit 7	D1, Bit 6	D1, Bit 5	D1, Bit 4
COMM3	R/W	D1, Bit 3	D1, Bit 2	D1, Bit 1	D1, Bit 0	FCOM1, Bit 3	FCOM1, Bit 2	FCOM1, Bit 1	FCOM1, Bit 0
COMM4	R/W	ICOM2, Bit 3	ICOM2, Bit 2	ICOM2, Bit 1	ICOM2, Bit 0	D2, Bit 7	D2, Bit 6	D2, Bit 5	D2, Bit 4
COMM5	R/W	D2, Bit 3	D2, Bit 2	D2, Bit 1	D2, Bit 0	FCOM2, Bit 3	FCOM2, Bit 2	FCOM2, Bit 1	FCOM2, Bit 0

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Table 21. Write Codes for ICOMn, Bits[3:0] and FCOMn, Bits[3:0] on I2C Master

Control Bits	Code	Action	Description
ICOMn, Bits[3:0]	0110	Start	Generate a start signal on I2C port followed by a data transmission
	0001	Stop	Generate a stop signal on I2C port
	0000	Blank	Proceed directly to data transmission on I2C port
	0111	No transmit	Release SDA and SCL and ignore the rest of the data
FCOMn, Bits[3:0]	0000	Master ACK	Master generates an ACK Signal on ninth clock cycle
	1000	Master NACK	Master generates a NACK signal on ninth clock cycle
	1001	Master NACK + stop	Master generates a NACK signal followed by a stop signal

Table 22. Write Codes for ICOMn, Bits[3:0] and FCOMn, Bits[3:0] on SPI Master

Control Bits	Code	Action	Description
ICOMn, Bits[3:0]	1000	CSBM low	Generates a CSBM low signal on SPI port (GPIO3)
	1010	CSBM falling edge	Drives CSBM (GPIO3) high, then low
	1001	CSBM high	Generates a CSBM high signal on SPI port (GPIO3)
	1111	No transmit	Releases the SPI port and ignores the rest of the data
FCOMn, Bits[3:0]	X000	CSBM low	Holds CSBM low at the end of byte transmission
	1001	CSBM high	Transitions CSBM high at the end of byte transmission

7.10.2 COMM Commands

Three commands help accomplish I2C or SPI communication to the slave device: WRCOMM, STCOMM, and RDCOMM.

WRCOMM Command: This command is used to write data to the COMM register. This command writes 6 bytes of data to the COMM register. The PEC needs to be written at the end of the data. If the PEC does not match, all data in the COMM register is cleared to 1s when CSB goes high. See the *Bus Protocols* section for more details on a write command format.

STCOMM Command: This command initiates I2C/SPI communication on the GPIO ports. The COMM register contains 3 bytes of data to be transmitted to the slave. During this command, the data bytes stored in the COMM register are transmitted to the slave I2C or SPI device and the data received from the I2C or SPI device is stored in the COMM register. This command uses GPIO4 (SDA), and GPIO5 (SCL) for I2C communication or GPIO3 (CSBM), GPIO4 (SDIOM), and GPIO5 (SCKM) for SPI communication.

The STCOMM command is followed by 24 clock cycles for each byte of data transmitted to the slave device while holding CSB low. For example, to transmit three bytes of data to the slave, send the STCOMM command and its PEC followed by 72 clock cycles. Pull CSB high at the end of the 72 clock cycles of the STCOMM command.

During I2C or SPI communication, the data received from the slave device is updated in the COMM register.

RDCOMM Command: The data received from the slave device can be read back from the COMM register using the RDCOMM command. The command reads back six bytes of data followed by the PEC. See the *Bus Protocols* section for more details on a read command format.

Table 23 describes the possible read back codes for ICOMn, Bits[3:0] and FCOMn, Bits[3:0] when using the device as an I2C master. Dn, Bits[7:0] contain the data byte transmitted by the I2C slave.

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Table 23. Read Codes for ICOMn, Bits[3:0] and FCOMn, Bits[3:0] on I2C Master

Control Bits	Code	Description
ICOMn, Bits[3:0]	0110	Master generated a start signal
	0001	Master generated a stop signal
	0000	Blank, SDA was held low between bytes
	0111	Blank, SDA was held high between bytes
FCOMn, Bits[3:0]	0000	Master generated an ACK signal
	0111	Slave generated an ACK signal
	1111	Slave generated a NACK signal
	0001	Slave generated an ACK signal, master generated a
		stop signal
	1001	Slave generated a NACK signal, master generated a stop signal

In case of the SPI master, the read back codes for ICOMn, Bits[3:0] and FCOMn, Bits[3:0] are always 0111 and 1111, respectively. Dn, Bits[7:0] contain the data byte transmitted by the SPI slave.

Figure 25 shows the operation of GD30BM1018 as an I2C or SPI master using the GPIOs.

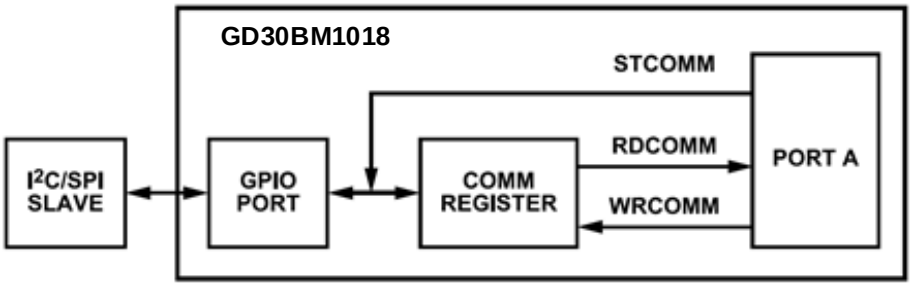

Figure 25. GD30BM1018 I2Cor SPI Master Using GPIOs

Any number of bytes can be transmitted to the slave in groups of 3 bytes using these commands. The GPIO ports do not reset between different STCOMM commands. However, if the wait time between the commands is greater than 2 sec, the watchdog times out and resets the ports to their default values.

To transmit several bytes of data using an I2C master, a start signal is only required at the beginning of the entire data stream. A stop signal is only required at the end of the data stream. All intermediate data groups can use a blank code before the data byte and an ACK/NACK signal as appropriate after the data byte. SDA and SCL do not reset between different STCOMM commands.

To transmit several bytes of data using an SPI master, a CSBM low signal is sent at the beginning of the 1st data byte. CSBM can be held low or taken high for intermediate data groups using the appropriate code on FCOMn, Bits[3:0]. A CSBM high signal is sent at the end of the last byte of data. CSBM, SDIOM, and SCKM do not reset between different STCOMM commands.

Figure 26 shows the 24 clock cycles following the STCOMM command for an I2C master in different cases. Note that if ICOMn, Bits[3:0] specified a stop condition, after the stop signal is sent, the SDA and SCL lines are held high and all data in the rest of the word is ignored. If ICOMn, Bits[3:0] are a no transmit, both SDA and SCL lines are released, and the rest of the data in the word is ignored. This is used when a particular device in the stack does not have to communicate to a slave.

Figure 27 shows the 24 clock cycles following the STCOMM command for an SPI master. Similar to the I2C

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master, if ICOMn, Bits[3:0] specified a CSBM HIGH or a no transmit condition, the CSBM, SCKM, and SDIOM lines of the SPI master are released and the rest of the data in the word is ignored.

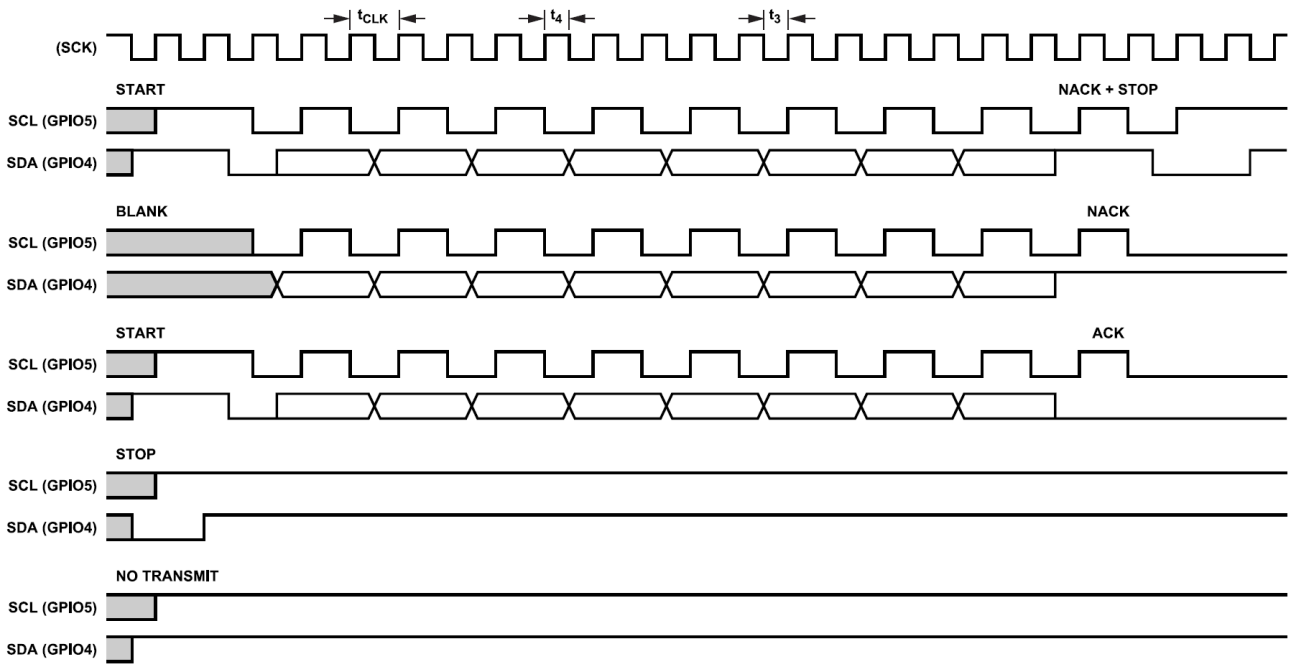

Figure 26. STCOMM Timing Diagram for an I2C Master

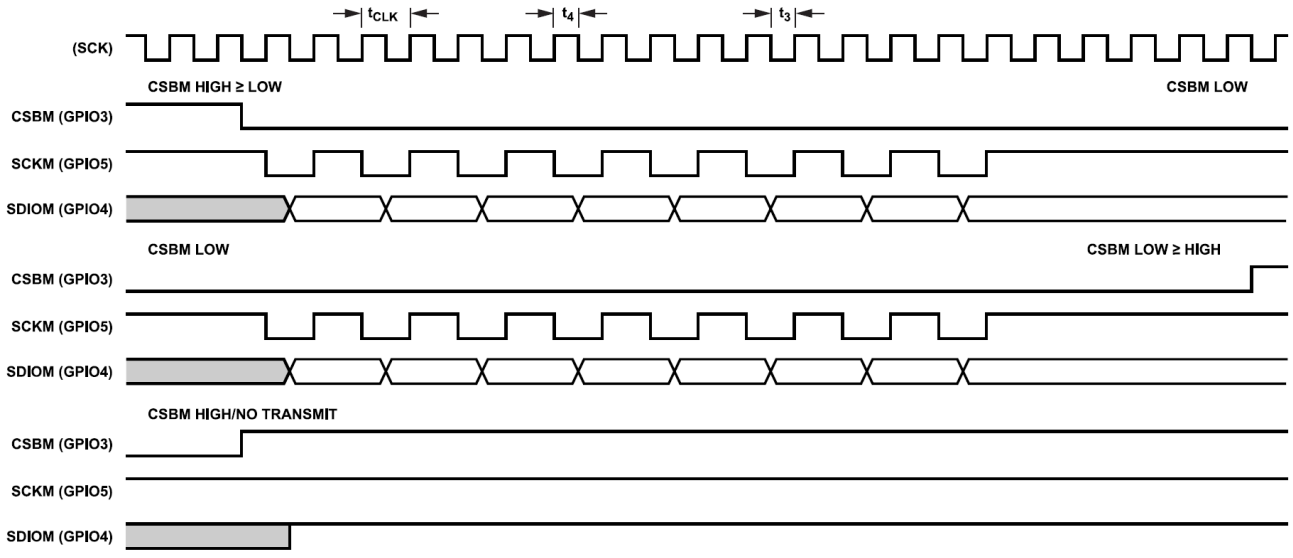

Figure 27. STCOMM Timing Diagram for an SPI Master

7.10.3 Timing Specifications of I2C and SPI Master

The timing of the GD30BM1018 I2C or SPI master is controlled by the timing of the communication at the primary SPI of the GD30BM1018. Table 24 shows the I2C master timing relationship to the primary SPI clock. Table 25 shows the SPI master timing specifications.

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Table 24. I2C Master Timing

I2C Master Parameter	Timing Relationship to Primary SPI	Timing Specifications at tCLK = 1 µs
SCL Clock Frequency	1/(2 × tCLK)	500 kHz maximum
tHD, STA	t3	200 ns minimum
tLOW	tCLK	1 µs minimum
tHIGH	tCLK	1 µs minimum
tSU, STA	tCLK + t41	1.03 µs minimum
tHD, DAT	t4	30 ns minimum
tSU, DAT	t3	200 ns minimum
tSU, STO	tCLK + t41	1.03 µs minimum
tBUF	3 × tCLK	3 µs minimum

1. When using isoSPI, t4 is generated internally and is a minimum of 30 ns. Also, t3 = tCLK – t4. When using SPI, t3 and t4 are the low and high times of the SCK input, each with a specified minimum of 200 ns.

Table 25. SPI Master Timing

SPI Master Parameter	Timing Relationship to Primary SPI	Timing Specifications at tCLK = 1 µs
SDIOM Valid to SCKM Rising Setup	t_3	200 ns minimum
SDIO Valid from SCKM Rising Hold	$t_{CLK} + t_4$[1]	1.03 µs minimum
SCKM Low	t_{CLK}	1 µs minimum
SCKM High	t_{CLK}	1 µs minimum
SCKM Period (SCKM_Low + SCKM_High)	2 × t_{CLK}	2 µs minimum
CSBM Pulse Width	3 × t_{CLK}	3 µs minimum
SCKM Rising to CSBM Rising	5 × $t_{CLK} + t_4$[1]	5.03 µs minimum
CSBM Falling to SCKM Falling	t_3	200 ns minimum
CSBM Falling to SCKM Rising	$t_{CLK} + t_3$	1.2 µs minimum
SCKM Falling to SDIOM Valid	Master Requires < t_{CLK}	

1. When using isoSPI, t4 is generated internally and is a minimum of 30 ns. Also, t3 = tCLK – t4. When using SPI, t3 and t4 are the low and high times of the SCK input, each with a specified minimum of 200 ns.

7.11 S Pin Muting

The S pins can be disabled by sending the mute command and reenabled by sending the unmute command. The mute and unmute commands do not require any subsequent data and thus the commands propagate quickly through a stack of GD30BM1018 devices. This action allows the host to quickly (<100 µs) disable and reenable discharging without disturbing register contents. This ability can be useful, for instance, to allow a specific settling time before taking cell measurements. The mute status is reported in the read-only MUTE bit in Configuration Register Group B.

7.12 Serial Interface Overview

There are two types of serial ports on the GD30BM1018: a standard 4-wire SPI and a 2-wire isoSPI. The state of the ISOMD pin determines whether Pin 53, Pin 54, Pin 61, and Pin 62 are a 2-wire or 4-wire serial port.

The GD30BM1018 is used in a daisy-chain configuration.

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A second isoSPI uses Pin 57, Pin 58, Pin 63, and Pin 64.

7.13 4-Wire Serial Peripheral Interface(SPI) Physical Layer

7.13.1 External Connections

Connecting ISOMD to V– configures serial Port A for 4-wire SPI. The SDO pin is an open drain output that requires a pull-up resistor tied to the appropriate supply voltage (see Figure 28).

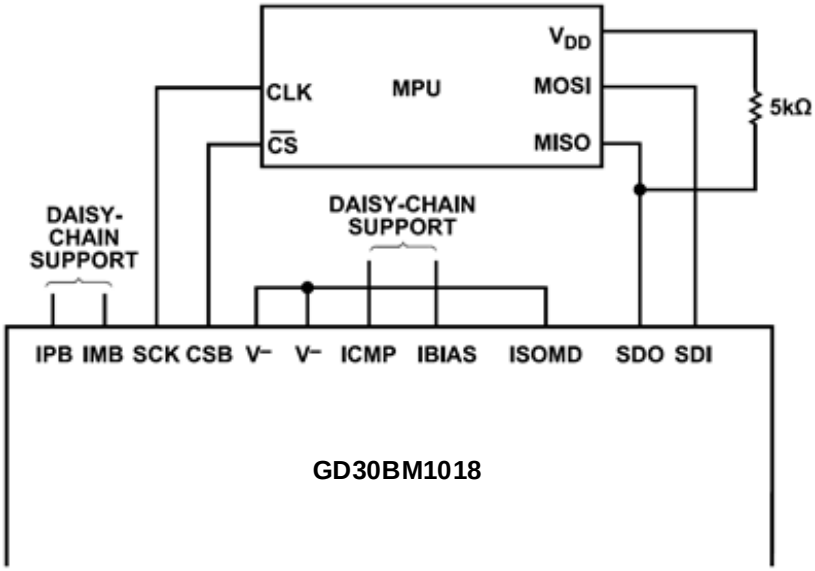

Figure 28. 4-Wire SPI Configuration

7.13.2 Timing

The 4-wire serial port is configured to operate in an SPI system using CPHA = 1 and CPOL =1. Consequently, data on SDI must be stable during the rising edge of SCK. The timing is depicted in Figure 29. The maximum data rate is 1 Mbps. However, the device is tested at a higher data rate in production to guarantee operation at the maximum specified data rate.

7.14 2-Wire Serial Peripheral Interface(SPI) Physical Layer

The 2-wire interface provides a means to interconnect GD30BM1018 devices using simple twisted pair cabling. The interface is designed for low packet error rates when the cabling is subjected to high RF fields. Isolation is achieved through an external transformer.

Standard SPI signals are encoded into differential pulses. The strength of the transmission pulse and the threshold level of the receiver are set by two external resistors. The values of the resistors allow the user to trade-off power dissipation for noise immunity.

Figure 30 shows how the isoSPI circuit operates. A 2 V reference drives the IBIAS pin. External resistors RB1 and RB2 create the reference current, IB. This current sets the drive strength of the transmitter. RB1 and RB2 also form a voltage divider to supply a fraction of the 2 V reference for the ICMP pin. The receiver circuit threshold is half of the voltage at the ICMP pin.

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7.14.1 External Connections

The GD30BM1018 has 2 serial ports, Port B and Port A. Port B is always configured as a 2-wire interface. Port A is either a 2-wire or 4-wire interface, depending on the connection of the ISOMD pin.

When Port A is configured as a 4-wire interface, Port A is always the slave port and Port B is the master port. Communication is always initiated on Port A of the first device in the daisy-chain configuration. The final device in the daisy chain does not use Port B, and it must be terminated into R_M. Figure 31 shows the simplest port connections possible when the microprocessor and the GD30BM1018 are located on the same PCB. In Figure 31, capacitors are used to couple signals between the GD30BM1018.

When Port A is configured as a 2-wire interface, communication can be initiated on either Port A or Port B. If communication is initiated on Port A, GD30BM1018 configures Port A as a slave and Port B as a master. Likewise, if communication is initiated on Port B, GD30BM1018 configures Port B as a slave and Port A as a master.

Figure 30 is an example of a robust interconnection of multiple identical PCBs, each containing one GD30BM1018 configured for operation in a daisy chain. The microprocessor is located on a separate PCB. To achieve 2-wire isolation between the microprocessor PCB and the 1st GD30BM1018 PCB, use the LTC6820 support IC. The LTC6820 is functionally equivalent to the diagram in Figure 30. In this example, communication is initiated on Port A. Therefore, the GD30BM1018 configures Port A as a slave and Port B as a master.

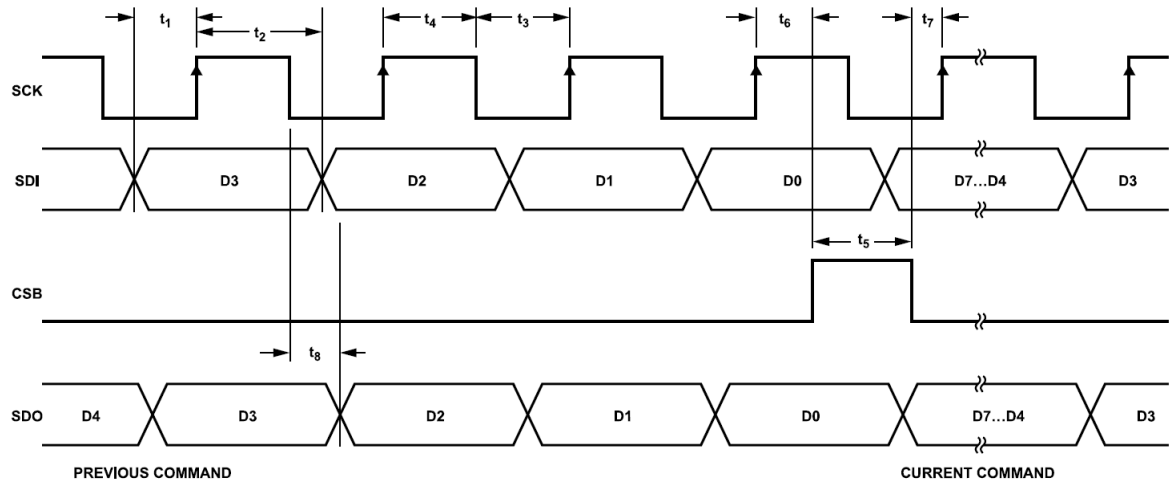

Figure 29. Timing Diagram of 4-Wire Serial Peripheral Interface

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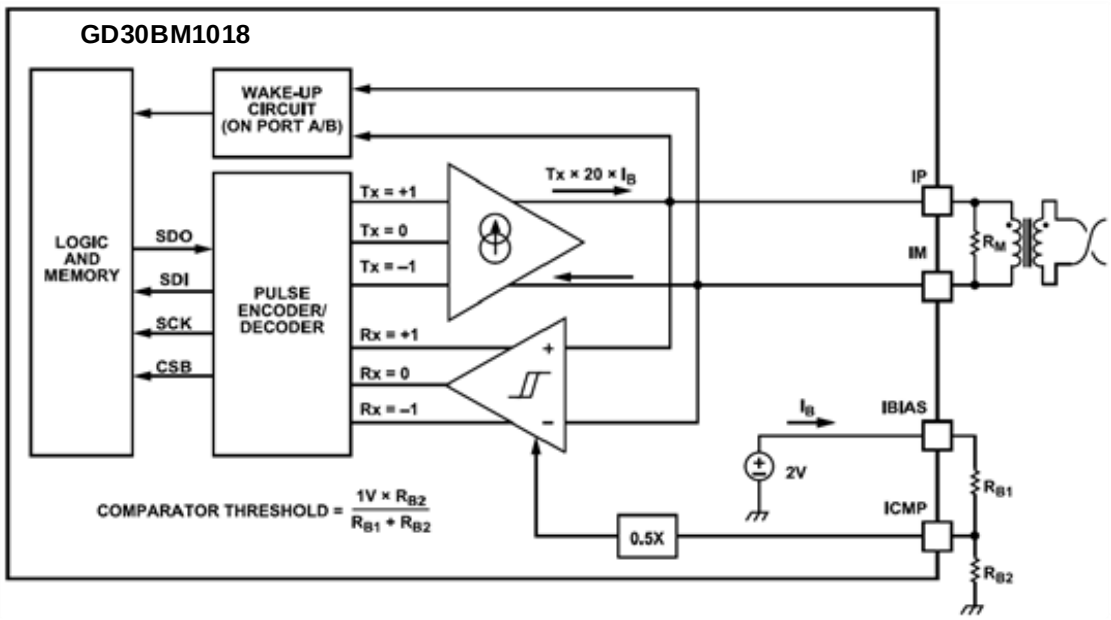

Figure 30. isoSPI Interface

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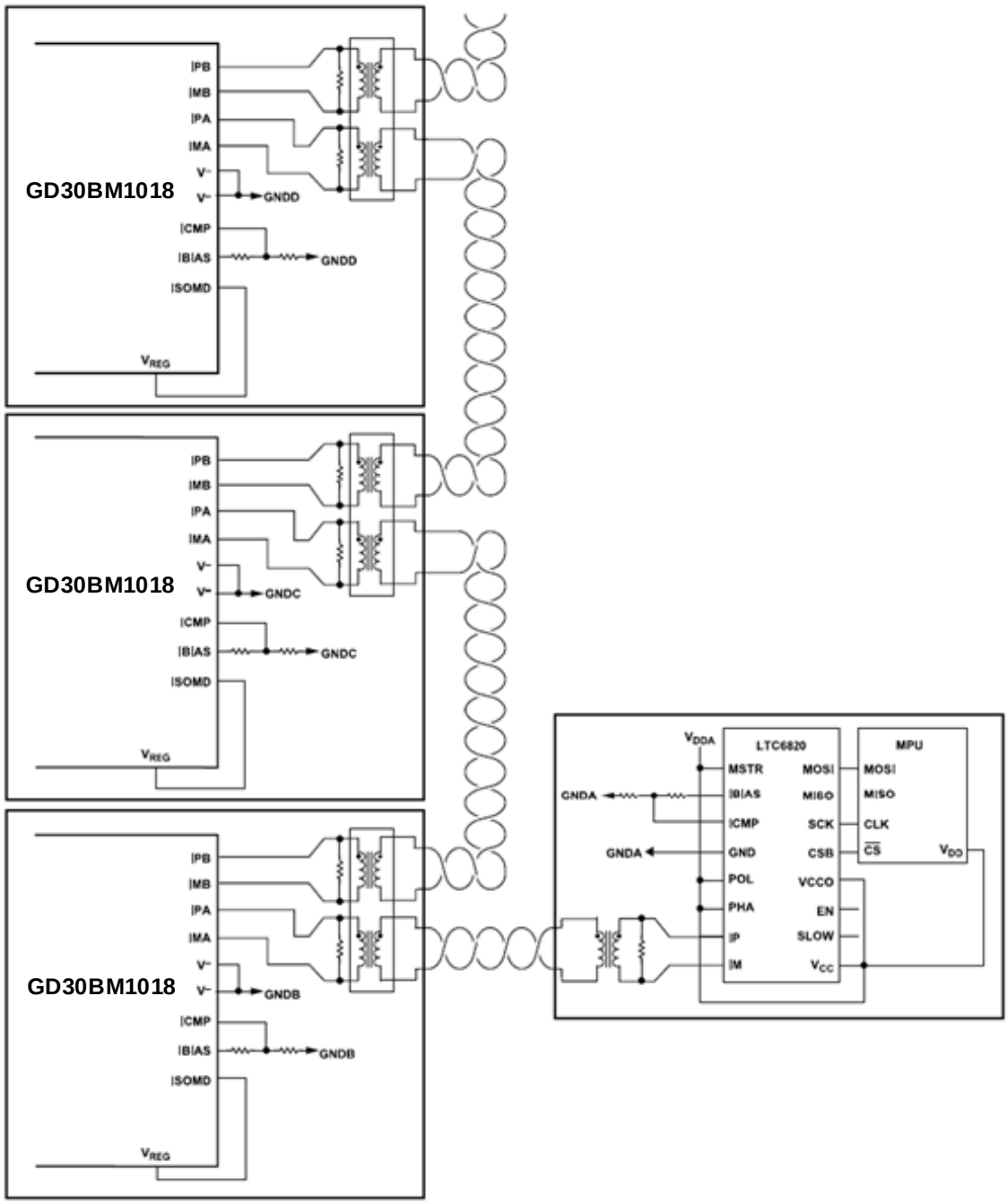

Figure 31. Transformer-Isolated Daisy-Chain Configuration

7.14.2 Waking up the Serial Interface

The serial ports (SPI or isoSPI) enter the low power idle state if there is no activity on Port A or Port B for a time of t_{IDLE}. The wake-up circuit monitors activity on Pin 61 through Pin 64. If ISOMD = V–, Port A is in SPI mode. Activity on the CSB pin or SCK pin wakes up the SPI. If ISOMD = V_{REG}, Port A is in isoSPI mode. Differential activity on IPA to IMA (or IPB to IMB) wakes up the isoSPI. The GD30BM1018 is ready to communicate when the isoSPI state changes to ready within t_{WAKE} or t_{READY}, depending on the core state (see Figure 15 and the *Sleep State*, *Standby State*, *REFUP State*, and *Measure State* sections for details).

Figure 32 shows the timing and the functionally equivalent circuit (only Port A shown). Common-mode signals do

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not wake up the serial interface. The interface is designed to wake up after receiving a large signal single-ended pulse, or a low-amplitude symmetric pulse. The differential signal (SCK(IPA) – CSB(IMA)), must be at least V_{WAKE} = 200 mV for a minimum duration of t_{DWELL} = 240 ns to qualify as a wake-up signal that powers up the serial interface.

7.14.3 Waking a Daisy Chain—Method 1

The GD30BM1018 sends a long +1 pulse on Port B after it is ready to communicate. In a daisy-chained configuration, this pulse wakes up the next device in the stack which, in turn, wakes up the next device. If there are N devices in the stack, all the devices are powered up within the time N × t_{WAKE} or N × t_{READY}, depending on the core state. For large stacks, the time N × t_{WAKE} may be equal to or larger than t_{IDLE}. In this case, after waiting longer than the time of N × t_{WAKE}, the host can send another dummy byte and wait for the time N × t_{READY} to ensure that all devices are in the ready state.

Method 1 can be used when all devices on the daisy chain are in the idle state, which guarantees that the devices propagate the wake-up signal up the daisy chain. However, this method fails to wake up all devices when a device in the middle of the chain is in the ready state instead of the idle state. When this happens, the device in the ready state does not propagate the wake-up pulse, so the devices above it remain in the idle state. This situation can occur when attempting to wake up the daisy chain after only t_{IDLE} of idle time (some devices may be idle, some may not).

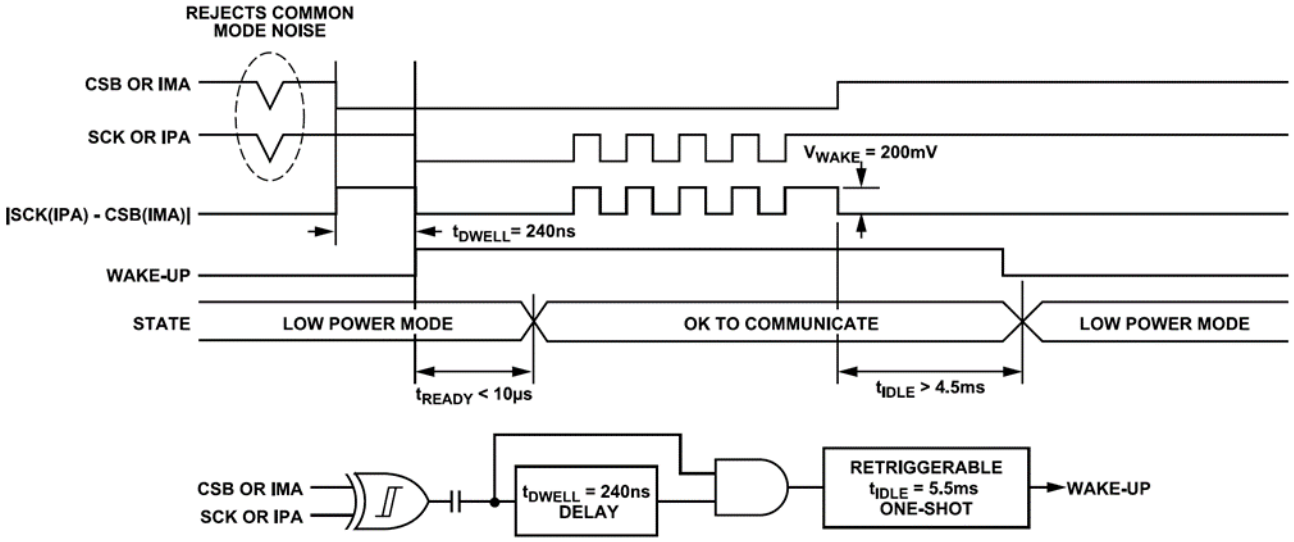

Figure 32. Wake-Up Detection and Idle Timer

7.14.4 Waking a Daisy Chain—Method 2

A more robust wake-up method does not rely on the built-in wakeup pulse, but manually sends isoSPI traffic for enough time to wake the entire daisy chain. At a minimum, a pair of long isoSPI pulses (–1 and +1) is needed for each device, separated by more than t_{READY} or t_{WAKE} (if the core state is standby mode or sleep mode, respectively), but less than t_{IDLE}. This allows each device to wake up and propagate the next pulse to the following device. This method works even if some devices in the chain are not in the idle state. In practice, implementing Method 2 requires toggling the CSB pin (of the LTC6820, or bottom GD30BM1018 with ISOMD = 0) to generate the long isoSPI pulses. Alternatively, dummy commands (such as RDCFGA) can be executed to generate the long isoSPI pulses.

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7.15 Data Link Layer

All data transfers on GD30BM1018 occur in byte groups. Every byte consists of 8 bits. Bytes are transferred with the MSB first. CSB must remain low for the entire duration of a command sequence, including between a command byte and subsequent data. On a write command, data is latched in on the rising edge of CSB.

7.16 Network Layer

7.16.1 Packet Error Code

The PEC is a 15-bit cyclic redundancy check (CRC) value calculated for all of the bits in a register group in the order they are passed, using the initial PEC value of 000000000010000 and the following characteristic polynomial: x15 + x14 + x10 + x8 + x7 + x4 + x3 + 1.

To calculate the 15-bit PEC value, a simple procedure can be established:

1. Initialize the PEC to 000000000010000 (PEC is a 15-bit register group).
2. For each bit DIN coming into the PEC register group, set:
   - IN0 = DIN XOR PEC, Bit 14
   - IN3 = IN0 XOR PEC, Bit 2
   - IN4 = IN0 XOR PEC, Bit 3
   - IN7 = IN0 XOR PEC, Bit 6
   - IN8 = IN0 XOR PEC, Bit 7
   - IN10 = IN0 XOR PEC, Bit 9
   - IN14 = IN0 XOR PEC, Bit 13
3. Update the 15-bit PEC as follows:
   - PEC, Bit 14 = IN14
   - PEC, Bit 13 = PEC, Bit 12
   - PEC, Bit 12 = PEC, Bit 11
   - PEC, Bit 11 = PEC, Bit 10
   - PEC, Bit 10 = IN10
   - PEC, Bit 9 = PEC, Bit 8
   - PEC, Bit 8 = IN8
   - PEC, Bit 7 = IN7
   - PEC, Bit 6 = PEC, Bit 5
   - PEC, Bit 5 = PEC, Bit 4
   - PEC, Bit 4 = IN4
   - PEC, Bit 3 = IN3
   - PEC, Bit 2 = PEC, Bit 1
   - PEC, Bit 1 = PEC, Bit 0
   - PEC, Bit 0 = IN0
4. Go back to Step 2 until all the data is shifted. The final PEC (16 bits) is the 15-bit value in the PEC register with a 0 bit appended to its LSB.

Figure 33 shows the 15-bit PEC algorithm. An example to calculate the PEC for a 16-bit word (0x0001) is listed in Table 26. The PEC for 0x0001 is computed as 0x3D6E after stuffing a 0 bit at the LSB. For longer data streams,

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the PEC is valid at the end of the last bit of data sent to the PEC register.

The GD30BM1018 calculates the PEC for any command or data received and compares it with the PEC following the command or data. The command or data is regarded as valid only if the PEC matches. GD30BM1018 also attaches the calculated PEC at the end of the data it shifts out. Table 27 shows the format of PEC while writing to or reading from GD30BM1018.

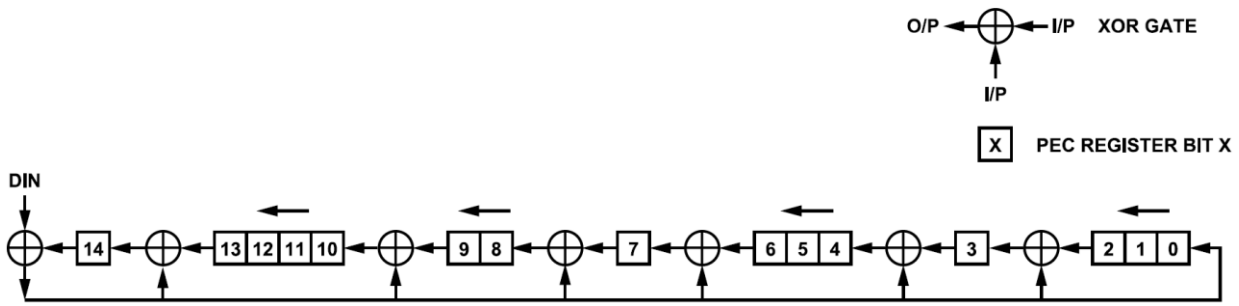

Figure 33. 15-Bit PEC Computation Circuit

Table 26. PEC Calculation for 0x0001

PEC, Bit 14	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	0	0
PEC, Bit 13	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	1	0	0
PEC, Bit 12	0	0	0	0	0	0	0	0	1	0	0	0	0	1	1	0	1	1
PEC, Bit 11	0	0	0	0	0	0	0	1	0	0	0	0	1	1	0	1	1	1
PEC, Bit 10	0	0	0	0	0	0	1	0	0	0	0	1	1	0	1	1	1	1
PEC, Bit 9	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	1	1
PEC, Bit 8	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	1	0	0
PEC, Bit 7	0	0	0	1	0	0	0	0	0	0	0	1	1	1	0	1	1	1
PEC, Bit 6	0	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
PEC, Bit 5	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	1
PEC, Bit 4	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	1	1
PEC, Bit 3	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0
PEC, Bit 2	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1
PEC, Bit 1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
PEC, Bit 0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1
IN14	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	0		0
IN10	0	0	0	0	0	1	0	0	0	0	1	1	0	1	1	1		PEC Word
IN8	0	0	0	1	0	0	0	0	0	0	1	0	0	0	1	0		
IN7	0	0	1	0	0	0	0	0	0	0	1	1	1	0	1	1		
IN4	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	1		
IN3	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0		
IN0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1		
DIN	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1		
Clock Cycle	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

Table 27. Write/Read PEC Format

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Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit0
PEC0	R	PEC, Bit14	PEC, Bit 13	PEC, Bit 12	PEC, Bit 11	PEC, Bit10	PEC, Bit 9	PEC, Bit 8	PEC,Bit17
PEC1	R	PEC, Bit 6	PEC, Bit 5	PEC, Bit 4	PEC, Bit 3	PEC, Bit 2	PEC, Bit 1	PEC, Bit 0	0

While writing any command to GD30BM1018, the command bytes CMD0 and CMD1 (see Table 30 and Table 31) and the PEC bytes PEC0 and PEC1 are sent on Port A in the following order:

CMD0, CMD1, PEC0, PEC1

After a write command to daisy-chained GD30BM1018 devices, data is sent to each device followed by the PEC. For example, when writing Configuration Register Group A to two daisy-chained devices (primary device P, stacked device S), the data is sent to the primary device on Port A in the following order:

CFGAR0(S), ····· , CFGAR5(S), PEC0(S), PEC1(S), CFGAR0(P), ····· , CFGAR5(P), PEC0(P), PEC1(P)

After a read command for daisy-chained devices, each device shifts out its data and the PEC that it computed for its data on Port A followed by the data received on Port B. For example, when reading Status Register Group B from two daisy-chained devices (primary device P, stacked device S), the primary device sends out data on Port A in the following order:

STBR0(P), ····· , STBR5(P), PEC0(P), PEC1(P), STBR0(S), ····· , STBR5(S), PEC0(S), PEC1(S)

See the *Bus Protocols* section for the command format.

All devices in a daisy-chained configuration receive the command bytes simultaneously. For example, to initiate ADC conversions in a stack of devices, a single ADCV command is sent, and all devices start conversions at the same time. For read and write commands, a single command is sent, and the stacked devices effectively turn into a cascaded shift register, in which data is shifted through each device to the next higher (on a write) or the next lower (on a read) device in the stack. See the *Serial Interface Overview* section.

7.16.2 Polling Methods

The simplest method to determine ADC completion is for the controller to start an ADC conversion and wait for the specified conversion time to pass before reading the results.

If using a single GD30BM1018 that communicates in SPI mode (ISOMD pin tied low), there are two methods of polling. The first method is to hold CSB low after an ADC conversion command is sent. After entering a conversion command, the SDO line is driven low when the device is busy performing conversions. SDO is pulled high when the device completes conversions. However, SDO also goes high when CSB goes high even if the device has not completed the conversion (see Figure 34). A problem with this method is that the controller is not free to perform other serial communications while waiting for ADC conversions to complete.

The next method overcomes this limitation. The controller can send an ADC start command, perform other tasks, and then send a poll ADC converter status (PLADC) command to determine the status of the ADC conversions (see Figure 35). After entering the PLADC command, SDO goes low if the device is busy performing conversions. SDO is pulled high at the end of conversions. However, SDO also goes high when CSB goes high even if the device has not completed the conversion.

If using a single GD30BM1018 that communicates in isoSPI mode, the low-side port transmits a data pulse only in response to a master isoSPI pulse received by it. Therefore, after entering the command in either method of polling described previously, isoSPI data pulses are sent to the part to update the conversion status. These pulses

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can be sent using the LTC6820 by simply clocking its SCK pin. In response to this pulse, the GD30BM1018 sends back a low isoSPI pulse if it is still busy performing conversions or a high data pulse if it has completed the conversions. If a CSB high isoSPI pulse is sent to the device, the device exits the polling command.

In a daisy-chained configuration of N stacked devices, the same two polling methods can be used. If the bottom device communicates in SPI mode, the SDO of the bottom device indicates the conversion status of the entire stack. That is, SDO remains low until all the devices in the stack have completed the conversions. In the first method of polling, after an ADC conversion command is sent, clock pulses are sent on SCK while keeping CSB low. The SDO status becomes valid only at the end of N clock pulses on SCK. During the first N clock pulses, the bottom GD30BM1018 in the daisy chain outputs a 0 or a low data pulse. After N clock pulses, the output data from the bottom GD30BM1018 gets updated for every clock pulse that follows (see Figure 36). In the second method, the PLADC command is sent followed by clock pulses on SCK while keeping CSB low. Similar to the first method, the SDO status is valid only after N clock cycles on SCK and gets updated after every clock cycle that follows (see Figure 37).

If the bottom device communicates in isoSPI mode, isoSPI data pulses are sent to the device to update the conversion status. Using the LTC6820, this action can be achieved by just clocking the SCK pin. The conversion status is valid only after the bottom GD30BM1018 device receives N isoSPI data pulses and the status gets updated for every isoSPI data pulse that follows. The device returns a low data pulse if any of the devices in the stack is busy performing conversions and returns a high data pulse if all the devices are free.

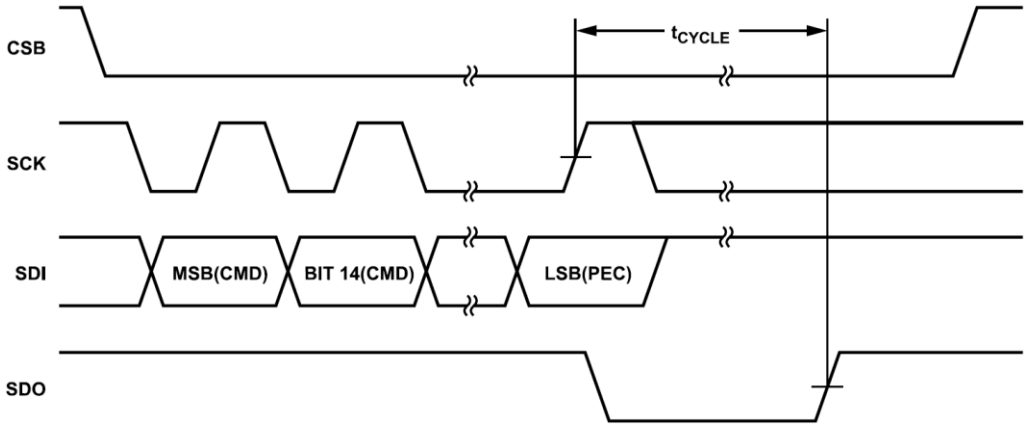

Figure 34. SDO Polling After an ADC Conversion Command (Single GD30BM1018)

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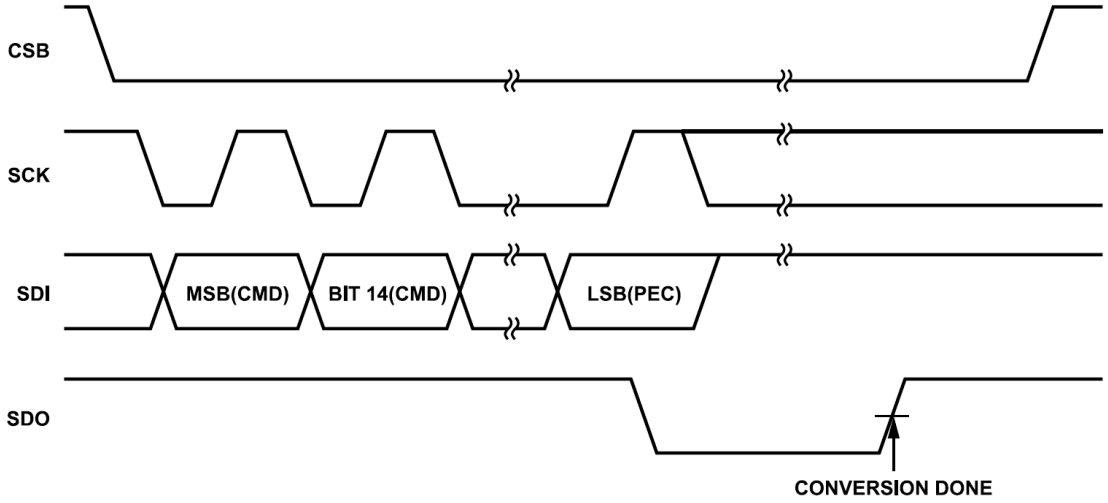

Figure 35. SDO Polling Using PLADC Command (Single GD30BM1018)

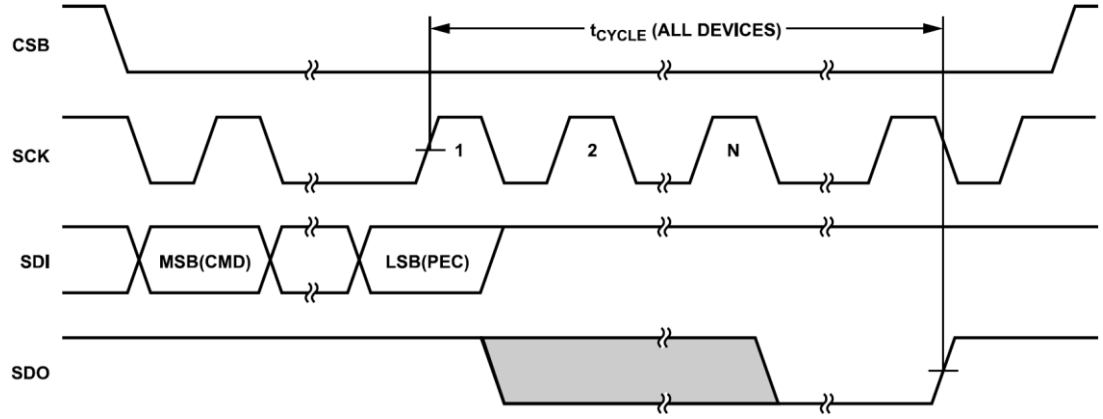

Figure 36. SDO Polling After an ADC Conversion Command (Daisy-Chain Configuration)

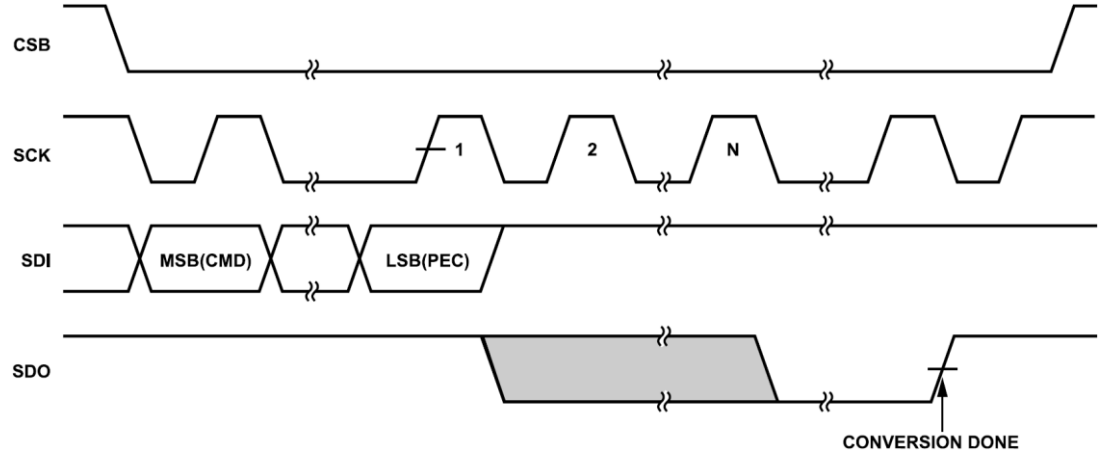

Figure 37. SDO Polling Using PLADC Command (Daisy-Chain Configuration)

7.16.3 Bus Protocols

The protocol formats for commands are depicted in Table 29, Table 30, and Table 31. Table 28 is the key for reading the protocol diagrams.

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Table 28. Protocol Key

Byte	Description
CMD0	Command Byte 0 (see Table 32)
CMD1	Command Byte 1 (see Table 32)
PEC0	PEC Byte 0(see Table 27)
PEC1	PEC Byte 1(see Table 27)
n	Number of bytes
…	Continuation of protocol
	Master to slave
	Slave to master

Table 29. Poll Command

8	8	8	8	
CMD0	CMD1	PEC0	PEC1	Poll Data

Table 30. Write Command

8	8	8	8	8		8	8	8	8		8
CMD0	CMD1	PEC0	PEC1	Data byte low	…	Data byte high	PEC0	PEC1	Shift Byte 1	…	Shift Byte n

Table 31. Read Command

8	8	8	8	8		8	8	8	8		8
CMD0	CMD1	PEC0	PEC1	Data byte low	…	Data byte high	PEC0	PEC1	Shift Byte 1	…	Shift Byte n

Command Format: The format for the commands is shown in Table 32. CC, Bits[10:0] is the 11-bit command code. A list of all the command codes is shown in Table 33. All commands have a value 0 for CMD0, Bit 7 through CMD0, Bit 3. The PEC must be computed on the entire 16-bit command (CMD0 and CMD1).

Table 32. Command Format

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit0
CMD0	W	0	0	0	0	0	CC, Bit 10	CC, Bit 9	CC, Bit 8
CMD1	W	CC, Bit 7	CC, Bit 6	CC, Bit 5	CC, Bit 4	CC, Bit 3	CC, Bit 2	CC, Bit 1	CC, Bit 0

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7.16.4 Commands

Table 33 lists all the commands and their options.

Table 33. Command Codes

		CC, Bits[10:0] – Command Code										
Command Description	**Name**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write Configuration Register Group A	WRCFGA	0	0	0	0	0	0	0	0	0	0	1
Write Configuration Register Group B	WRCFGB	0	0	0	0	0	1	0	0	1	0	0
Read Configuration Register Group A	RDCFGA	0	0	0	0	0	0	0	0	0	1	0
Read Configuration Register Group B	RDCFGB	0	0	0	0	0	1	0	0	1	1	0
Read Cell Voltage Register Group A	RDCVA	0	0	0	0	0	0	0	0	1	0	0
Read Cell Voltage Register Group B	RDCVB	0	0	0	0	0	0	0	0	1	1	0
Read Cell Voltage Register Group C	RDCVC	0	0	0	0	0	0	0	1	0	0	0
Read Cell Voltage Register Group D	RDCVD	0	0	0	0	0	0	0	1	0	1	0
Read Cell Voltage Register Group E	RDCVE	0	0	0	0	0	0	0	1	0	0	1
Read Cell Voltage Register Group F	RDCVF	0	0	0	0	0	0	0	1	0	1	1
Read Auxiliary Register Group A	RDAUXA	0	0	0	0	0	0	0	1	1	0	0
Read Auxiliary Register Group B	RDAUXB	0	0	0	0	0	0	0	1	1	1	0
Read Auxiliary Register Group C	RDAUXC	0	0	0	0	0	0	0	1	1	0	1
Read Auxiliary Register Group D	RDAUXD	0	0	0	0	0	0	0	1	1	1	1
Read Status Register Group A	RDSTATA	0	0	0	0	0	0	1	0	0	0	0
Read Status Register Group B	RDSTATB	0	0	0	0	0	0	1	0	0	1	0
Write S Control Register Group	WRSCTRL	0	0	0	0	0	0	1	0	1	0	0
Write PWM Register Group	WRPWM	0	0	0	0	0	1	0	0	0	0	0
Write PWM/S Control Register Group B	WRPSB	0	0	0	0	0	0	1	1	1	0	0
Read S Control Register Group	RDSCTRL	0	0	0	0	0	0	1	0	1	1	0
Read PWM Register Group	RDPWM	0	0	0	0	0	1	0	0	0	1	0
Read PWM/S Control Register Group B	RDPSB	0	0	0	0	0	0	1	1	1	1	0
Start S Control Pulsing and Poll Status	STSCTRL	0	0	0	0	0	0	1	1	0	0	1
Clear S Control Register Group	CLRSCTRL	0	0	0	0	0	0	1	1	0	0	0
Start Cell Voltage ADC Conversion and Poll Status	ADCV	0	1	MD, Bit 1	MD, Bit 0	1	1	DCP	0	CH, Bit2	CH, Bit 1	CH, Bit 0
Start Open Wire ADC Conversion and Poll Status	ADOW	0	1	MD, Bit 1	MD, Bit 0	PUP	1	DCP	1	CH, Bit 2	CH, Bit 1	CH, Bit 0
Start Self Test Cell Voltage Conversion and Poll Status	CVST	0	1	MD, Bit 1	MD, Bit 0	ST, Bit 1	ST, Bit 0	0	0	1	1	1
Start Overlap Measurements of Cell 7 and Cell 13 Voltages	ADOL	0	1	MD, Bit 1	MD, Bit 0	0	0	DCP	0	0	0	1
Start GPIOs ADC Conversion and Poll Status	ADAX	1	0	MD, Bit 1	MD, Bit 0	1	1	0	0	CHG, Bit 2	CHG, Bit 1	CHG, Bit 0
Start GPIOs ADC Conversion with Digital Redundancy and Poll Status	ADAXD	1	0	MD, Bit 1	MD, Bit 0	0	0	0	0	CHG, Bit 2	CHG, Bit 1	CHG, Bit 0
Start GPIOs Open Wire ADC Conversion and Poll Status	AXOW	1	0	MD, Bit 1	MD, Bit 0	PUP	0	1	0	CHG, Bit 2	CHG, Bit 1	CHG, Bit 0
Start Self Test GPIOs Conversion and Poll Status	AXST	1	0	MD, Bit 1	MD, Bit 0	ST, Bit 1	ST, Bit 0	0	0	1	1	1
Start Status Group ADC Conversion and Poll Status	ADSTAT	1	0	MD, Bit 1	MD, Bit 0	1	1	0	1	CHST, Bit 2	CHST, Bit 1	CHST, Bit 0
Start Status Group ADC Conversion with Digital Redundancy and Poll Status	ADSTATD	1	0	MD, Bit 1	MD, Bit 0	0	0	0	1	CHST, Bit 2	CHST, Bit 1	CHST, Bit 0
Start Self Test Status Group Conversion and Poll Status	STATST	1	0	MD, Bit 1	MD, Bit 0	ST, Bit 1	ST, Bit 0	0	1	1	1	1
Start Combined Cell Voltage and GPIO1, GPIO2 Conversion and Poll Status	ADCVAX	1	0	MD, Bit 1	MD, Bit 0	1	1	DCP	1	1	1	1
Start Combined Cell Voltage and SC Conversion and Poll Status	ADCVSC	1	0	MD, Bit 1	MD, Bit 0	1	1	DCP	0	1	1	1
Clear Cell Voltage Register Groups	CLRCELL	1	1	1	0	0	0	1	0	0	0	1
Clear Auxiliary Register Groups	CLRAUX	1	1	1	0	0	0	1	0	0	1	0
Clear Status Register Groups	CLRSTAT	1	1	1	0	0	0	1	0	0	1	1
Poll ADC Conversion Status	PLADC	1	1	1	0	0	0	1	0	1	0	0
Diagnose MUX and Poll Status	DIAGN	1	1	1	0	0	0	1	0	1	0	1
Write COMM Register Group	WRCOMM	1	1	1	0	0	1	0	0	0	0	1
Read COMM Register Group	RDCOMM	1	1	1	0	0	1	0	0	0	1	0
Start I2C/SPI Communication	STCOMM	1	1	1	0	0	1	0	0	0	1	1

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		CC, Bits[10:0] – Command Code										
Command Description	**Name**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Mute Discharge	Mute	0	0	0	0	0	1	0	1	0	0	0
Unmute Discharge	Unmute	0	0	0	0	0	1	0	1	0	0	1

Table 34. Command Bit Descriptions

Name	Description	Values									
MD, Bits[1:0]	ADC Mode	MD 00 01 10 11	ADCOPT(CFGAR0, Bit 0) = 0 422 Hz mode 27 kHz mode (fast) 7 kHz mode (normal) 26 Hz mode (filtered)	ADCOPT(CFGAR0, Bit 0) = 1 1 kHz mode 14 kHz mode 3 kHz mode 2 kHz mode							
DCP	Discharge Permitted	DCP 0 1	Discharge Not Permitted Discharge Permitted								
CH, Bits[2:0]	Cell Selection for ADC Conversion	CH	Total Conversion Time in the 8 ADC Modes								
				27 kHz	14 kHz	7 kHz	3 kHz	2 kHz	1 kHz	422 Hz	26 Hz
		000	All cells	1.1 ms	1.3 ms	2.3 ms	3.0 ms	4.4 ms	7.2 ms	12.8 ms	201 ms
		001	Cells 1, 7, 13	203 µs	232 µs	407 µs	523 µs	756 µs	1.2 ms	2.2 ms	34 ms
		010	Cells 2, 8, 14	203 µs	232 µs	407 µs	523 µs	756 µs	1.2 ms	2.2 ms	34 ms
		011	Cells 3, 9, 15	203 µs	232 µs	407 µs	523 µs	756 µs	1.2 ms	2.2 ms	34 ms
		100	Cells 4, 10, 16	203 µs	232 µs	407 µs	523 µs	756 µs	1.2 ms	2.2 ms	34 ms
		101	Cells 5, 11, 17	203 µs	232 µs	407 µs	523 µs	756 µs	1.2 ms	2.2 ms	34 ms
		110	Cells 6, 12, 18	203 µs	232 µs	407 µs	523 µs	756 µs	1.2 ms	2.2 ms	34 ms
PUP	Pull-Up/Pull- Down Current for Open Wire Conversions	PUP									
		0 1	Pull-down current Pull-up current Self Test Conversion Result								
ST, Bits[1:0]	Self Test Mode Selection	ST 01 10	Self Test 1 Self test 2	27 kHz 0x9565 0x6A9A	14 kHz 0x9553 0x6AAC	7 kHz 0x9555 0x6AAA	3 kHz 0x9555 0x6AAA	2 kHz 0x9555 0x6AAA	1 kHz 0x9555 0x6AAA	422 Hz 0x9555 0x6AAA	26 Hz 0x9555 0x6AAA
CHG, Bits[2:0]	GPIO Selection for ADC Conversion	CHG	Total Conversion Time in the 8 ADC Modes								
				27 kHz	14 kHz	7 kHz	3 kHz	2 kHz	1 kHz	422 Hz	26 Hz
		000	GPIO1 to GPIO5, 2nd Reference, GPIO6 to GPIO9	1.8 ms 380 µs	2.1 ms 439 µs	3.9 ms 788 µs	5.0ms 1.0 ms	7.4 ms 1.5 ms	12.0 ms 2.4 ms	21.3 ms 4.3 ms	335 ms 67.1 ms
		001	GPIO1 and GPIO6	380 µs	439 µs	788 µs	1.0 ms	1.5 ms	2.4 ms	4.3 ms	67.1 ms
		010	GPIO2 and GPIO7	380 µs	439 µs	788 µs	1.0 ms	1.5 ms	2.4 ms	4.3 ms	67.1 ms
		011	GPIO3 and GPIO8								
		100	GPIO4 and GPIO9 GPIO5	380 µs	439 µs	788 µs	1.0 ms	1.5 ms	2.4 ms	4.3 ms	67.1 ms
		101	2nd Reference	200 µs	229 µs	403 µs	520 µs	753 µs	1.2 ms	2.1 ms	34 ms
		110		200 µs	229 µs	403 µs	520 µs	753 µs	1.2 ms	2.1 ms	34 ms
CHST, Bits[2:0][1]	Status Group Selection	CHST 000	Total Conversion Time in the 8 ADC Modes								
				27 kHz	14 kHz	7 kHz	3 kHz	2 kHz	1 kHz	422 Hz	26 Hz
			SC, ITMP, VA, VD	742 µs	858 µs	1.6 ms	2.0 ms	3.0 ms	4.8 ms	8.5 ms	134 ms
		001		200 µs	229 µs	403 µs	520 µs	753 µs	1.2 ms	2.1 ms	34 ms
		010	SC ITMP VA	200 µs	229 µs	403 µs	520 µs	753 µs	1.2 ms	2.1 ms	34 ms
		011	VD	200 µs	229 µs	403 µs	520 µs	753 µs	1.2 ms	2.1 ms	34 ms
		100		200 µs	229 µs	403 µs	520 µs	753 µs	1.2 ms	2.1 ms	34 ms

1. Note: Valid options for CHST in ADSTAT command are 0 to 4. If CHST is set to 5/6 in ADSTAT command, the GD30BM1018 ignores the command.

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8 Memory Map

Table 35. Configuration Register Group A

Register	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit0
CFGAR0	R/W	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	REFON	DTEN	ADCOPT
CFGAR1	R/W	VUV[7]	VUV[6]	VUV[5]	VUV[4]	VUV[3]	VUV[2]	VUV[1]	VUV[0]
CFGAR2	R/W	VOV[3]	VOV[2]	VOV[1]	VOV[0]	VUV[11]	VUV[10]	VUV[9]	VUV[8]
CFGAR3	R/W	VOV[11]	VOV[10]	VOV[9]	VOV[8]	VOV[7]	VOV[6]	VOV[5]	VOV[4]
CFGAR4	R/W	DCC8	DCC7	DCC6	DCC5	DCC4	DCC3	DCC2	DCC1
CFGAR5	R/W	DCTO[3]	DCTO[2]	DCTO[1]	DCTO[0]	DCC12	DCC11	DCC10	DCC9

Table 36. Configuration Register Group B

Register	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit0
CFGBR0	R/W	DCC16	DCC15	DCC14	DCC13	GPIO9	GPIO8	GPIO7	GPIO6
CFGBR1	R/W	MUTE	FDRF	PS[1]	PS[0]	DTMEN	DCC0	DCC18	DCC17
CFGBR2	R/W	RSVD0	RSVD0	RSVD0	RSVD0	RSVD0	RSVD0	RSVD0	RSVD0
CFGBR3	R/W	RSVD0	RSVD0	RSVD0	RSVD0	RSVD0	RSVD0	RSVD0	RSVD0
CFGBR4	R/W	RSVD0	RSVD0	RSVD0	RSVD0	RSVD0	RSVD0	RSVD0	RSVD0
CFGBR5	R/W	RSVD0	RSVD0	RSVD0	RSVD0	RSVD0	RSVD0	RSVD0	RSVD0

Table 37. Cell Voltage Register Group A

Register	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit0
CVAR0	R	C1V[7]	C1V[6]	C1V[5]	C1V[4]	C1V[3]	C1V[2]	C1V[1]	C1V[0]
CVAR1	R	C1V[15]	C1V[14]	C1V[13]	C1V[12]	C1V[11]	C1V[10]	C1V[9]	C1V[8]
CVAR2	R	C2V[7]	C2V[6]	C2V[5]	C2V[4]	C2V[3]	C2V[2]	C2V[1]	C2V[0]
CVAR3	R	C2V[15]	C2V[14]	C2V[13]	C2V[12]	C2V[11]	C2V[10]	C2V[9]	C2V[8]
CVAR4	R	C3V[7]	C3V[6]	C3V[5]	C3V[4]	C3V[3]	C3V[2]	C3V[1]	C3V[0]
CVAR5	R	C3V[15]	C3V[14]	C3V[13]	C3V[12]	C3V[11]	C3V[10]	C3V[9]	C3V[8]

Table 38. Cell Voltage Register Group B

Register	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit0
CVBR0	R	C4V[7]	C4V[6]	C4V[5]	C4V[4]	C4V[3]	C4V[2]	C4V[1]	C4V[0]
CVBR1	R	C4V[15]	C4V[14]	C4V[13]	C4V[12]	C4V[11]	C4V[10]	C4V[9]	C4V[8]
CVBR2	R	C5V[7]	C5V[6]	C5V[5]	C5V[4]	C5V[3]	C5V[2]	C5V[1]	C5V[0]
CVBR3	R	C5V[15]	C5V[14]	C5V[13]	C5V[12]	C5V[11]	C5V[10]	C5V[9]	C5V[8]
CVBR4	R	C6V[7]	C6V[6]	C6V[5]	C6V[4]	C6V[3]	C6V[2]	C6V[1]	C6V[0]
CVBR5	R	C6V[15]	C6V[14]	C6V[13]	C6V[12]	C6V[11]	C6V[10]	C6V[9]	C6V[8]

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Table 39. Cell Voltage Register Group C

Register	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit0
CVCR0	R	C7V[7]	C7V[6]	C7V[5]	C7V[4]	C7V[3]	C7V[2]	C7V[1]	C7V[0]
CVCR1	R	C7V[15]	C7V[14]	C7V[13]	C7V[12]	C7V[11]	C7V[10]	C7V[9]	C7V[8]
CVCR21	R	C8V[7] 1	C8V[6] 1	C8V[5] 1	C8V[4] 1	C8V[3] 1	C8V[2] 1	C8V[1] 1	C8V[0] 1
CVCR3 1	R	C8V[15] 1	C8V[14] 1	C8V[13] 1	C8V[12] 1	C8V[11] 1	C8V[10] 1	C8V[9] 1	C8V[8] 1
CVCR4	R	C9V[7]	C9V[6]	C9V[5]	C9V[4]	C9V[3]	C9V[2]	C9V[1]	C9V[0]
CVCR5	R	C9V[15]	C9V[14]	C9V[13]	C9V[12]	C9V[11]	C9V[10]	C9V[9]	C9V[8]

Table 40. Cell Voltage Register Group D

Register	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit0
CVDR0	R	C10V[7]	C10V[6]	C10V[5]	C10V[4]	C10V[3]	C10V[2]	C10V[1]	C10V[0]
CVDR1	R	C10V[15]	C10V[14]	C10V[13]	C10V[12]	C10V[11]	C10V[10]	C10V[9]	C10V[8]
CVDR2	R	C11V[7]	C11V[6]	C11V[5]	C11V[4]	C11V[3]	C11V[2]	C11V[1]	C11V[0]
CVDR3	R	C11V[15]	C11V[14]	C11V[13]	C11V[12]	C11V[11]	C11V[10]	C11V[9]	C11V[8]
CVDR4	R	C12V[7]	C12V[6]	C12V[5]	C12V[4]	C12V[3]	C12V[2]	C12V[1]	C12V[0]
CVDR5	R	C12V[15]	C12V[14]	C12V[13]	C12V[12]	C12V[11]	C12V[10]	C12V[9]	C12V[8]

Table 41. Cell Voltage Register Group E

Register	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit0
CVER0	R	C13V[7]	C13V[6]	C13V[5]	C13V[4]	C13V[3]	C13V[2]	C13V[1]	C13V[0]
CVER1	R	C13V[15]	C13V[14]	C13V[13]	C13V[12]	C13V[11]	C13V[10]	C13V[9]	C13V[8]
CVER21	R	C14V[7] 1	C14V[6] 1	C14V[5] 1	C14V[4] 1	C14V[3] 1	C14V[2] 1	C14V[1] 1	C14V[0] 1
CVER3 1	R	C14V[15] 1	C14V[14] 1	C14V[13] 1	C14V[12] 1	C14V[11] 1	C14V[10] 1	C14V[9] 1	C14V[8] 1
CVER4	R	C15V[7]	C15V[6]	C15V[5]	C15V[4]	C15V[3]	C15V[2]	C15V[1]	C15V[0]
CVER5	R	C15V[15]	C15V[14]	C15V[13]	C15V[12]	C15V[11]	C15V[10]	C15V[9]	C15V[8]

Table 42. Cell Voltage Register Group F

Register	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit0
CVFR0	R	C16V[7]	C16V[6]	C16V[5]	C16V[4]	C16V[3]	C16V[2]	C16V[1]	C16V[0]
CVFR1	R	C16V[15]	C16V[14]	C16V[13]	C16V[12]	C16V[11]	C16V[10]	C16V[9]	C16V[8]
CVFR2	R	C17V[7]	C17V[6]	C17V[5]	C17V[4]	C17V[3]	C17V[2]	C17V[1]	C17V[0]
CVFR3	R	C17V[15]	C17V[14]	C17V[13]	C17V[12]	C17V[11]	C17V[10]	C17V[9]	C17V[8]
CVFR4	R	C18V[7]	C18V[6]	C18V[5]	C18V[4]	C18V[3]	C18V[2]	C18V[1]	C18V[0]
CVFR5	R	C18V[15]	C18V[14]	C18V[13]	C18V[12]	C18V[11]	C18V[10]	C18V[9]	C18V[8]

Table 43. Auxiliary Register Group A

Register	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit0
AVAR0	R	G1V[7]	G1V[6]	G1V[5]	G1V[4]	G1V[3]	G1V[2]	G1V[1]	G1V[0]
AVAR1	R	G1V[15]	G1V[14]	G1V[13]	G1V[12]	G1V[11]	G1V[10]	G1V[9]	G1V[8]

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Register	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit0
AVAR2	R	G2V[7]	G2V[6]	G2V[5]	G2V[4]	G2V[3]	G2V[2]	G2V[1]	G2V[0]
AVAR3	R	G2V[15]	G2V[14]	G2V[13]	G2V[12]	G2V[11]	G2V[10]	G2V[9]	G2V[8]
AVAR4	R	G3V[7]	G3V[6]	G3V[5]	G3V[4]	G3V[3]	G3V[2]	G3V[1]	G3V[0]
AVAR5	R	G3V[15]	G3V[14]	G3V[13]	G3V[12]	G3V[11]	G3V[10]	G3V[9]	G3V[8]

Table 44. Auxiliary Register Group B

Register	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit0
AVBR0	R	G4V[7]	G4V[6]	G4V[5]	G4V[4]	G4V[3]	G4V[2]	G4V[1]	G4V[0]
AVBR1	R	G4V[15]	G4V[14]	G4V[13]	G4V[12]	G4V[11]	G4V[10]	G4V[9]	G4V[8]
AVBR2	R	G5V[7]	G5V[6]	G5V[5]	G5V[4]	G5V[3]	G5V[2]	G5V[1]	G5V[0]
AVBR3	R	G5V[15]	G5V[14]	G5V[13]	G5V[12]	G5V[11]	G5V[10]	G5V[9]	G5V[8]
AVBR4	R	REF[7]	REF[6]	REF[5]	REF[4]	REF[3]	REF[2]	REF[1]	REF[0]
AVBR5	R	REF[15]	REF[14]	REF[13]	REF[12]	REF[11]	REF[10]	REF[9]	REF[8]

Table 45. Auxiliary Register Group C

Register	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit0
AVCR0	R	G6V[7]	G6V[6]	G6V[5]	G6V[4]	G6V[3]	G6V[2]	G6V[1]	G6V[0]
AVCR1	R	G6V[15]	G6V[14]	G6V[13]	G6V[12]	G6V[11]	G6V[10]	G6V[9]	G6V[8]
AVCR2	R	G7V[7]	G7V[6]	G7V[5]	G7V[4]	G7V[3]	G7V[2]	G7V[1]	G7V[0]
AVCR3	R	G7V[15]	G7V[14]	G7V[13]	G7V[12]	G7V[11]	G7V[10]	G7V[9]	G7V[8]
AVCR4	R	G8V[7]	G8V[6]	G8V[5]	G8V[4]	G8V[3]	G8V[2]	G8V[1]	G8V[0]
AVCR5	R	G8V[15]	G8V[14]	G8V[13]	G8V[12]	G8V[11]	G8V[10]	G8V[9]	G8V[8]

Table 46. Auxiliary Register Group D

Register	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit0
AVDR0	R	G9V[7]	G9V[6]	G9V[5]	G9V[4]	G9V[3]	G9V[2]	G9V[1]	G9V[0]
AVDR1	R	G9V[15]	G9V[14]	G9V[13]	G9V[12]	G9V[11]	G9V[10]	G9V[9]	G9V[8]
AVDR2	R	RSVD1	RSVD1	RSVD1	RSVD1	RSVD1	RSVD1	RSVD1	RSVD1
AVDR3	R	RSVD1	RSVD1	RSVD1	RSVD1	RSVD1	RSVD1	RSVD1	RSVD1
AVDR4	R	C16OV	C16UV	C15OV	C15UV	C14OV	C14UV	C13OV	C13UV
AVDR5	R	RSVD1	RSVD1	RSVD1	RSVD1	C18OV	C18UV	C17OV	C17UV

Table 47. Status Register Group A

Register	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit0
STAR0	R	SC[7]	SC[6]	SC[5]	SC[4]	SC[3]	SC[2]	SC[1]	SC[0]
STAR1	R	SC[15]	SC[14]	SC[13]	SC[12]	SC[11]	SC[10]	SC[9]	SC[8]
STAR2	R	ITMP[7]	ITMP[6]	ITMP[5]	ITMP[4]	ITMP[3]	ITMP[2]	ITMP[1]	ITMP[0]
STAR3	R	ITMP[15]	ITMP[14]	ITMP[13]	ITMP[12]	ITMP[11]	ITMP[10]	ITMP[9]	ITMP[8]
STAR4	R	VA[7]	VA[6]	VA[5]	VA[4]	VA[3]	VA[2]	VA[1]	VA[0]
STAR5	R	VA[15]	VA[14]	VA[13]	VA[12]	VA[11]	VA[10]	VA[9]	VA[8]

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Table 48. Status Register Group B

Register	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit0
STBR0	R	VD[7]	VD[6]	VD[5]	VD[4]	VD[3]	VD[2]	VD[1]	VD[0]
STBR1	R	VD[15]	VD[14]	VD[13]	VD[12]	VD[11]	VD[10]	VD[9]	VD[8]
STBR2	R	C4OV	C4UV	C3OV	C3UV	C2OV	C2UV	C1OV	C1UV
STBR3	R	C8OV	C8UV	C7OV	C7UV	C6OV	C6UV	C5OV	C5UV
STBR4	R	C12OV	C12UV	C11OV	C11UV	C10OV	C10UV	C9OV	C9UV
STBR5	R	REV[3]	REV[2]	REV[1]	REV[0]	RSVD	RSVD	MUXFAIL	THSD

Table 49. COMM Register Group

Register	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit0
COMM0	R/W	ICOM0[3]	ICOM0[2]	ICOM0[1]	ICOM0[0]	D0[7]	D0[6]	D0[5]	D0[4]
COMM1	R/W	D0[3]	D0[2]	D0[1]	D0[0]	FCOM0[3]	FCOM0[2]	FCOM0[1]	FCOM0[0]
COMM2	R/W	ICOM1[3]	ICOM1[2]	ICOM1[1]	ICOM1[0]	D1[7]	D1[6]	D1[5]	D1[4]
COMM3	R/W	D1[3]	D1[2]	D1[1]	D1[0]	FCOM1[3]	FCOM1[2]	FCOM1[1]	FCOM1[0]
COMM4	R/W	ICOM2[3]	ICOM2[2]	ICOM2[1]	ICOM2[0]	D2[7]	D2[6]	D2[5]	D2[4]
COMM5	R/W	D2[3]	D2[2]	D2[1]	D2[0]	FCOM2[3]	FCOM2[2]	FCOM2[1]	FCOM2[0]

Table 50. S Control Register Group

Register	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit0
SCTRL0	R/W	SCTL2[3]	SCTL2[2]	SCTL2[1]	SCTL2[0]	SCTL1[3]	SCTL1[2]	SCTL1[1]	SCTL1[0]
SCTRL1	R/W	SCTL4[3]	SCTL4[2]	SCTL4[1]	SCTL4[0]	SCTL3[3]	SCTL3[2]	SCTL3[1]	SCTL3[0]
SCTRL2	R/W	SCTL6[3]	SCTL6[2]	SCTL6[1]	SCTL6[0]	SCTL5[3]	SCTL5[2]	SCTL5[1]	SCTL5[0]
SCTRL3	R/W	SCTL8[3]	SCTL8[2]	SCTL8[1]	SCTL8[0]	SCTL7[3]	SCTL7[2]	SCTL7[1]	SCTL7[0]
SCTRL4	R/W	SCTL10[3]	SCTL10[2]	SCTL10[1]	SCTL10[0]	SCTL9[3]	SCTL9[2]	SCTL9[1]	SCTL9[0]
SCTRL5	R/W	SCTL12[3]	SCTL12[2]	SCTL12[1]	SCTL12[0]	SCTL11[3]	SCTL11[2]	SCTL11[1]	SCTL11[0]

Table 51. PWM Register Group

Register	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit0
PWMR0	R/W	PWM2[3]	PWM2[2]	PWM2[1]	PWM2[0]	PWM1[3]	PWM1[2]	PWM1[1]	PWM1[0]
PWMR1	R/W	PWM4[3]	PWM4[2]	PWM4[1]	PWM4[0]	PWM3[3]	PWM3[2]	PWM3[1]	PWM3[0]
PWMR2	R/W	PWM6[3]	PWM6[2]	PWM6[1]	PWM6[0]	PWM5[3]	PWM5[2]	PWM5[1]	PWM5[0]
PWMR3	R/W	PWM8[3]	PWM8[2]	PWM8[1]	PWM8[0]	PWM7[3]	PWM7[2]	PWM7[1]	PWM7[0]
PWMR4	R/W	PWM10[3]	PWM10[2]	PWM10[1]	PWM10[0]	PWM9[3]	PWM9[2]	PWM9[1]	PWM9[0]
PWMR5	R/W	PWM12[3]	PWM12[2]	PWM12[1]	PWM12[0]	PWM11[3]	PWM11[2]	PWM11[1]	PWM11[0]

Table 52. PWM/S Control Register Group B

Register	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit0
PSR0	R/W	PWM14[3]	PWM14[2]	PWM14[1]	PWM14[0]	PWM13[3]	PWM13[2]	PWM13[1]	PWM13[0]
PSR1	R/W	PWM16[3]	PWM16[2]	PWM16[1]	PWM16[0]	PWM15[3]	PWM15[2]	PWM15[1]	PWM15[0]

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Register	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit0
PSR2	R/W	PWM18[3]	PWM18[2]	PWM18[1]	PWM18[0]	PWM17[3]	PWM17[2]	PWM7[1]	PWM17[0]
PSR3	R/W	SCTL14[3]	SCTL14[2]	SCTL14[1]	SCTL14[0]	SCTL13[3]	SCTL13[2]	SCTL13[1]	SCTL13[0]
PSR4	R/W	SCTL16[3]	SCTL16[2]	SCTL16[1]	SCTL16[0]	SCTL15[3]	SCTL15[2]	SCTL15[1]	SCTL15[0]
PSR5	R/W	SCTL18[3]	SCTL18[2]	SCTL18[1]	SCTL18[0]	SCTL17[3]	SCTL17[2]	SCTL17[1]	SCTL17[0]

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Table 53. Memory Map Bit Descriptions

Bit	Description	Values
GPIOx	GPIOx pin control	Write: 0: GPIOx pin pull-down on 1: GPIOx pin pull-down off (default) Read: 0: GPIOx pin at Logic 0 1: GPIOx pin at Logic 1
REFON	Reference powered up	1: reference remains powered up until watchdog timeout 0: reference shuts down after conversions (default)
DTEN	Discharge timer enable (read only)	0: disables discharge timer 1: enables the discharge timer for discharge switches
ADCOPT	ADC mode option bit	0: selects modes 27 kHz, 7 kHz, 422 Hz or 26 Hz with MD, Bits[1:0] in ADC conversion commands (default) 1: selects modes 14 kHz, 3 kHz, 1 kHz, or 2 kHz with MD, Bits[1:0] in ADC conversion commands
VUV	Undervoltage comparison voltage1	Comparison voltage = (VUV + 1) × 16 × 100 µV, default: VUV = 0x000
VOV	Overvoltage comparison voltage1	Comparison voltage = VOV × 16 × 100 µV, default: VOV = 0x000
DCC[x]	Discharge Cell x	x = 1 to 18: 1: turn on shorting switch for Cell x 0: turn off shorting switch for Cell x (default) x = 0: 1: turn on GPIO9 pull-down 0: turn off GPIO9 pull-down (default)

DCTO	Discharge time out value	DCTO (write)	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
		Time(minutes)	Disabled	0.5	1	2	3	4	5	10	15	20	30	40	60	75	90	120
		DCTO (read)	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
		Time left (minutes)	Disabled or time-out	0 to 0.5	0.5 to 1	1 to 2	2 to 3	3 to 4	4 to 5	5 to 10	10 to 15	15 to 20	20 to 30	30 to 40	40 to 60	60 to 75	75 to 90	90 to120

MUTE	Mute status (read only)	1: mute is activated and discharging is disabled 0: mute is deactivated
FDRF	Force digital redundancy failure	1: forces the digital redundancy comparison for ADC conversions to fail 0: enables the normal redundancy comparison

PS, Bits[1:0]	Digital redundancy path selection	11: redundancy is applied only to the ADC3 digital path 10: redundancy is applied only to the ADC2 digital path 01: redundancy is applied only to the ADC1 digital path 00: redundancy is applied sequentially to the ADC1, ADC2, and ADC3 digital paths during cell conversions and applied to ADC1 during AUX and STATUS conversions
DTMEN	Enable discharge timer monitor	1: enables the discharge timer monitor function if the DTEN pin is asserted 0: disables the discharge timer monitor function. The normal discharge timer function is enabled if the DTEN pin is asserted
CxV	Cell x voltage1	x = 1 to 18 16-bit ADC measurement value for Cell x Cell voltage for Cell x = CxV × 100 µV CxV is rest to 0xFFFF on power-up and after clear command
GxV	GPIO x voltage1	x = 1 to 9 16-bit ADC measurement value for GPIOx Voltage for GPIOx = GxV × 100 µV GxV is reset to 0xFFFF on power-up and after clear command
REF	2nd reference voltage1	16-bit ADC measurement value for 2nd reference
SC	Sum of all cells measurement1	16-bit ADC measurement value of the sum of all cell voltages, sum of all cells voltage = SC × 100 µV × 30
ITMP	Internal die temperature1	16-bit ADC measurement value of the internal die temperature, temperature measurement voltage = ITMP × 100 µV/7.6mV/°C − 276°C
VA	Analog power supply voltage1	16-bit ADC measurement value of the analog power supply voltage, analog power supply voltage = VA × 100 µV, the value of VA is set by external components that must be in the range of 4.5 V to 5.5 V for normal operation
VD	Digital power supply voltage1	16-bit ADC measurement value of the digital power supply voltage, digital power supply voltage = VD × µV, normal range is within 2.7 V to 3.6 V
CxOV	Cell x overvoltage flag	x = 1 to 18 Cell voltage compared to VOV comparison voltage 0: cell x not flagged for overvoltage condition 1: cell x flagged
CxUV	Cell x undervoltage flag	x = 1 to 18 Cell voltage compared to VUV comparison voltage 0: cell x not flagged for undervoltage condition 1: cell x flagged
REV	Revision code	Device revision code
RSVD	Reserved bits	Read: read back value can be 1 or 0
RSVD0	Reserved bits	Read: read back value is always 0
RSVD1	Reserved bits	Read: read back value is always 1
MUXFAIL	Multiplexer self test result	Read:

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<table>
<tr><td></td><td></td><td colspan="6">0: multiplexer passed self test 1: multiplexer failed self test</td></tr>
<tr><td>THSD</td><td>Thermal shutdown status</td><td colspan="6">Read:
0: thermal shutdown has not occurred
1: thermal shutdown has occurred, THSD Bit cleared to 0 on read of Status Register Group B</td></tr>
<tr><td>SCTx[x]</td><td>S pin control bits</td><td colspan="6">0000: drive S pin high (deasserted)
0001: send 1 high pulse on S pin
0010: send 2 high pulses on S pin
0011: send 3 high pulses on S pin
0100: send 4 high pulses on S pin
0101: send 5 high pulses on S pin
0110: send 6 high pulses on S pin
0111: send 7 high pulses on S pin
1xxx: drive S pin low (asserted)</td></tr>
<tr><td>PWMx[x]</td><td>PWM discharge control</td><td colspan="6">0000: selects 0% discharge duty cycle if DCCx = 1 and watchdog timer has expired 0001: selects 6.7% discharge duty cycle if DCCx = 1 and watchdog timer has expired 0010: selects 13.3% discharge duty cycle if DCCx = 1 and watchdog timer has expired
...
1110: selects 93.3% discharge duty cycle if DCCx = 1 and watchdog timer has expired 1111: selects 100% discharge duty cycle if DCCx = 1 and watchdog timer has expired</td></tr>
<tr><td rowspan="9">ICOMn</td><td rowspan="9">Initial communication bits</td><td rowspan="4">Write</td><td rowspan="2">I2C</td><td colspan="2">0110</td><td>0001</td><td>0000</td><td>0111</td></tr>
<tr><td colspan="2">Start</td><td>Stop</td><td>Blank</td><td>No transmit</td></tr>
<tr><td rowspan="2">SPI</td><td colspan="2">1000</td><td>1010</td><td>1001</td><td>1111</td></tr>
<tr><td colspan="2">CSB low</td><td>CSB falling edge</td><td>CSB high</td><td>No transmit</td></tr>
<tr><td rowspan="3">Read</td><td rowspan="2">I2C</td><td colspan="2">0110</td><td>0001</td><td>0000</td><td>0111</td></tr>
<tr><td colspan="2">Start from master</td><td>stop from master</td><td>SDA low be-tween bytes</td><td>SDA high between bytes</td></tr>
<tr><td>SPI</td><td colspan="2">0111</td><td>0001</td><td>0000</td><td>0111</td></tr>
<tr><td>Dn</td><td>I2C/SPI communication data byte</td><td colspan="6">I2C/SPI communication data byteData transmitted (received) to (from) I2C/SPI slave device</td></tr>
<tr><td rowspan="5">FCOMn</td><td rowspan="5">Final communication control bits</td><td rowspan="4">Write</td><td rowspan="2">I2C</td><td colspan="2">0000</td><td>1000</td><td colspan="2">1001</td></tr>
<tr><td></td><td colspan="2">Master ACK</td><td>Master NACK</td><td colspan="2">Master NACK + stop</td></tr>
<tr><td rowspan="2">SPI</td><td colspan="2">X000</td><td>1001</td><td colspan="2"></td></tr>
<tr><td></td><td colspan="2"></td><td>CSB high</td><td colspan="2"></td></tr>
<tr><td rowspan="2">Read</td><td>I2C</td><td>0000</td><td>0111</td><td>1111</td><td>0001</td><td colspan="2">1001</td></tr>
<tr><td></td><td>ACK from master</td><td>ACK from slave</td><td>NACK from slave</td><td>ACK from slave + stop from master</td><td colspan="2">NACK from slave + stop from master</td></tr>
<tr><td></td><td></td><td></td><td>SPI</td><td colspan="6">1111</td></tr>
</table>

1. Voltage equations use the decimal value of registers, 0 to 4095 for 12 bits and 0 to 65535 for 16 bits.

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9 Application Information

9.1 PROVIDING DC POWER

9.1.1 Simple Linear Regulation

The primary supply pin for the GD30BM1018 is the 5 V (±0.5 V) VREG input pin. To generate the required 5 V supply for VREG, the DRIVE pin can be used to form a discrete regulator with the addition of a few external components, as shown in Figure 38. The DRIVE pin provides a 5.7 V output, capable of sourcing 1 mA. When buffered with an NPN transistor, the DRIVE pin provides a stable 5 V over temperature. The NPN transistor must be chosen to have a sufficient Beta over temperature (> 40) to supply the necessary supply current. The peak VREG current requirement of the GD30BM1018 approaches 35 mA when simultaneously communicating over isoSPI and making ADC conversions. If the VREG pin is required to support any additional load, a transistor with an even higher Beta may be required.

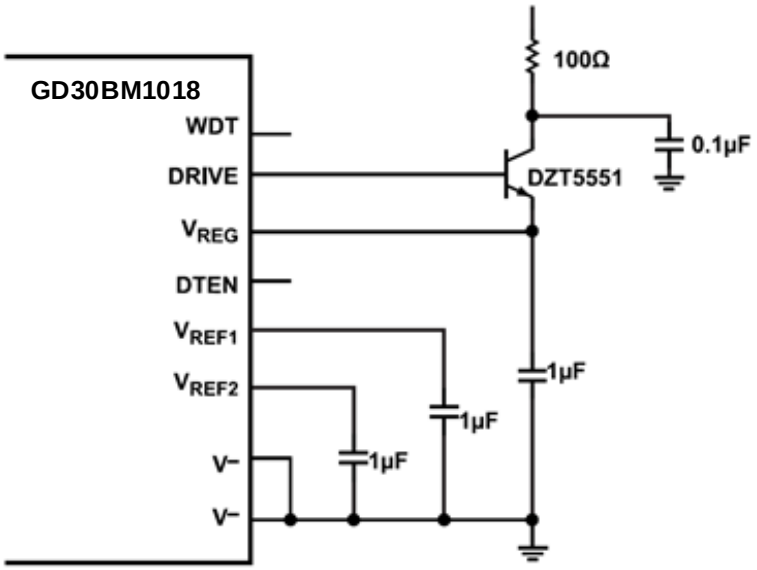

Figure 38. Simple VREG Power Source Using NPN Pass Transistor

The NPN collector can be powered from any voltage source that is a minimum 6 V above V–. This includes the cells that are being monitored, or an unregulated power supply. A 100 Ω, 100 nF RC decoupling network is recommended for the collector power connection to protect the NPN from transients. The emitter of the NPN must be bypassed with a 1 µF capacitor. Larger capacitance must be avoided because this increases the wake-up time of the GD30BM1018. Some attention must be given to the thermal characteristic of the NPN, as there can be significant heating with a high collector voltage.

9.2 Internal Protection and Filtering

9.2.1 Filtering of Cell and GPIO Inputs

The GD30BM1018 uses a Δ-Σ ADC, which includes a Δ-Σ modulator followed by a sinc3 finite impulse response (FIR) digital filter, which greatly relaxes input filtering requirements. Furthermore, the programmable oversampling ratio allows the user to determine the best trade-off between measurement speed and filter cutoff frequency. Even

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with this high order low-pass filter, fast transient noise can still induce some residual noise in measurements, especially in the faster conversion modes. This noise can be minimized by adding an RC, low-pass decoupling to each ADC input, which also helps reject potentially damaging high energy transients. Adding more than about 100 Ω to the ADC inputs begins to introduce a systematic error in the measurement, which can be improved by raising the filter capacitance or mathematically compensating in software with a calibration procedure. For situations that demand the highest level of battery voltage ripple rejection, grounded capacitor filtering is recommended. This configuration has a series resistance and capacitors that decouple high frequency noise to V–. In systems where noise is less periodic or higher oversampling rates are in use, a differential capacitor filter structure is adequate. In this configuration there are series resistors to each input, but the capacitors connect between the adjacent C pins. However, the differential capacitor sections interact. As a result, the filter response is less consistent and results in less attenuation than predicted by the RC, by approximately a decade. Note that the capacitors only see one cell of applied voltage (thus smaller and lower cost) and tend to distribute transient energy uniformly across the IC (reducing stress events on the internal protection structure). Figure 39 shows the two methods schematically. ADC accuracy varies with R and C as shown in the typical performance curves, but the error is minimized if R = 100 Ω and C = 10 nF. The GPIO pins always use a grounded capacitor configuration because the measurements are all with respect to V–.

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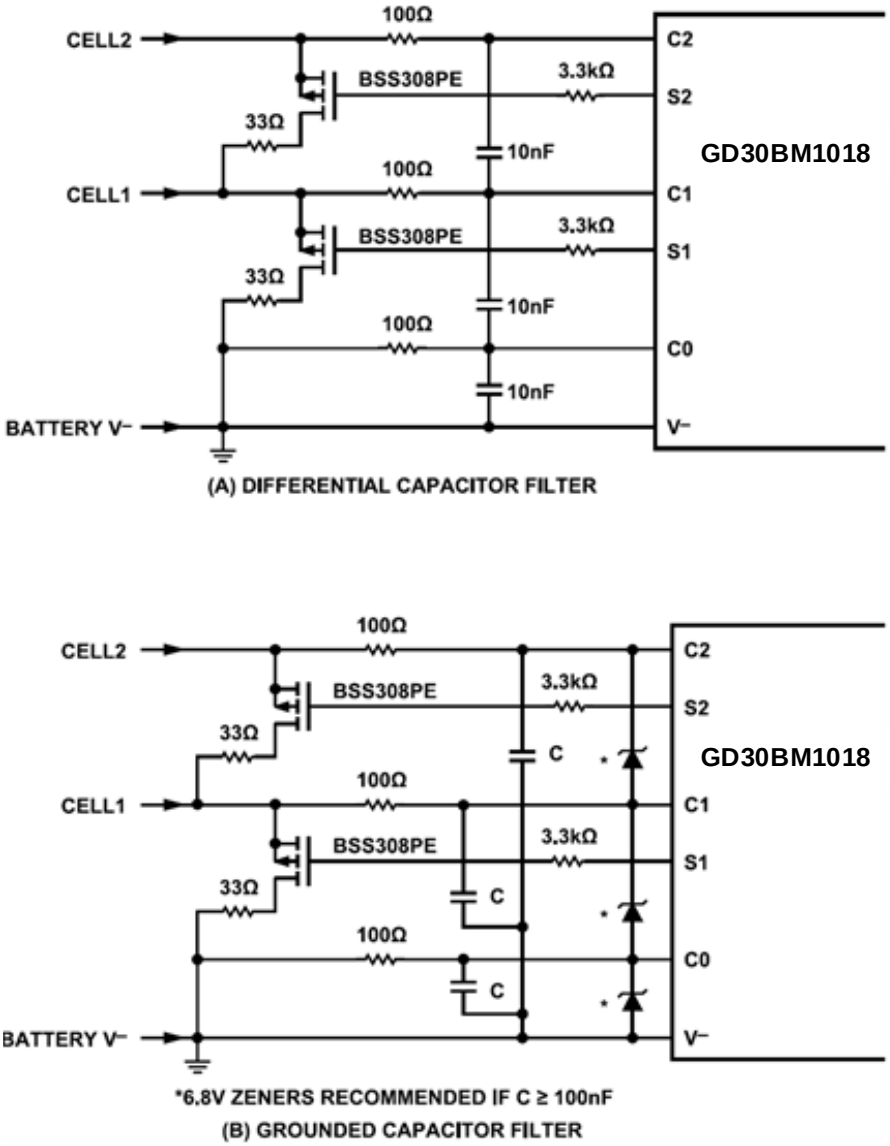

Figure 39. Input Filter Structure Configurations

9.3 Cell Balancing

9.3.1 Cell Balancing with Internal MOSFETs

With passive balancing, if one cell in a series stack becomes over- charged, an S output can slowly discharge this cell by connecting it to a resistor. Each S output is connected to an internal N-channel MOSFET with a maximum on resistance of 10 Ω. An external resistor must be connected in series with these MOSFETs to allow most of the heat to be dissipated outside of the GD30BM1018 package, as shown in Figure 40.

The internal discharge switches (MOSFETs) S1 through S18 can be used to passively balance cells as shown in Figure 40 with balancing current of 200 mA or less (80 mA or less if the die temperature is over 85°C). Balancing current larger than 200 mA is not recommended for the internal switches due to excessive die heating. When discharging cells with the internal discharge switches, the die temperature must be monitored. See the *Thermal Shutdown* section.

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Note that the antialiasing filter resistor is part of the discharge path and must be removed or reduced. Use of an RC for added cell voltage measurement filtering is permitted, but the filter resistor must remain small, typically around 10 Ω to reduce the effect on the balance current.

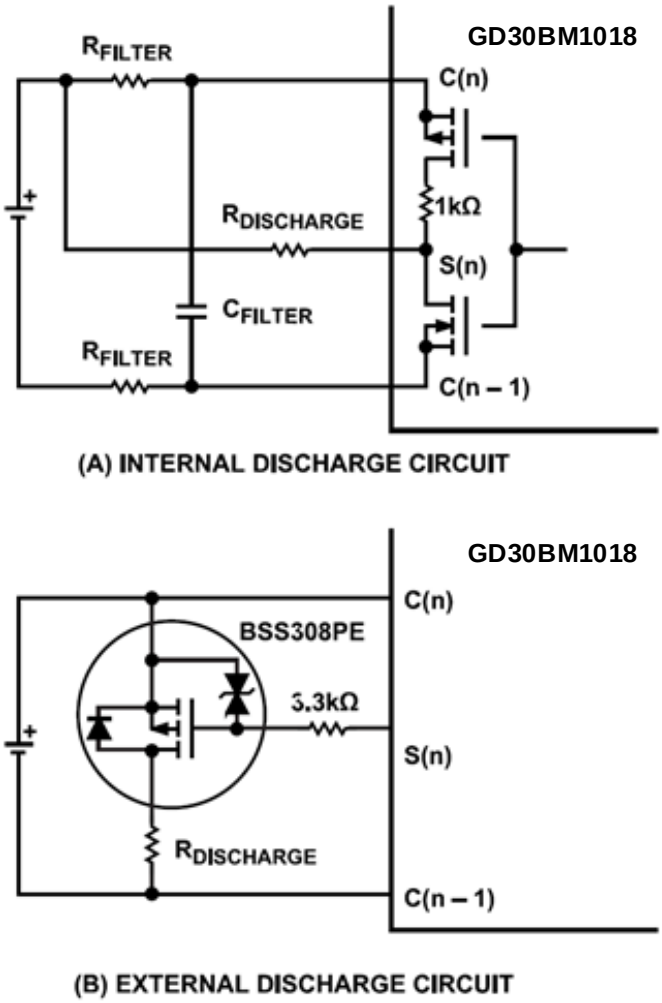

Figure 40. Internal/External Discharge Circuits

9.3.2 Cell Balancing with External Transistors

For applications that require balancing currents above 200 mA or large cell filters, the S outputs can be used to control external transistors. The GD30BM1018 includes an internal pull-up PMOS transistor with a 1 kΩ series resistor. The S pins can act as digital outputs suitable for driving the gate of an external MOSFET, as shown in Figure 40. Figure 39 shows external MOSFET circuits that include RC filtering. For applications with very low cell voltages, the PMOS in Figure 40 can be replaced with a PNP. When a PNP is used, the resistor in series with the base must be reduced.

9.3.3 Choosing a Discharge Resistor

When sizing the balancing resistor, it is important to know the typical battery imbalance and the allowable time for cell balancing. In most small battery applications, it is reasonable for the balancing circuitry to be able to correct for a 5% state of charge (SOC) error with 5 hours of balancing. For example, a 5 AHr battery with a 5% SOC

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imbalance has approximately 250 mA Hrs of imbalance. Using a 50 mA balancing current, the error can be corrected in 5 hours. With a 100 mA balancing current, the error can be corrected in 2.5 hours. In systems with very large batteries, it is difficult to use passive balancing to correct large SOC imbalances in short periods of time. The excessive heat created during balancing generally limits the balancing current. In large capacity battery applications, if short balancing times are required, an active balancing solution must be considered. When choosing a balance resistor, the following equations can be used to help determine a resistor value:

$$\text{Balance Current} = \frac{\%\ \text{of SOC Imbalance} \times \text{Battery Capacity}}{\text{Number of Hours to Balance}} \quad (6)$$

$$\text{Balance Resistor} = \frac{\text{Nominal cell Voltage}}{\text{Balance Current}} \quad (7)$$

9.4 Discharge Control During Cell Measurements

If the discharge permitted (DCP) bit is high at the time of a cell measurement command, the S pin discharge states do not change during cell measurements. If the DCP bit is low, S pin discharge states are disabled while the corresponding cell or adjacent cells are being measured. If using an external discharge transistor, the relatively low 1 kΩ impedance of the internal GD30BM1018 PMOS transistors allow the discharge currents to fully turn off before the cell measurement. In Table 54, off indicates that the S pin discharge is forced off irrespective of the state of the corresponding DCC bit. On indicates that the S pin discharge remains on during the measurement period if it was on prior to the measurement command.

In some cases, it is not possible for the automatic discharge control to eliminate all measurement error caused by running the discharges. This is due to the discharge transistor not turning off fast enough for the cell voltage to completely settle before the measurement starts. For the best measurement accuracy when running discharge, the mute and unmute commands must be used. The mute command can be issued to temporarily disable all discharge transistors before the ADCV command is issued. After the cell conversion completes, an unmute command can be sent to reenable all discharge transistors that were previously on. Using this method maximizes the measurement accuracy with a very small time penalty.

9.4.1 Method to Verify Discharge Circuits

When using the internal discharge feature, the ability to verify discharge functionality can be implemented in the software. In applications using an external discharge MOSFET, an additional resistor can be added between the battery cell and the source of the discharge MOSFET, which allows the system to test discharge functionality.

Table 54. shows the ADCV command with DCP = 0.

Discharge Pin	Cell Measurement Periods						Cell Calibration Periods					
	Cell 1, Cell 7, Cell 13	Cell 2, Cell 8, Cell 14	Cell 3, Cell 9, Cell 15	Cell 4, Cell10, Cell 16	Cell 5, Cell11, Cell 17	Cell 6, Cell12, Cell 18	Cell 1, Cell 7, Cell 13	Cell 2, Cell 8, Cell 14	Cell 3, Cell 9, Cell 15	Cell 4, Cell10, Cell 16	Cell 5, Cell11, Cell 17	Cell 6, Cell12, Cell 18
	t_0 to t_{1M}	t_{1M} to t_{2M}	t_{2M} to t_{3M}	t_{3M} to t_{4M}	t_{4M} to t_{5M}	t_{5M} to t_{6M}	t_{6M} to t_{1C}	t_{1C} to t_{2C}	t_{2C} to t_{3C}	t_{3C} to t_{4C}	t_{4C} to t_{5C}	t_{5C} to t_{6C}
S1	Off	Off	On	On	On	Off	Off	Off	On	On	On	Off
S2	Off	Off	Off	On	On	On	Off	Off	Off	On	On	On
S3	On	Off	Off	Off	On	On	On	Off	Off	Off	On	On
S4	On	On	Off	Off	Off	On	On	On	Off	Off	Off	On

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Discharge Pin	Cell Measurement Periods						Cell Calibration Periods					
	Cell 1, Cell 7, Cell 13	Cell 2, Cell 8, Cell 14	Cell 3, Cell 9, Cell 15	Cell 4, Cell10, Cell 16	Cell 5, Cell11, Cell 17	Cell 6, Cell12, Cell 18	Cell 1, Cell 7, Cell 13	Cell 2, Cell 8, Cell 14	Cell 3, Cell 9, Cell 15	Cell 4, Cell10, Cell 16	Cell 5, Cell11, Cell 17	Cell 6, Cell12, Cell 18
	t_0 to t_{1M}	t_{1M} to t_{2M}	t_{2M} to t_{3M}	t_{3M} to t_{4M}	t_{4M} to t_{5M}	t_{5M} to t_{6M}	t_{6M} to t_{1C}	t_{1C} to t_{2C}	t_{2C} to t_{3C}	t_{3C} to t_{4C}	t_{4C} to t_{5C}	t_{5C} to t_{6C}
S5	On	On	On	Off	Off	Off	On	On	On	Off	Off	Off
S6	Off	On	On	On	Off	Off	Off	On	On	On	Off	Off
S7	Off	Off	On	On	On	Off	Off	Off	On	On	On	Off
S8	Off	Off	Off	On	On	On	Off	Off	Off	On	On	On
S9	On	Off	Off	Off	On	On	On	Off	Off	Off	On	On
S10	On	On	Off	Off	Off	On	On	On	Off	Off	Off	On
S11	On	On	On	Off	Off	Off	On	On	On	Off	Off	Off
S12	Off	On	On	On	Off	Off	Off	On	On	On	Off	Off
S13	Off	Off	On	On	On	Off	Off	Off	On	On	On	Off
S14	Off	Off	Off	On	On	On	Off	Off	Off	On	On	On
S15	On	Off	Off	Off	On	On	On	Off	Off	Off	On	On
S16	On	On	Off	Off	Off	On	On	On	Off	Off	Off	On
S17	On	On	On	Off	Off	Off	On	On	On	Off	Off	Off
S18	Off	On	On	On	Off	Off	Off	On	On	On	Off	Off

Both circuits are shown in Figure 41. The functionality of the discharge circuits can be verified by conducting cell measurements and comparing measurements when the discharge is off to meas- urements when the discharge is on. The measurement taken when the discharge is on requires that the discharge permit (DCP) bit be set. The change in the measurement when the discharge is turned on is calculable based on the resistor values. The following algorithm can be used in conjunction with Figure 41 to verify each discharge circuit:

- Step 1: Measure all cells with no discharging (all S outputs off) and read and store the results.
- Step 2: Turn on S1, S7, and S13.
- Step 3: Measure C1 to C0, C7 to C6, and C13 to C12.
- Step 4: Turn off S1, S7, and S13.
- Step 5: Turn on S2, S8, and S14.
- Step 6: Measure C2 to C1, C8 to C7, and C14 to C13.
- Step 7: Turn off S2, S8, and S14.
- ……
- Step 17: Turn on S6, S12, and S18.
- Step 18: Measure C6 to C5, C12 to C11, and C18 to C17.
- Step 19: Turn off S6, S12, and S18.
- Step 20: Read the Cell Voltage Register Groups to get the results of Step 2 through Step 19.
- Step 21: Compare new readings with old readings. Each cell voltage reading must have decreased by a fixed percentage set by RDISCHARGE and RFILTER for internal designs and RDISCHARGE1 and

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RDISCHARGE2 for external MOSFET designs. The exact amount of the decrease depends on the resistor values and MOSFET characteristics.

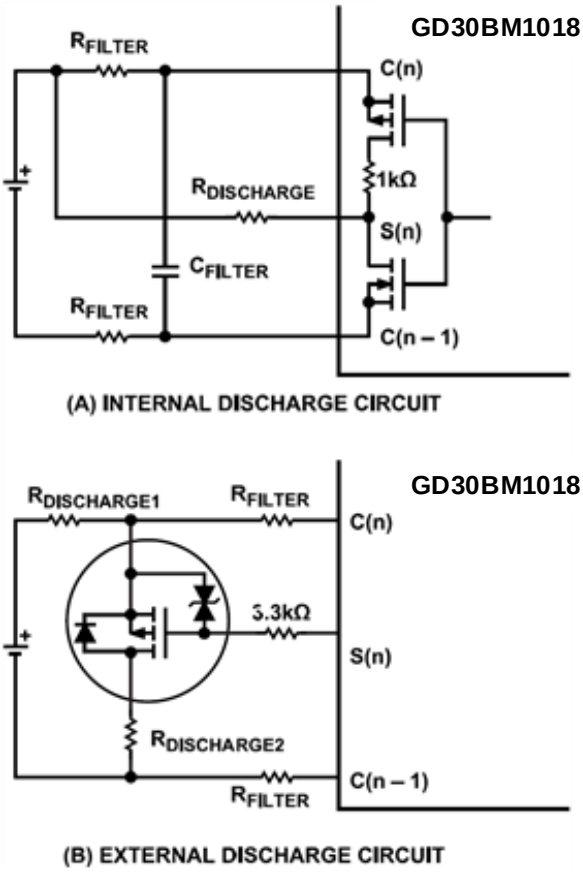

Figure 41. Balancing Self Test Circuit

9.5 Digital Communication

9.5.1 PEC Calculation

The PEC can be used to ensure that the serial data read from the GD30BM1018 is valid and has not been corrupted. This feature is critical for reliable communication, particularly in environments of high noise. The GD30BM1018 requires that a PEC be calculated for all data being read from and written to the GD30BM1018. For this reason, it is important to have an efficient method for calculating the PEC.

The C code provides a simple implementation of a lookup table derived PEC calculation method. There are two functions. The first function init_PEC15_Table() must only be called once when the microcontroller starts and initializes a PEC15 table array called pec15Table[]. This table is used in all future PEC calculations. The PEC15 table can also be hard coded into the microcontroller rather than running the init_PEC15_Table() function at startup. The pec15() function calculates the PEC and returns the correct 15-bit PEC for byte arrays of any given length.

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```
int16 pec15Table[256];

int16 CRC15_POLY = 0x4599;

void init_PEC15_Table()

{

for (int i = 0; i < 256; i++)

{

remainder = i << 7;

for (int bit = 8; bit > 0; --bit)

{

if (remainder & 0x4000)

{

remainder = ((remainder << 1)); remainder = (remainder ^ CRC15_POLY)

}

else

{

remainder = ((remainder << 1));

}

}

pec15Table[i] = remainder&0xFFFF;

}

}

unsigned int16 pec15 (char *data , int len)

{

int16 remainder,address; remainder = 16;//PEC seed for (int i = 0; i < len; i++)

{

address = ((remainder >> 7) ^ data[i]) & 0xff;//calculate PEC table address remainder = (remainder << 8 ) ^ pec15Table[address];

}

return (remainder*2);//The CRC15 has a 0 in the LSB so the final value must be multiplied by 2

}
```


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9.5.2 ISOSPI Ibias and Icmp Setup

The GD30BM1018 allows the isoSPI links of each application to be optimized for power consumption or for noise immunity. The power and noise immunity of an isoSPI system is determined by the programmed IB current, which controls the isoSPI signaling currents. IB can range from 100 µA to 1 mA. Internal circuitry scales up this bias current to create the isoSPI signal currents equal to be 20 × IB. A low IB reduces the isoSPI power consumption in the ready and active states, whereas a high IB increases the amplitude of the differential signal voltage VA across the matching termination resistor, RM. The IB current is programmed by the sum of the RB1 and RB2 resistors connected between the 2 V IBIAS pin and GND, as shown in Figure 42. The receiver input threshold is set by the ICMP voltage that is programmed with the resistor divider created by the RB1 and RB2 resistors. The receiver threshold is half of the voltage present on the ICMP pin.

The following guidelines must be followed when setting IB (100 µA to 1 mA) and the receiver comparator threshold voltage VICMP/2:

RM = Transmission Line Characteristic Impedance Z0

Signal Amplitude = VA = （20×IB）×（RM/2）

Receiver Comparator Threshold (VTCMP) = K × VA

Voltage on ICMP Pin (VCIMP) = 2 × VTCMP

RB2 = VICMP/IB

RB1 = (2/IB) - (RB2)

Select IB and K (signal amplitude VA to receiver comparator threshold ratio) according to the application:

- For lower power links: IB = 0.5 mA and K = 0.5.
- For full power links: IB = 1 mA and K = 0.5.
- For long links (>50m): IB = 1 mA and K = 0.25.

For applications with little system noise, setting IB to 0.5 mA is a good compromise between power consumption and noise immunity. Using this IB setting with a 1:1 transformer and RM = 100 Ω, RB1 must be set to 3.01 k, and RB2 set to 1 kΩ. With a typical CAT5 twisted pair, these settings allow communication up to 50 m. For applications in very noisy environments or that require cables longer than 50 m, it is recommended to increase IB to 1 mA. Higher drive current compensates for the increased insertion loss in the cable and provides high noise immunity. When using cables over 50 m and a transformer with a 1:1 turns ratio and RM = 100 Ω, RB1 is 1.5 k, and RB2 is 499 Ω.

The maximum clock rate of an isoSPI link is determined by the length of the isoSPI cable. For cables 10 m or less, the maximum 1 MHz SPI clock frequency is possible. As the length of the cable increases, the maximum possible SPI clock rate decreases. This dependence is a result of the increased propagation delays that can create possible timing violations.

Cable delay affects three timing specifications: tCLK, t6, and t7. In the electrical characteristics table, each of these specifications is derated by 100 ns to allow for 50 ns of cable delay. For longer cables, the minimum timing parameters may be calculated as shown below:

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$$t_{CLK}, t_6, \text{and } t_7 > 0.9\mu s + 2 \times t_{CABLE} (0.2m \text{ per ns}) \quad (8)$$

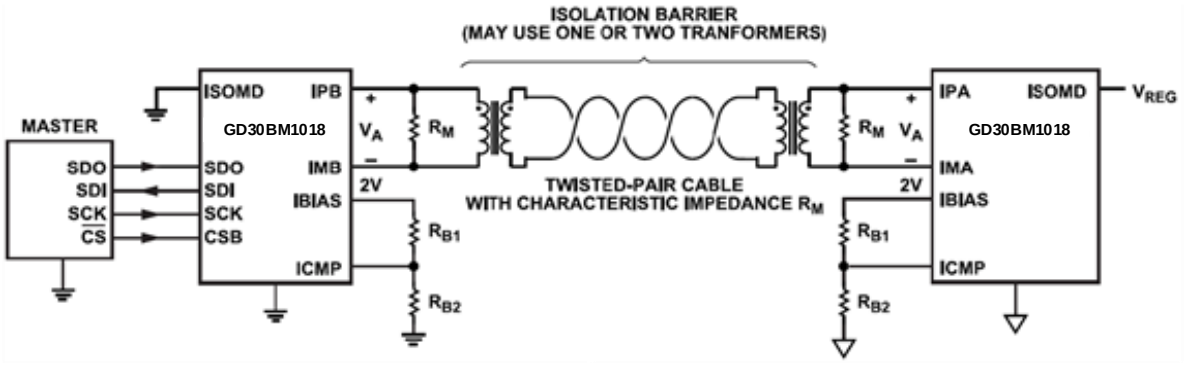

Figure 42. isoSPI Circuit

9.5.3 ISOSPI Layout Guidelines

The layout of the isoSPI signal lines also plays a significant role in maximizing the noise immunity of a data link. The following layout guidelines are recommended:

1. The transformer must be placed as close to the isoSPI cable connector as possible. The distance must be kept less than 2 cm. The GD30BM1018 must be placed close to but at least 1 cm to 2 cm away from the transformer to help isolate the IC from magnetic field coupling.
2. A V– ground plane must not extend under the transformer, the isoSPI connector, or in between the transformer and the connector.
3. The isoSPI signal traces must be as direct as possible while isolated from adjacent circuitry by ground metal or space. No traces must cross the isoSPI signal lines, unless separated by a ground plane on an inner layer.

9.6 Reading External Temperature Probes

Figure 43 shows the typical biasing circuit for a negative temperature coefficient (NTC) thermistor. The 10 kΩ at 25°C is the most popular sensor value and the VREF2 output stage is designed to provide the current required to bias several of these probes. The biasing resistor is selected to correspond to the NTC value so the circuit provides 1.5 V at 25°C (VREF2 is 3 V nominal). The overall circuit response is approximately –1%/°C in the range of typical cell temperatures, as shown in the chart of Figure 43.

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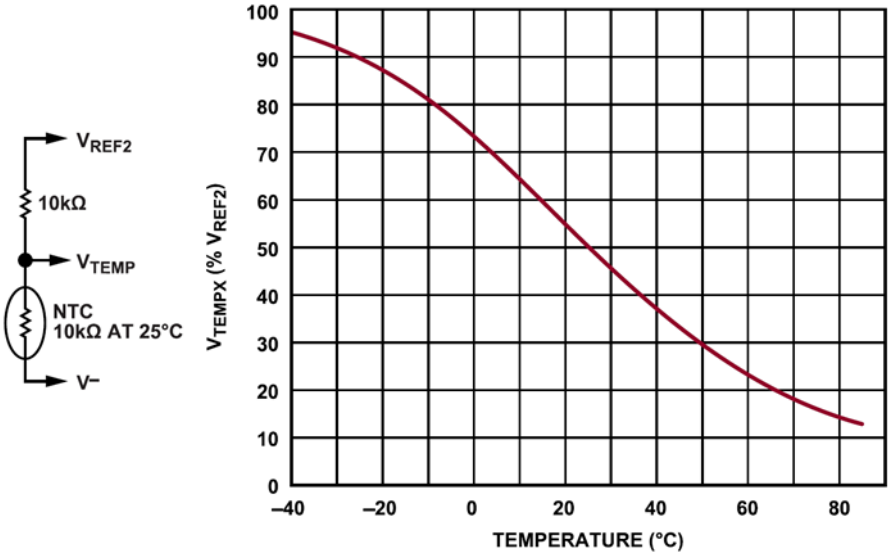

Figure 43. Typical Temperature Probe Circuit and Relative Output

9.7 Typical Application Circuit

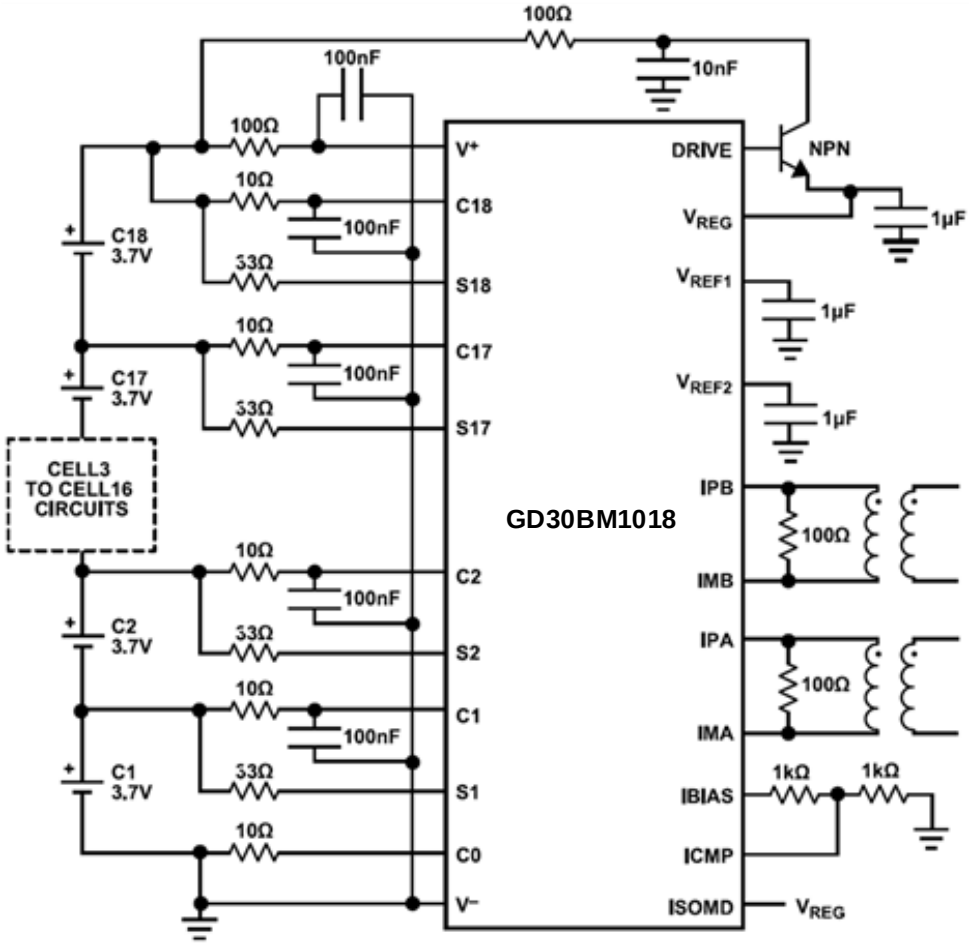

Figure 44. Schematic of GD30BM1018 Application

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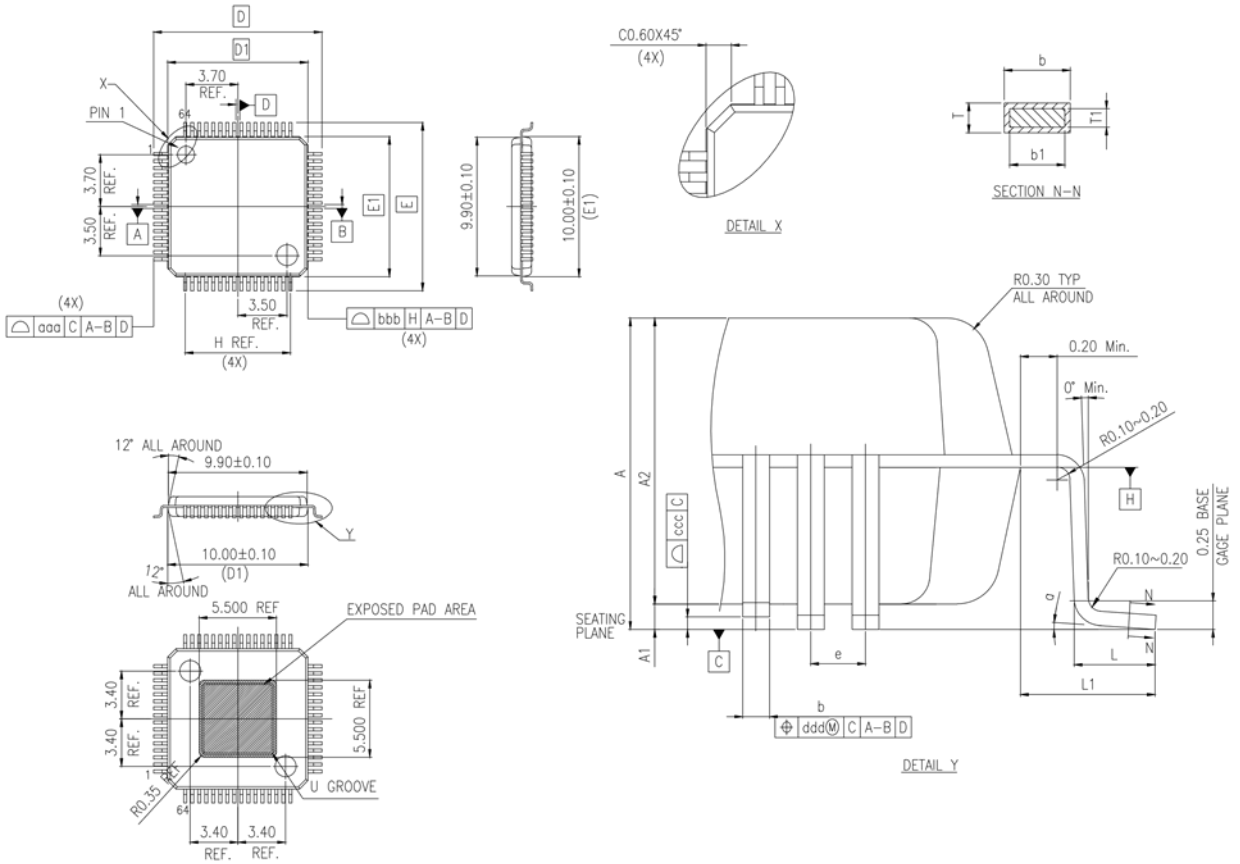
10 Package Information

10.1 Outline Dimensions

LQFP_EP (64) Package Outline



NOTES:

1. All dimensions are in millimeters.
2. Package dimensions does not include mold flash, protrusions, or gate burrs.
3. Refer to the Table 55. *LQFP_EP (64) dimensions(mm)*.

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Table 55. LQFP_EP (64) dimensions(mm)

SYMBOL	MIN	TYP	MAX
A			1.60
A1	0.05	0.10	0.15
A2	1.35	1.40	1.45
D	11.80	12.00	12.20
D1	9.90	10.00	10.10
E	11.80	12.00	12.20
E1	9.90	10.00	10.10
L	0.45	0.60	0.75
L1	1.00 REF		
T	0.09	0.15	0.20
T1	0.097	0.127	0.130
a	0°		7°
b	0.17	0.22	0.22
b1	0.17	0.20	0.23
e	0.50 BASE		
H	7.50 REF		
aaa	0.20		
bbb	0.20		
ccc	0.08		
ddd	0.08		

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11 Ordering Information

Ordering Code	Package Type	ECO Plan	Packing Type	MOQ	OP Temp(°C)
GD30BM1018RWTR-I	LQFP64	Green	Tape & Reel	3000	–40°C to +125°C

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12 Revision History

REVISION NUMBER	DESCRIPTION	DATE
1.0	Initial release and device details	2024

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